Panasonic Electronic Components - MN101LR05DXW Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AM13L
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	64KB (64K x 8)
Program Memory Type	ReRAM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/panasonic/mn101lr05dxw

1.2 Hardware Features

■ Features

In this document, the divided clock and the frequency of it are described as follows:
Divided clock: Clock name/n (n: division ratio)
Frequency: $f_{Clock\ name}$

- CPU Core
  - AM13L core
  - LOAD-STORE architecture (3- or 4-stage Pipeline)
- Machine Cycle and Operating Voltage
  - High-Speed mode
    100 ns / 10 MHz (Max) (V_{DD30}: 1.8 V to 3.6 V)
    1.0 μs / 1 MHz (Max) (V_{DD30}: 1.3 V to 3.6 V)
  - Low-Speed Mode
    25 μs / 40 kHz (Max) (V_{DD30}: 1.1 V to 3.6 V)
- Operating Mode
  - NORMAL mode (High-Speed mode)
  - SLOW mode (Low-Speed mode)
  - HALT mode (High-Speed/Low-Speed mode)
  - STOP mode
- Embedded Memory
  - ROM (ReRAM): 64 KB (Programmable area and Data area vary depending on the ROM name. For details, see Table:1.1.1.)
  - RAM: 4 KB
- ReRAM Specification
  - Program voltage (V_{DD30}): 1.8 V to 3.6 V
  - Program cycles: 1000 times (Program area), 100000 times (Data area)
  - Data is rewritable in bytes without data erase.
- Clock Oscillator (4 circuits)
  - External Low-Speed Oscillation (SOSCCLK): 32.768 kHz (crystal or ceramic)
  - External High-Speed Oscillation (HOSCCLK): up to 10 MHz (crystal or ceramic)
  - Internal Low-Speed Oscillation (SRCCLK): 40 kHz ± 20 % (V_{DD30}: 1.1 V to 3.6 V)
  - Internal High-Speed Oscillation (HRCCLK): 10/8 MHz ± 3 % (V_{DD30}: 1.8 V to 3.6 V)
    1 MHz ± 10 % (V_{DD30}: 1.3 V to 3.6 V)

  * MN101LR02D does not have external high-speed oscillation (HOSCCLK).
- Internal Operating Clock
  - System Clock (SYSCLK): 10 MHz (Max)

  SYSCLK is generated by dividing HCLK or SCLK, and the division ratio is 1, 2, 4, 8, 16 or 32.
  HCLK: HOSCCLK or HRCCLK
  SCLK: SOSCCLK or SRCCLK

  * MN101LR02D cannot be selected HOSCCLK.

- Interrupt Circuit
  MN101LR05D/04D/03D: 31 internal interrupts (except for NMI)
  8 external interrupts (IRQ interrupt: 7, KEY interrupt: 1)
  MN101LR02D: 29 internal interrupts (except for NMI)
  3 external interrupts (IRQ interrupt: 2, KEY interrupt: 1)

- DMA (1 channel)
  - Data transfer size: 8 bits/16 bits
  - Maximum transfer counts: 1023
  - Activation trigger: external interrupts / internal interrupts / software (setting the DMA start bit)

- Watchdog Timer (WDT)
  - Function: 1st watchdog time-out generates NMI, and 2nd consecutive time-out generates a LSI reset.
  - Clock Source: WDTCLK (SOSCCLK or SRCCLK)

- Timer Counter: 13 units
  - General-purpose 8-bit timer (Timer 0/1/2/3/4/5): 6 units
  - General-purpose 16-bit timer (Timer 7/8/9): 3 units
  - 8-bit free-run (Timer 6) /Time-base timer: 1 unit each
  - RTC time base timer (RTC-TBT): 1 unit
  - Real Time Clock (RTC): 1 unit

  <Timer 0>
  - Function: Square wave output, additional pulse PWM output, event count, simple pulse width measurement
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/32, HCLK/64, SCLK, SYSCLK/2, SYSCLK/4, or TM0IO input

  <Timer 1 >
  - Function: Square wave output, event count, 16-bit cascade connection (connected with Timer 0)
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/64, HCLK/128, SCLK, SYSCLK/2, SYSCLK/8, or TM1IO input

  <Timer 2>
  - Function: Square wave output, additional pulse PWM output, event count, simple pulse width measurement
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/32, HCLK/64, SCLK, SYSCLK/2, SYSCLK/4, or TM2IO input

  * MN101LR02D cannot be used simple pulse width measurement.

  <Timer 3 >
  - Function: Square wave output, event count, 16-bit cascade connection (connected with Timer 2)
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/64, HCLK/128, SCLK, SYSCLK/2, SYSCLK/8, or TM3IO input

  <Timer 4>
  - Function: Square wave output, additional pulse PWM output, event count, simple pulse width measurement
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/32, HCLK/64, SCLK, SYSCLK/2, SYSCLK/4, or TM4IO input

  <Timer 5 >
  - Function: Square wave output, event count, 16-bit cascade connection (connected with Timer 4)
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/64, HCLK/128, SCLK, SYSCLK/2, SYSCLK/8, or TM5IO input

  * MN101LR02D cannot be used square wave output, event count and TM5IO.

<Timer 6>
- Function: One-minute timer can be generated in combination with a time base timer.
- Clock Source: HCLK, HCLK/2^7, HCLK/2^{13}, SYSCLK, SCLK, SCLK/2^7 or SCLK/2^{13}

<Time Base Timer>
- Function: An interrupt can be generated at a given set time.
- Clock Source: HCLK or SCLK
- Interrupt generation cycle: $2^N/f_{HCLK}$, $2^N/f_{SCLK}$ (N = 7, 8, 9, 10, 12, 13, 14, 15)

<Timer 7>
- Function: Square wave output, PWM output (duty/cycle are programmable), one-shot pulse output, IGBT output, event count, and input capture
- Clock Source: Generated clock by dividing HCLK, SYSCLK, SCLK, or TM7IO input by 1, 2, 4 or 16.

<Timer 8 >
- Function: Square wave output, PWM output (duty/cycle are programmable), event count, and input capture
- Clock Source: Generated clock by dividing HCLK, SYSCLK, SCLK, or TM8IO input by 1, 2, 4 or 16.

<Timer 9 >
- Function: Square wave output, PWM output (duty/cycle are programmable), event count, and input capture
- Clock Source: Generated clock by dividing HCLK, SYSCLK, SCLK, or TM9IO input by 1, 2, 4 or 16.

* MN101LR03D and MN101LR02D
cannot be used square wave output, PWM output, event count and TM9IO.

<RTC time base timer (RTC-TBT)>
- Function: Clock generation for the Real Time Clock (RTC)
Frequency correction
(Correction Range: ±488 ppm to ±31220 ppm, Accuracy: approx. 0.48 ppm to 30.52 ppm)
- Clock Source: SOSCCLK or SRCCLK

<Real Time Clock (RTC)>
- Function: Calendar calculation, adjustment of leap year
Periodic interrupt (0.5 s, 1 s, 1 min or 1 hour)
Alarm0 interrupt (date/hour/minute), Alarm1 interrupt (month/day/hour/minute)

• Buzzer Output/Inverted Buzzer Output
- Output frequency: $f_{HCLK}/2^M$ (M = 9, 10, 11, 12, 13, 14), $f_{SCLK}/2^N$ (N = 3, 4)

* MN101LR02D can be used inverted buzzer output only.

• Serial Interface: 4 units

<Serial Interface 0, 1> (Full duplex UART/Clock synchronous serial)
- Function:
Full duplex UART:
Parity check, Detection of overrun error/framing error, Selectable transfer bits of 7 or 8
Clock synchronous serial (SPI compatible):
2,3 or 4-wire communication, MSB/LSB first selectable, multiple bytes transmission is available.
- Clock Source: external clock, dedicated baud rate timer

<Serial Interface 2, 3> (Multi-master IIC/Clock synchronous serial)
- Function:
Multi-master IIC
Clock synchronous serial (SPI compatible):
2,3 or 4-wire communication, MSB/LSB first selectable, multiple bytes transmission is available.
- Clock Source: external clock, dedicated baud rate timer

- Package
  MN101LR05D: TQFP080-P-1212 (12 mm square, 0.5 mm pitch, halogen free)
  MN101LR04D: TQFP064-P-1010 (10 mm square, 0.5 mm pitch, halogen free)
  MN101LR03D: TQFP048-P-0707 (7 mm square, 0.5 mm pitch, halogen free)
  MN101LR02D: HQFN032-A-0505 (5 mm square, 0.5 mm pitch, halogen free)

  Panasonic "halogen free" semiconductor products refer to the products made of molding resin and interposer which conform to the following standards.
  - Bromine: 900 ppm (Maximum Concentration Value)
  - Chlorine: 900 ppm (Maximum Concentration Value)
  - Bromine + Chlorine: 1500 ppm (Maximum Concentration Value)

  The above-mentioned standards are based on the numerical value described in IEC61249-2-21.
  Antimony and its compounds are not added intentionally.

- Operating Ambient Temperature: Ta = -40 °C to 85 °C

1.3 Comparison of Product Specification

Table:1.3.1 Functions

Function	Specification	MN101LR05D	MN101LR04D	MN101LR03D	MN101LR02D
Port	I/O port	69 pins	53 pins	37 pins	22 pins
	N-channel transistor drive strength	55 pins	41 pins	27 pins	19 pins
Interrupt	Internal interrupt	31	31	31	29
	External interrupt	8 (7: IRQ0-6, 1: KEY0-7)	8 (7: IRQ0-6, 1: KEY1-7)	8 (7: IRQ0-6, 1: KEY1-5)	3 (2: IRQ4-5, 1: KEY1-7)
Timer 5	Timer I/O	TM5IO	TM5IO	TM5IO	- (*1)
Timer 9	Timer I/O	TM9IO	TM9IO	- (*1)	- (*1)
Serial interface 1		√	√	√	-
Serial interface 3	Serial communication pins	SBO3/SDA3 SBT3/SCL3 SBI3 SBCS3	SBO3/SDA3 SBT3/SCL3 SBI3 SBCS3	SBO3/SDA3 SBT3/SCL3 - -	SBO3/SDA3 SBT3/SCL3 SBI3 -
	Clock synchronous	2, 3 or 4-wire	2, 3 or 4-wire	2-wire	2 or 3-wire
	SPI compatible	√	√	- (*2)	- (*2)
Buzzer	Buzzer output /Inverted buzzer output	BUZ NBUZ	BUZ NBUZ	BUZ NBUZ	- NBUZ
ADC	Analog input	8 pins (AN0-7)	6 pins (AN2-7)	4 pins (AN2-5)	3 pins (AN3-5)
LCD driver	Segment output	43 pins (SEG0-42) /39 pins (SEG4-42)	31 pins (SEG0-30)	21 pins (SEG0-20)	-
	Common output	4 pins (COM0-3) /8 pins (COM0-7)	4 pins (COM0-3)	4 pins (COM0-3)	-
Oscillation		HOSCCLK SOSCCLK HRCCLK SRCCLK	HOSCCLK SOSCCLK HRCCLK SRCCLK	HOSCCLK SOSCCLK HRCCLK SRCCLK	- SOSCCLK HRCCLK SRCCLK
Package		80-pin TQFP	64-pin TQFP	48-pin TQFP	32-pin HQFN

*1 Timer function is available.
*2 Chip select pin is not assigned.

Table:1.3.2 Functions of I/O Port

I/O Port	MN101LR05D								MN101LR04D								MN101LR03D								MN101LR02D							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Port0	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	-	-	-	-	-	√	√	√	-	-	-	-
Port1	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	-	-	-	-	√	√	√	-	-	-
Port2	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	-	-	-	-	-	-	√	-	-	-	-	-	-	-
Port3	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-
Port4	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	√	√	√	√	√	-	-	-	√	√	√	√	√
Port5	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	-	-	-	-	-	√	√	√	-	-	-	-	-
Port6	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	√	√	√	√	-	-	-	-
Port7	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	-	-	-	-	√	√	√	√	-	-	-	-	-	-	-	-
Port8	-	-	√	√	√	√	√	√	-	-	√	√	√	√	√	√	-	-	√	√	√	√	√	√	-	-	-	-	-	-	-	-

√ : implemented I/O port

√ : implemented I/O port (selectable N-channel transistor drive strength)

- : not implemented

Table:1.3.3 Functions of LCD Control

I/O Port	MN101LR05D								MN101LR04D								MN101LR03D							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Port2	-	SEG 36	SEG 37	SEG 38	SEG 39	SEG 40	SEG 41	SEG 42	-	SEG 28	-	-	-	-	SEG 29	SEG 30	-	SEG 20	-	-	-	-	-	-
Port3	SEG 28	SEG 29	SEG 30	SEG 31	SEG 32	SEG 33	SEG 34	SEG 35	SEG 20	SEG 21	SEG 22	SEG 23	SEG 24	SEG 25	SEG 26	SEG 27	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	SEG 18	SEG 19
Port4	SEG 20	SEG 21	SEG 22	SEG 23	SEG 24	SEG 25	SEG 26	SEG 27	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	SEG 18	SEG 19	-	-	-	SEG 7	SEG 8	SEG 9	SEG 10	SEG 11
Port5	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	SEG 18	SEG 19	SEG 8	SEG 9	SEG 10	-	-	-	-	SEG 11	SEG 4	SEG 5	SEG 6	-	-	-	-	-
Port6	SEG 4	SEG 5	SEG 6	SEG 7	SEG 8	SEG 9	SEG 10	SEG 11	SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	-	-	-	-	SEG 0	SEG 1	SEG 2	SEG 3
Port7	COM 0	COM 1	COM 2	COM 3	COM 4/ SEG 0	COM 5/ SEG 1	COM 6/ SEG 2	COM 7/ SEG 3	-	-	-	-	COM 0	COM 1	COM 2	COM 3	-	-	-	-	COM 0	COM 1	COM 2	COM 3
Port8	-	-	VLC 2	VLC 3	C2	C1	-	-	-	-	VLC 2	VLC 3	C2	C1	-	-	-	-	VLC 2	VLC 3	C2	C1	-	-
-	VLC1								VLC1								VLC1							

-: not implemented

LCD control function is not implemented in MN101LR02D.

Set "0" to the registers and bits corresponding to the functions which are not implemented.

Pin No.				Power supply /Oscillations /Reset /Mode control	Port	External interrupt /KEY interrupt	Timer	Serial interface	Buzzer /Clock output	A/D
MN101 LR05D	MN101 LR04D	MN101 LR03D	MN101 LR02D							
45	37	29	21		P44			SBCS2A		
46	38				P45			SBI1B/RXD1B		
47	39				P46			SBO1B/TXD1B		
48	40				P47			SBT1B		
49	41				P50			SBCS1B		
50					P51			SBI3B		
51					P52			SBO3B/SDA3B		
52					P53			SBT3B/SCL3B		
53					P54	KEY0B		SBCS3B		
54	42	30	22		P55	KEY1B	TM1IOA			
55	43	31	23		P56	KEY2B	TM3IOA			
56	44	32	24		P57	KEY3B	TM8IOA		CLKOUTB	
57	45	33			P60	IRQ0B				
58	46	34			P61	IRQ1B				
59	47	35			P62	IRQ2B				
60	48	36			P63	IRQ3B				
61	49		25		P64	KEY4B		SBI0A/RXD0A		
62	50		26		P65	KEY5B		SBO0A/TXD0A		
63	51		27		P66	KEY6B		SBT0A		
64	52		28		P67	KEY7B		SBCS0A		
65	53	37			P70	IRQ6B				
66	54	38			P71	IRQ5B				
67	55	39			P72	IRQ4B	TM3IOB			
68	56	40			P73		TM5IOB			
69					P74					
70					P75					
71					P76					
72					P77					
73	57	41		C1	P82					
74	58	42		C2	P83					
75	59	43		VLC3	P84					
76	60	44		VLC2	P85					
77	61	45		VLC1						
78	62	46	29	VDD30						
79	63	47	30	VDD18						
80	64	48	31	VDD11						

* See Table:1.3.3 for LCD control pins.

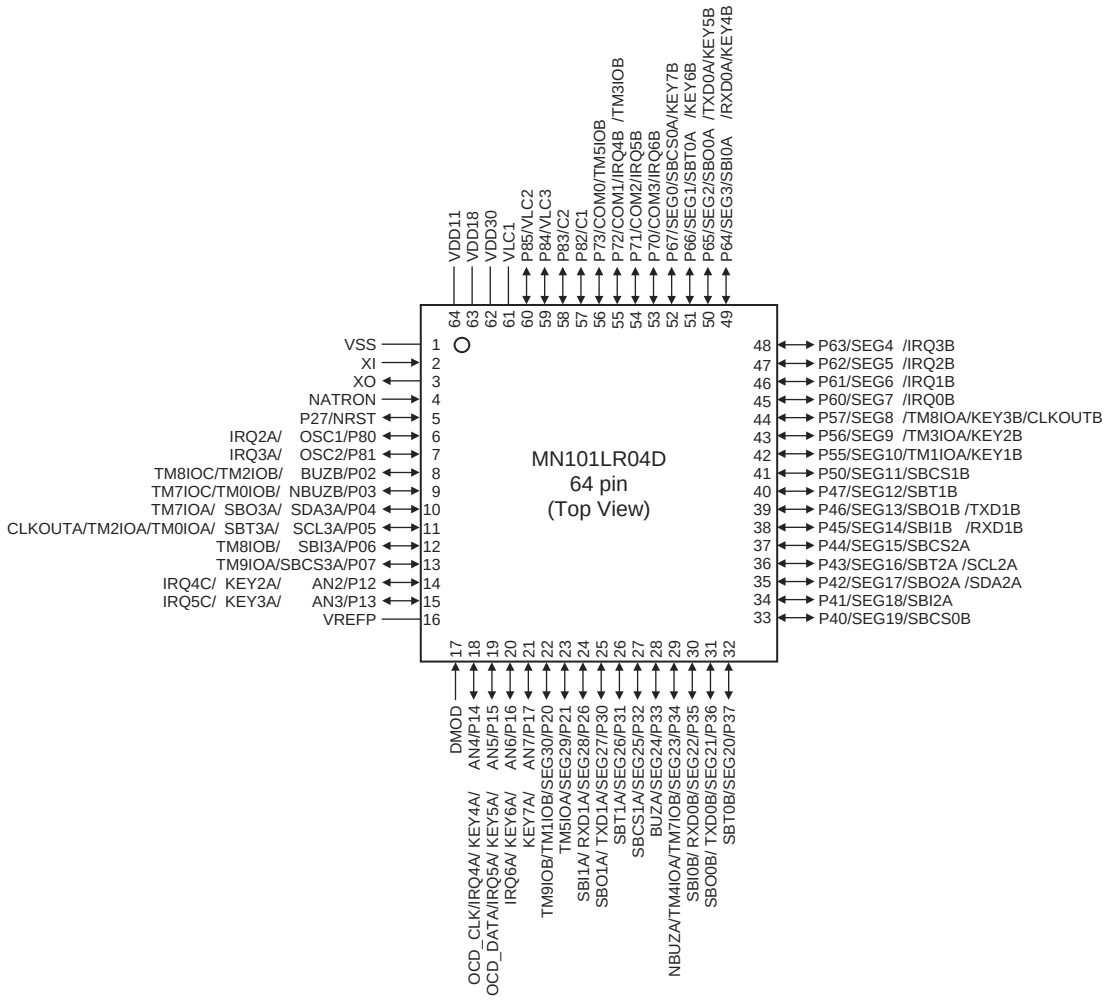

Figure:1.4.2 MN101LR04D Pin Configuration

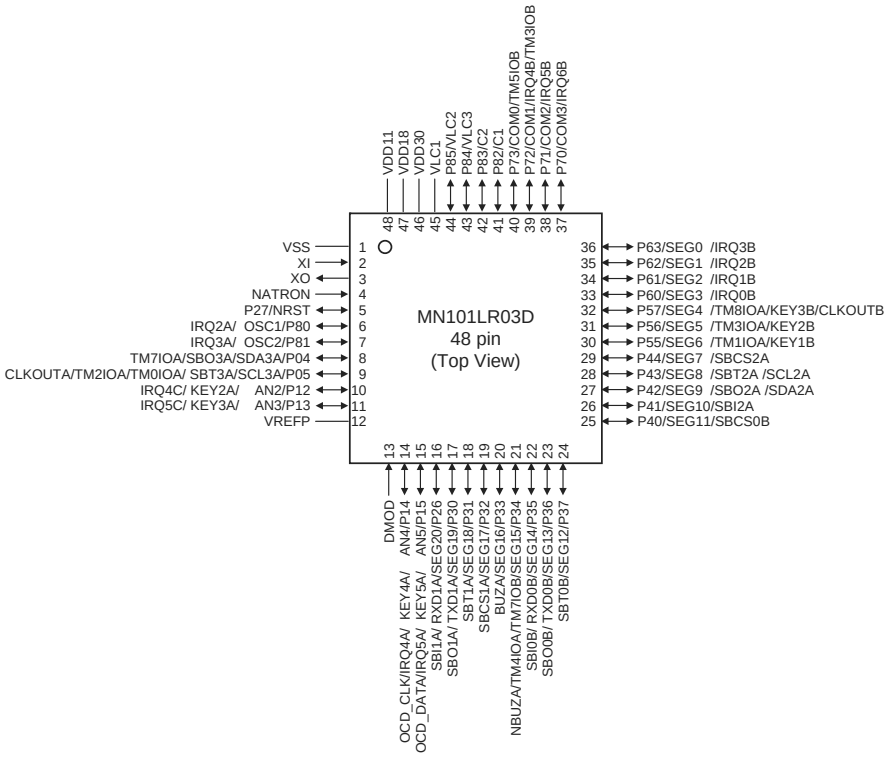

Figure:1.4.3 MN101LR03D Pin Configuration

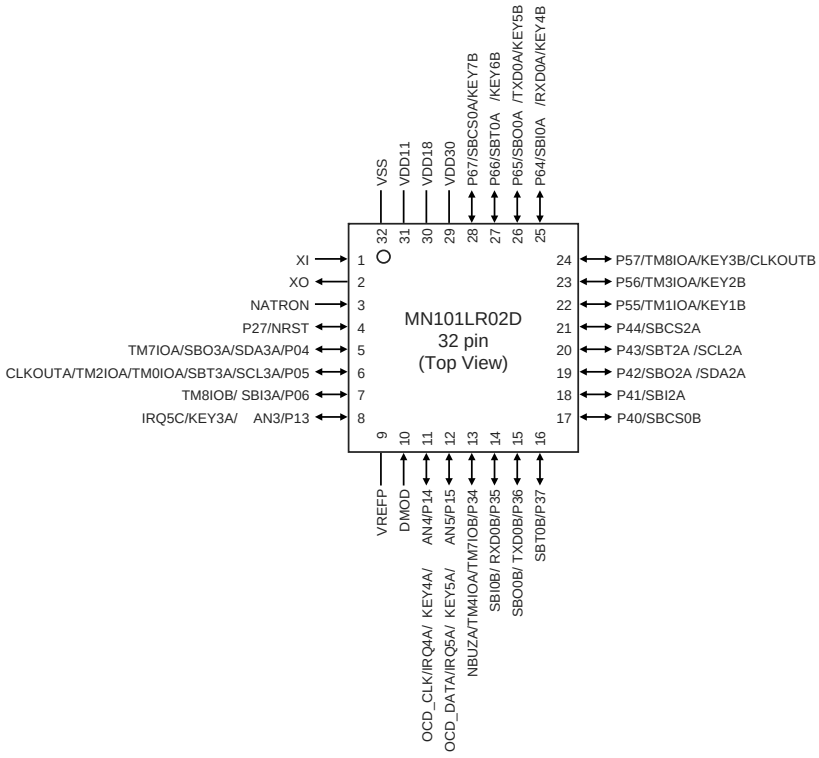

Figure:1.4.4 MN101LR02D Pin Configuration

Table:1.4.2 General-purpose Port Function Pin

Pin name				Input/ Output	Output drive strength selectable	Description
MN101LR 05D	MN101LR 04D	MN101LR 03D	MN101LR 02D			
P00	-	-	-	Input/ Output	Yes	Port 0 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P01	-	-	-		Yes	
P02	P02	-	-		Yes	
P03	P03	-	-		Yes	
P04	P04	P04	P04		Yes	
P05	P05	P05	P05		Yes	
P06	P06	-	P06		Yes	
P07	P07	-	-		Yes	
P10	-	-	-	Input/ Output	No	Port 1 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected.
P11	-	-	-		No	
P12	P12	P12	-		No	
P13	P13	P13	P13		No	
P14	P14	P14	P14		No	
P15	P15	P15	P15		No	
P16	P16	-	-		No	
P17	P17	-	-		No	
P20	P20	-	-	Input/ Output	Yes	Port 2 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P21	P21	-	-		Yes	
P22	-	-	-		Yes	
P23	-	-	-		Yes	
P24	-	-	-		Yes	
P25	-	-	-		Yes	
P26	P26	P26	-		Yes	
P27	P27	P27	P27	Input/ Output	No	Port 2 -LSI is reset by setting P2OUT.P2OUT7 to "0".
P30	P30	P30	-	Input/ Output	Yes	Port 3 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P31	P31	P31	-		Yes	
P32	P32	P32	-		Yes	
P33	P33	P33	-		Yes	
P34	P34	P34	P34		Yes	
P35	P35	P35	P35		Yes	
P36	P36	P36	P36		Yes	
P37	P37	P37	P37		Yes	

Pin name				Input/ Output	Output drive strength selectable	Description
MN101LR 05D	MN101LR 04D	MN101LR 03D	MN101LR 02D			
P40	P40	P40	P40	Input/ Output	Yes	Port 4 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P41	P41	P41	P41		Yes	
P42	P42	P42	P42		Yes	
P43	P43	P43	P43		Yes	
P44	P44	P44	P44		Yes	
P45	P45	-	-		Yes	
P46	P46	-	-		Yes	
P47	P47	-	-		Yes	
P50	P50	-	-	Input/ Output	Yes	Port 5 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P51	-	-	-		Yes	
P52	-	-	-		Yes	
P53	-	-	-		Yes	
P54	-	-	-		Yes	
P55	P55	P55	P55		Yes	
P56	P56	P56	P56		Yes	
P57	P57	P57	P57		Yes	
P60	P60	P60	-	Input/ Output	Yes	Port 6 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P61	P61	P61	-		Yes	
P62	P62	P62	-		Yes	
P63	P63	P63	-		Yes	
P64	P64	-	P64		Yes	
P65	P65	-	P65		Yes	
P66	P66	-	P66		Yes	
P67	P67	-	P67		Yes	
P70	P70	P70	-	Input/ Output	Yes	Port 7 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P71	P71	P71	-		Yes	
P72	P72	P72	-		Yes	
P73	P73	P73	-		Yes	
P74	-	-	-		Yes	
P75	-	-	-		Yes	
P76	-	-	-		Yes	
P77	-	-	-		Yes	
P80	P80	P80	-	Input/ Output	No	Port 8 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected.
P81	P81	P81	-		No	
P82	P82	P82	-		No	
P83	P83	P83	-		No	
P84	P84	P84	-		No	
P85	P85	P85	-		No	

1.5 Electrical Characteristics

1.5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *2 *3 V_{SS} = 0 V

Parameter			Symbol	Rating	Unit
A1	Supply voltage		V_{DD30}	-0.3 to +4.6	V
A2	Input pin voltage		V_I	-0.3 to V_{DD30} + 0.3 (up to 4.6)	V
A3	Output pin voltage		V_O	-0.3 to V_{DD30} + 0.3 (up to 4.6)	
A4	Input/Output pin voltage		V_{IO1}	-0.3 to V_{DD30} + 0.3 (up to 4.6)	
A5	Peak output current	Except P1/8 *4	I_{OL1} (peak)	30	mA
A6		P1/8 *5	I_{OL2} (peak)	10	
A7		All pins	I_{OH} (peak)	-10	
A8	Average output current *1	Except P1/8 *4	I_{OL1} (avg)	20	
A9		P1/8 *5	I_{OL2} (avg)	5	
A10		All pins	I_{OH} (avg)	-5	
A11	Total output current for all pins *1		I_{TOL}	60	
A12			I_{TOH}	-60	
A13	Power dissipation		P_T	230 (Ta = +85 °C)	mW
A14	Operating ambient temperature		T_{opr}	-40 to +85	°C
A15	Storage temperature		T_{stg}	-55 to +125	

*1 The values are applied to any period of 100 ms.

*2 To stabilize the internal power supply voltage, connect bypass capacitors as follows to at least one or more points close to the LSI: Capacitors of 1μF or more between VDD30 and VSS, Capacitors of 0.1 μF and 1μF or more between VOUT18 and VSS.

*3 The absolute maximum ratings are the limit values beyond which the IC may be damaged.
Operation is not guaranteed under these conditions.

*4 The value is applied when selecting the large current output by setting PnNLC register. Except P1 corresponds in MN101LR02D.

*5 P1 corresponds in MN101LR02D.

1.5.2 Operating Condition

B. Operating Condition

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
Supply voltage *6							
B1	Supply voltage	V_{DD1}	$f_{SYSCLK} \leq$ 10.0 MHz	1.8	--	3.6	V
B2		V_{DD2}	$f_{SYSCLK} \leq$ 1.0 MHz *7	1.3	--	3.6	
B3		V_{DD3}	$f_{SYSCLK} \leq$ 40 kHz *8 *10	1.1	--	3.6	
B4	RAM retention supply voltage	V_{DD4}	At STOP mode *10	1.1	--	3.6	
Operating speed *9							
B5	Instruction execution time $1/f_{SYSCLK}$	t_{c1}	V_{DD30} = 1.8 V to 3.6 V	0.1	--	--	µs
B6		t_{c2}	V_{DD30} = 1.3 V to 3.6 V	1.0	--	--	
B7		t_{c3}	V_{DD30} = 1.1 V to 3.6 V *10	25.0	--	--	

*6 f_{SYSCLK}: Frequency for the system clock

*7 When f_{SYSCLK} is generated by using the internal high-speed oscillation.

*8 When f_{SYSCLK} is generated by using the external low-speed oscillation or the internal low-speed oscillation.

*9 tc1,2: When f_{SYSCLK} is generated by using the internal high-speed oscillation or the external high-speed oscillation.
(However, for tc2, only by using the internal high-speed oscillation)
tc3: When f_{SYSCLK} is generated by using the internal low-speed oscillation.

*10 When using auto reset function, the lowest voltage is the auto reset detection voltage.

$V_{DD30} = V_{RSTL}$ to 3.6 V, V_{SS} = 0 V
V_{RSTL} = 1.1 V at auto reset function
Ta = -40 °C to +85 °C

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
External high-speed oscillation Figure:1.5.1 (MN101LR02D is not applicable.)							
B8	Frequency	$F_{HOSCCLK}$	V_{DD30} = 1.8 V to 3.6 V	1.0	--	10.0	MHz
External low-speed oscillation Figure:1.5.2							
B9	Frequency	$F_{SOSCCLK}$	$V_{DD30} = V_{RSTL}$ to 3.6 V	--	32.768	--	kHz
Internal high-speed RC oscillation *11							
B10	Frequency	$F_{HRCCLK10}$	V_{DD30} = 1.8 V to 3.6 V FCNT = "00"	--	10	--	MHz
B11		$F_{HRCCLK8}$	V_{DD30} = 1.8 V to 3.6 V FCNT = "01"	--	8	--	MHz
B12		$F_{HRCCLK1}$	V_{DD30} = 1.3 V to 3.6 V FCNT = "10"	--	1	--	MHz

V_{DD30} = 1.8 V to 3.6 V, V_{SS} = 0 V
V_{RSTL} = 1.1 V at auto reset function
Ta = -40 °C to +85 °C

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is open.) (MN101LR02D is not applicable.)							
B18	Clock frequency	$f_{HOSCCLK}$		1.0	--	10.0	MHz
B19	High period time *12	t_{wh1}	Figure:1.5.3	45	--	--	ns
B20	Low period time *12	t_{wl1}		45	--	--	
B21	Rise time	t_{wr1}	Figure:1.5.3	--	--	5.0	
B22	Fall time	t_{wf1}		--	--	5.0	

*12 Set the clock duty ratio to the value from 45 % to 55 %.

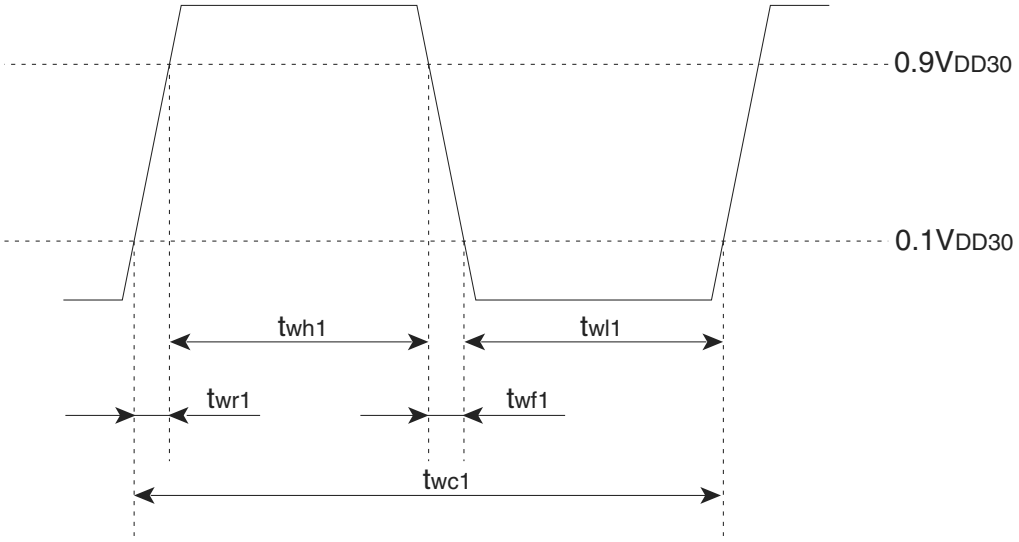

Figure:1.5.3 OSC1 timing diagram

1.5.3 DC Characteristics

C. DC Characteristics

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
Supply current *13							
C1 *14	Operating supply current	I_{DD1}	$f_{HOSCCLK}$ = 10 MHz V_{DD30} = 3.0 V, V_{DD18} = 1.8 V [f_{SYSCLK} = $f_{HOSCCLK}$]	--	2.1	3.1	mA
C2		I_{DD2}	f_{HRCCLK} = 10 MHz V_{DD30} = 3.0 V, V_{DD18} = 1.8 V [f_{SYSCLK} = f_{HRCCLK}]	--	2.1	3.0	
C3		I_{DD3}	f_{HRCCLK} = 8 MHz V_{DD30} = 3.0 V, V_{DD18} = 1.8 V [f_{SYSCLK} = f_{HRCCLK}]	--	1.72	2.5	
C4		I_{DD4}	f_{HRCCLK} = 8 MHz V_{DD30} = 3.0 V, V_{DD18} = 1.8 V [f_{SYSCLK} = f_{HRCCLK}/2]	--	0.94	1.5	
C5 *14		I_{DD5}	$f_{HOSCCLK}$ = 4 MHz V_{DD30} = 3.0 V, V_{DD18} = 1.8 V [f_{SYSCLK} = $f_{HOSCCLK}$]	--	0.84	1.3	
C6		I_{DD6}	f_{HRCCLK} = 1 MHz V_{DD30} = 3.0 V, V_{DD18} = 1.3 V [f_{SYSCLK} = f_{HRCCLK}]	--	0.22	0.36	
C7		I_{DD7}	$f_{SOSCCLK}$ = 32.768 kHz V_{DD30} = 3.0 V, V_{DD18} = 1.1 V [f_{SYSCLK} = $f_{SOSCCLK}$]	--	5.6	9.5	µA
C8		I_{DD8}	f_{SRCCLK} = 40 kHz V_{DD30} = 3.0 V, V_{DD18} = 1.1 V [f_{SYSCLK} = f_{SRCCLK}]	--	6.7	11.6	

*14 MN101LR02D is not applicable.

V_{DD30} = V_{RSTL} to 3.6 V, V_{SS} = 0 V
V_{RSTL} = 1.1 V at auto reset function
Ta = -40 °C to +85 °C

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
Input pin 1 NATRON (Schmitt input)							
C15	High-level input voltage	V_{IH1}		0.8V_{DD30}	--	V_{DD30}	V
C16	Low-level input voltage	V_{IL1}		0	--	0.2V_{DD30}	
C17	Input leakage current	I_{LK1}	V_I = 0 V to V_{DD30}	--	--	± 1	μA
Input pin 2 DMOD (Schmitt input)							
C18	High-level input voltage	V_{IH2}		0.8V_{DD30}	--	V_{DD30}	V
C19	Low-level input voltage	V_{IL2}		0	--	0.2V_{DD30}	
C20	Pull-down resistance	I_{RL2}	V_{DD30} = 3.0 V, V_I = V_{DD30}	30	100	300	kΩ
Input/Output pin 3 (Schmitt input) MN101LR05D: P10 to P17, P80 to P85 MN101LR04D: P12 to P17, P80 to P85 MN101LR03D: P12 to P15, P80 to P85 MN101LR02D: P13 to P15							
C21	High-level input voltage	V_{IH3}		0.8V_{DD30}	--	V_{DD30}	V
C22	Low-level input voltage	V_{IL3}		0	--	0.2V_{DD30}	
C23	Input leakage current	I_{LK3}	V_I = 0 V to V_{DD30}	--	--	± 1	μA
C24	Pull-down resistance	I_{RH3}	V_{DD30} = 3.0 V, V_I = V_{SS} with pull-up resistor	30	100	300	kΩ
C25	High-level output voltage	V_{OH3}	V_{DD30} = 3.0 V, I_{OH} = -2.0 mA	2.4	--	--	V
C26	Low-level output voltage	V_{OL3}	V_{DD30} = 3.0 V, I_{OL} = 2.0 mA	--	--	0.4	
Input/Output pin 4 (Schmitt input) MN101LR05D: P00 to P07, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77 MN101LR04D: P02 to P07, P20, P21, P26, P30 to P37, P40 to P47, P50, P55 to P57, P60 to P67, P70 to P73 MN101LR03D: P04, P05, P26, P30 to P37, P40 to P44, P55 to P57, P60 to P63, P70 to P73 MN101LR02D: P04 to P06, P34 to P37, P40 to P44, P55 to P57, P64 to P67							
C27	High-level input voltage	V_{IH4}		0.8V_{DD30}	--	V_{DD30}	V
C28	Low-level input voltage	V_{IL4}		0	--	0.2V_{DD30}	
C29	Input leakage current	I_{LK4}	V_I = 0 V to V_{DD30}	--	--	±1	μA
C30	Pull-down resistance	I_{RH4}	V_{DD30} = 3.0 V, V_I = V_{SS} with pull-up resistor	30	100	300	kΩ
C31	High-level output voltage	V_{OH4}	V_{DD30} = 3.0 V, I_{OH} = -2.0 mA	2.4	--	--	V
C32	Low-level output voltage 1	V_{OL41}	V_{DD30} = 3.0 V, I_{OL} = 2.0 mA at Large output current OFF	--	--	0.4	
C33	Low-level output voltage 2	V_{OL42}	V_{DD30} = 3.0 V, I_{OL} = 8.0 mA at Large output current ON	--	--	0.4	

1.5.5 Reset/Power supply Detection Characteristics

E. Reset/Power supply Detection Characteristics

V_{DD30} = V_{RSTL} to 3.6 V, V_{SS} = 0 V
V_{RSTL} = 1.1 V at auto reset function
Ta = -40 °C to +85 °C

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
Reset							
E1	Operating supply current	V_{DD3}	With auto reset	V_{RSTL}	--	3.6	V
E2	Auto reset voltage detection level	V_{RSTH}	V_{DD30} = "Low" --> "High"	1.10	1.23	1.35	
E3		V_{RSTL}	V_{DD30} = "High" --> "Low"	1.10	1.18	1.30	
E4	Slope of voltage startup	SL_{VDD30}		--	--	1.0	V/ms
Power supply Detection							
E5	Detection voltage	V_{LVI}		1.00	1.10	1.20	V
				1.05	1.15	1.25	
				1.10	1.20	1.30	
				1.15	1.25	1.35	
				1.20	1.30	1.40	
				1.25	1.35	1.45	
				1.30	1.40	1.50	
				1.40	1.50	1.60	
				1.50	1.60	1.70	
				1.60	1.70	1.80	
				1.70	1.80	1.90	
				1.80	1.90	2.00	
				1.90	2.00	2.10	
				2.00	2.10	2.20	
				2.10	2.20	2.30	
				2.20	2.30	2.40	
				2.30	2.40	2.50	
				2.40	2.50	2.60	
				2.50	2.60	2.70	
				2.60	2.70	2.80	
				2.70	2.80	2.90	
				2.80	2.90	3.00	

■ Package code: HQFN032-A-0505Unit: mm

Figure:1.6.4 32-pin HQFN Package Dimension

This package dimension is subject to change. Before using this product, obtain product spec-

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