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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f071c8t6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 2 Description

The STM32F071x8/xB microcontrollers incorporate the high-performance ARM<sup>®</sup> Cortex<sup>®</sup>-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 128 Kbytes of Flash memory and 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (two I<sup>2</sup>Cs, two SPI/one I<sup>2</sup>S, one HDMI CEC and four USARTs), one 12-bit ADC, one 12-bit DAC with two channels, seven 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F071x8/xB microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F071x8/xB microcontrollers include devices in six different packages ranging from 48 pins to 100 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F071x8/xB microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.



## 3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.5 **Power management**

### 3.5.1 Power supply schemes

- V<sub>DD</sub> = V<sub>DDIO1</sub> = 2.0 to 3.6 V: external power supply for I/Os (V<sub>DDIO1</sub>) and the internal regulator. It is provided externally through VDD pins.
- V<sub>DDA</sub> = from V<sub>DD</sub> to 3.6 V: external analog power supply for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V<sub>DDA</sub> is 2.4 V when the ADC or DAC are used). It is provided externally through VDDA pin. The V<sub>DDA</sub> voltage level must be always greater or equal to the V<sub>DD</sub> voltage level and must be established first.
- V<sub>DDIO2</sub> = 1.65 to 3.6 V: external power supply for marked I/Os. V<sub>DDIO2</sub> is provided externally through the VDDIO2 pin. The V<sub>DDIO2</sub> voltage level is completely independent from V<sub>DD</sub> or V<sub>DDA</sub>, but it must not be provided without a valid supply on V<sub>DD</sub>. The V<sub>DDIO2</sub> supply is monitored and compared with the internal reference voltage (V<sub>REFINT</sub>). When the V<sub>DDIO2</sub> is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- V<sub>BAT</sub> = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V<sub>DD</sub> is not present.

For more details on how to connect power pins, refer to *Figure 12: Power supply scheme*.

### 3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold,  $V_{POR/PDR}$ , without the need for an external reset circuit.

- The POR monitors only the V<sub>DD</sub> supply voltage. During the startup phase it is required that V<sub>DDA</sub> should arrive first and be greater than or equal to V<sub>DD</sub>.
- The PDR monitors both the V<sub>DD</sub> and V<sub>DDA</sub> supply voltages, however the V<sub>DDA</sub> power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V<sub>DDA</sub> is higher than or equal to V<sub>DD</sub>.

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}$  is higher than the  $V_{PVD}$ 



Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

## 3.13 Touch sensing controller (TSC)

The STM32F071x8/xB devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0		TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1	5	TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2	5	TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
	TSC_G2_IO1	PA4		TSC_G6_IO1	PB11
2	TSC_G2_IO2	PA5	6	TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6	0	TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
	TSC_G3_IO1	PC5		TSC_G7_IO1	PE2
3	TSC_G3_IO2	PB0	7	TSC_G7_IO2	PE3
5	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
	TSC_G4_IO1	PA9		TSC_G8_IO1	PD12
4	TSC_G4_IO2	PA10	8	TSC_G8_IO2	PD13
	TSC_G4_IO3	PA11	0	TSC_G8_IO3	PD14
	TSC_G4_IO4	PA12		TSC_G8_IO4	PD15

Table 5. Capacitive sensing GPIOs available on STM32F071x8/xB devices



	Number of capacitive sensing channels						
Analog I/O group	STM32F071Vx	STM32F071Rx	STM32F071Cx				
G1	3	3	3				
G2	3	3	3				
G3	3	3	2				
G4	3	3	3				
G5	3	3	3				
G6	3	3	3				
G7	3	0	0				
G8	3	0	0				
Number of capacitive sensing channels	24	18	17				

Table 6. Number of capacitive sensing channels available
on STM32F071x8/xB devices

## 3.14 Timers and watchdogs

The STM32F071x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

Table 7 compares the features of the different timers.

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	integer from 1 to 65536	Yes	-	-

Table 7. Timer feature comparison



TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

### 3.14.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

### 3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

## 3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on  $V_{DD}$  supply when present or through the  $V_{BAT}$  pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when  $V_{DD}$  power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.



	Pin	numb	pers						Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UFQFPN48	WLCSP49	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
C11	73	-	-	-	PF6	I/O	FT	(3)	-	-
F11	74	47	35	B1	VSS	S	-	-	Ground	
G11	75	48	36	B2	VDDIO2	S	-	-	Digital power su	ıpply
A10	76	49	37	A1	PA14	I/O	FT	(3) (4)	USART2_TX, SWCLK	-
A9	77	50	38	A2	PA15	I/O	FT	(3)	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TIM2_CH1_ETR, EVENTOUT	-
B11	78	51	-	-	PC10	I/O	FT	(3)	USART3_TX, USART4_TX	-
C10	79	52	-	-	PC11	I/O	FT	(3)	USART3_RX, USART4_RX	-
B10	80	53	-	-	PC12	I/O	FT	(3)	USART3_CK, USART4_CK	-
C9	81	-	-	-	PD0	I/O	FT	(3)	SPI2_NSS, I2S2_WS	-
B9	82	-	-	-	PD1	I/O	FT	(3)	SPI2_SCK, I2S2_CK	-
C8	83	54	-	-	PD2	I/O	FT	(3)	USART3_RTS, TIM3_ETR	-
B8	84	-	-	-	PD3	I/O	FT	-	SPI2_MISO, I2S2_MCK, USART2_CTS	-
B7	85	-	-	-	PD4	I/O	FT	-	SPI2_MOSI, I2S2_SD, USART2_RTS	-
A6	86	-	-	-	PD5	I/O	FT	-	USART2_TX	-
B6	87	-	-	-	PD6	I/O	FT	-	USART2_RX	-
A5	88	-	-	-	PD7	I/O	FT	-	USART2_CK	-
A8	89	55	39	A3	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-
A7	90	56	40	A4	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
C5	91	57	41	B4	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6

Table 13. STM32F071x8/xB	pin definitions (	(continued)
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•	Table 15. Alternate functions selected through GPIOB_AFR registers for port B									
Pin name	AF0	AF1	AF2	AF3	AF4	AF5				
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	USART3_CK	-				
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	USART3_RTS	-				
PB2	-	-	-	TSC_G3_IO4	-	-				
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1	-	-				
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2	-	TIM17_BKIN				
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-				
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3	-	-				
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	USART4_CTS	-				
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC		-				
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT		SPI2_NSS, I2S2_WS				
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK, I2S2_CK				
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1	USART3_RX	-				
PB12	SPI2_NSS, I2S2_WS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2	USART3_CK	TIM15_BKIN				
PB13	SPI2_SCK, I2S2_CK	-	TIM1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL				
PB14	SPI2_MISO, I2S2_MCK	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA				
PB15	SPI2_MOSI, I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-				

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Pin name	AF0	AF1
PC0	EVENTOUT	-
PC1	EVENTOUT	-
PC2	EVENTOUT	SPI2_MISO, I2S2_MCK
PC3	EVENTOUT	SPI2_MOSI, I2S2_SD
PC4	EVENTOUT	USART3_TX
PC5	TSC_G3_IO1	USART3_RX
PC6	TIM3_CH1	-
PC7	TIM3_CH2	-
PC8	TIM3_CH3	-
PC9	TIM3_CH4	-
PC10	USART4_TX	USART3_TX
PC11	USART4_RX	USART3_RX
PC12	USART4_CK	USART3_CK
PC13	-	-
PC14	-	-
PC15	-	-

### Table 16. Alternate functions selected through GPIOC\_AFR registers for port C

### Table 17. Alternate functions selected through GPIOD\_AFR registers for port D

Pin name	AF0	AF1
PD0	-	SPI2_NSS, I2S2_WS
PD1	-	SPI2_SCK, I2S2_CK
PD2	TIM3_ETR	USART3_RTS
PD3	USART2_CTS	SPI2_MISO, I2S2_MCK
PD4	USART2_RTS	SPI2_MOSI, I2S2_SD
PD5	USART2_TX	-
PD6	USART2_RX	-
PD7	USART2_CK	-
PD8	USART3_TX	-
PD9	USART3_RX	-
PD10	USART3_CK	-
PD11	USART3_CTS	-
PD12	USART3_RTS	TSC_G8_IO1
PD13	-	TSC_G8_IO2
PD14	-	TSC_G8_IO3
PD15	CRS_SYNC	TSC_G8_IO4



Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
AHB2	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
AHB2	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
AHB1	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
APB	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

### Table 20. STM32F071x8/xB peripheral register boundary addresses



## 6.3 Operating conditions

## 6.3.1 General operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit	
f <sub>HCLK</sub>	Internal AHB clock frequency	-	0	48	M⊔⇒	
f <sub>PCLK</sub>	Internal APB clock frequency	-	0	48	IVITIZ	
V <sub>DD</sub>	Standard operating voltage	-	2.0	3.6	V	
V <sub>DDIO2</sub>	I/O supply voltage	Must not be supplied if $V_{DD}$ is not present	1.65	3.6	V	
V	Analog operating voltage (ADC and DAC not used)	Must have a potential equal	V <sub>DD</sub>	3.6	V	
⊻ DDA	Analog operating voltage (ADC and DAC used)	to or higher than $V_{DD}$	2.4	3.6	v	
V <sub>BAT</sub>	Backup operating voltage	-	1.65	3.6	V	
		TC and RST I/O	-0.3	V <sub>DDIOx</sub> +0.3	v	
V <sub>IN</sub>	I/O input voltage	TTa I/O	-0.3	V <sub>DDA</sub> +0.3 <sup>(1)</sup>		
		FT and FTf I/O	-0.3	5.5 <sup>(1)</sup>		
		BOOT0	0	5.5		
		UFBGA100	-	364		
	Power dissipation at $T_A = 85 \degree C$ for suffix 6 or $T_A = 105 \degree C$ for	LQFP100	-	476		
		LQFP64	-	455	mW	
P <sub>D</sub>		LQFP48	-	370		
	suffix 7 <sup>(2)</sup>	UFQFPN48	-	625		
		WLCSP49	-	408		
	Ambient temperature for the	Maximum power dissipation	-40	85	°C	
т.	suffix 6 version	Low power dissipation <sup>(3)</sup>	-40	105	Ĵ	
ĨĂ	Ambient temperature for the	Maximum power dissipation	-40	105	°C	
	suffix 7 version	Low power dissipation <sup>(3)</sup>	-40	125	Ĵ	
т.	lunction temporature report	Suffix 6 version	-40	105	°C	
TJ	Junction temperature range	Suffix 7 version	-40	125	J <sup>°</sup> C	

### Table 24. General operating conditions

1. For operation with a voltage higher than  $V_{DDIOx}$  + 0.3 V, the internal pull-up resistor must be disabled.

2. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_{Jmax}$ . See Section 7.7: Thermal characteristics.

3. In low power dissipation state,  $T_A$  can be extended to this range as long as  $T_J$  does not exceed  $T_{Jmax}$  (see Section 7.7: *Thermal characteristics*).

## 6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 25* are derived from tests performed under the ambient temperature condition summarized in *Table 24*.



Symbol	Para- meter	Conditions (1)	fнськ	V <sub>DDA</sub> = 2.4 V				V <sub>DDA</sub> = 3.6 V					
				Tun	Max @ T <sub>A</sub> <sup>(2)</sup>		Tun	Max @ T <sub>A</sub> <sup>(2)</sup>			Unit		
				тур	25 °C	85 °C	105 °C	тур	25 °C	85 °C	105 °C	1	
S		HSI48	48 MHz	311	326	334	343	322	337	345	354		
	Supply current in Run or Sleep mode, code executing from Flash memory	Supply current in Run or Sleep mode, code executing	48 MHz	152	170 <sup>(3)</sup>	178	182 <sup>(3)</sup>	165	184 <sup>(3)</sup>	196	200 <sup>(3)</sup>		
			32 MHz	105	121	126	128	113	129	136	138		
			24 MHz	81.9	95.9	99.5	101	88.7	102	107	108		
			8 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5		
I <sub>DDA</sub>			1 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	μA	
		from	from	48 MHz	223	244	255	260	245	265	279	284	
		Flash         HSI clock, memory         32 MHz         176         195         203         206         1           or RAM         24 MHz         154         171         178         181         1	32 MHz	176	195	203	206	193	212	221	224		
	or RAM		168	185	192	195							
		HSI clock, PLL off	8 MHz	74.2	83.4	86.4	87.3	83.4	92.5	95.3	96.6		

Table 30. Typical and maximum current consumption from the  $\mathrm{V}_{\mathrm{DDA}}$  supply

 Current consumption from the V<sub>DDA</sub> supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I<sub>DDA</sub> is independent from the frequency.

2. Data based on characterization results, not tested in production unless otherwise specified.

3. Data based on characterization results and tested in production (using one common test limit for sum of I<sub>DD</sub> and I<sub>DDA</sub>).





Figure 16. Typical application with an 8 MHz crystal

1.  $R_{EXT}$  value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions <sup>(1)</sup>		Тур	Max <sup>(2)</sup>	Unit	
I <sub>DD</sub>		low drive capability	-	0.5	0.9		
	LSE current consumption	medium-low drive capability	-	-	1	μA	
		medium-high drive capability	-	-	1.3		
		high drive capability	-	-	1.6		
g <sub>m</sub>		low drive capability	5	-	-		
	Oscillator transconductance	medium-low drive capability	8	-	-		
		medium-high drive capability	15	-	-	μΑνν	
		high drive capability	25	-	-		
t <sub>SU(LSE)</sub> <sup>(3)</sup>	Startup time	V <sub>DDIOx</sub> is stabilized	-	2	-	S	

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

2. Guaranteed by design, not tested in production.

 t<sub>SU(LSE)</sub> is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer



## High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f <sub>HSI14</sub>	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1 <sup>(2)</sup>	%
DuCy <sub>(HSI14)</sub>	Duty cycle	-	45 <sup>(2)</sup>	-	55 <sup>(2)</sup>	%
		$T_A = -40$ to 105 °C	-4.2 <sup>(3)</sup>	-	5.1 <sup>(3)</sup>	%
ACC	Accuracy of the HSI14 oscillator (factory calibrated)	T <sub>A</sub> = −10 to 85 °C	-3.2 <sup>(3)</sup>	-	3.1 <sup>(3)</sup>	%
ACC <sub>HSI14</sub>		T <sub>A</sub> = 0 to 70 °C	-2.5 <sup>(3)</sup>	-	2.3 <sup>(3)</sup>	%
		T <sub>A</sub> = 25 °C	-1	-	1	%
t <sub>su(HSI14)</sub>	HSI14 oscillator startup time	-	1 <sup>(2)</sup>	-	2 <sup>(2)</sup>	μs
I <sub>DDA(HSI14)</sub>	HSI14 oscillator power consumption	-	-	100	150 <sup>(2)</sup>	μA

### Table 42. HSI14 oscillator characteristics<sup>(1)</sup>

1.  $V_{DDA}$  = 3.3 V,  $T_A$  = -40 to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.



### Figure 19. HSI14 oscillator accuracy characterization results



Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
l <sub>lkg</sub>		TC, FT and FTf I/O TTa in digital mode V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DDIOx</sub>	-	-	± 0.1	
	Input leakage current <sup>(2)</sup>	TTa in digital mode V <sub>DDIOx</sub> ≤ V <sub>IN</sub> ≤ V <sub>DDA</sub>	-	-	1	μA
		TTa in analog mode V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DDA</sub>	-	-	± 0.2	
		FT and FTf I/O V <sub>DDIOx</sub> ≤ V <sub>IN</sub> ≤ 5 V	-	-	10	
R <sub>PU</sub>	Weak pull-up equivalent resistor (3)	V <sub>IN</sub> = V <sub>SS</sub>	25	40	55	kΩ
R <sub>PD</sub>	Weak pull-down equivalent resistor <sup>(3)</sup>	V <sub>IN</sub> = - V <sub>DDIOx</sub>	25	40	55	kΩ
C <sub>IO</sub>	I/O pin capacitance	-	-	5	-	pF

Table 53. I/O static	characteristics (	(continued)
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1. Data based on design simulation only. Not tested in production.

2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 52: I/O current injection susceptibility*.

 Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 21* for standard I/Os, and in *Figure 22* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.





Figure 29. SPI timing diagram - slave mode and CPHA = 0





1. Measurement points are done at CMOS levels: 0.3  $V_{\text{DD}}$  and 0.7  $V_{\text{DD}}$ 



### **Device marking**

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.



### Figure 36. UFBGA100 package marking example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



### **Device marking**

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.





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Cumhal		millimeters		inches <sup>(1)</sup>		
Зупрог	Min	Тур	Max	Min	Тур	Max
А	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 <sup>(2)</sup>	-	0.025	-	-	0.0010	-
b <sup>(3)</sup>	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.242	3.277	3.312	0.1276	0.1290	0.1304
E	3.074	3.109	3.144	0.1210	0.1224	0.1238
е	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.4385	-	-	0.0173	-
G	-	0.3545	-	-	0.0140	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ССС	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.



## 7.7 Thermal characteristics

The maximum chip junction temperature (T<sub>J</sub>max) must never exceed the values given in *Table 24: General operating conditions*.

The maximum chip-junction temperature,  $T_{\rm J}$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J max = T_A max + (P_D max x \Theta_{JA})$$

Where:

- T<sub>A</sub> max is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W,
- P<sub>D</sub> max is the sum of P<sub>INT</sub> max and P<sub>I/O</sub> max (P<sub>D</sub> max = P<sub>INT</sub> max + P<sub>I/O</sub>max),
- P<sub>INT</sub> max is the product of I<sub>DD</sub> and V<sub>DD</sub>, expressed in Watts. This is the maximum chip internal power.

 $\mathsf{P}_{I\!/\!O}$  max represents the maximum power dissipation on output pins where:

 $\mathsf{P}_{\mathsf{I/O}} \max = \Sigma \; (\mathsf{V}_{\mathsf{OL}} \times \mathsf{I}_{\mathsf{OL}}) + \Sigma \; ((\mathsf{V}_{\mathsf{DDIOx}} - \mathsf{V}_{\mathsf{OH}}) \times \mathsf{I}_{\mathsf{OH}}),$ 

taking into account the actual V\_{OL} / I\_{OL} and V\_{OH} / I\_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
	<b>Thermal resistance junction-ambient</b> UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
0	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
OJA	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	49	

Table 77. Package thermal characteristics

### 7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

### 7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.



# 9 Revision history

Date	Revision	Changes
13-Jan-2014	1	Initial draft
21-Feb-2014	2	Added part number STM32F071V8. Changed status of document from "Preliminary data" to "Production data". Updated "Reset and power management" data in <i>Features</i> . Updated t <sub>S_vrefint</sub> in <i>Table: Embedded internal reference</i> <i>voltage</i> . Updated V <sub>HSEH</sub> and V <sub>HSEL</sub> in <i>Table: High-speed external user</i> <i>clock characteristics</i> . Updated V <sub>LSEH</sub> and V <sub>LSEL</sub> in <i>Table: Low-speed external user</i> <i>clock characteristics</i> . Updated t <sub>S_temp</sub> in <i>Table: TS characteristics</i> . Updated t <sub>S_vbat</sub> in <i>Table: VBAT monitoring characteristics</i> . Updated <i>Figure: UFBGA100 package top view</i> and <i>Figure:</i> <i>WLCSP49 package top view</i> . Modified value of t <sub>S_sc</sub> and removed row V <sub>BG</sub> in <i>Table:</i> <i>Comparator characteristics</i> .
17-Dec-2015	3	<ul> <li>Cover page: <ul> <li>part numbers moved to title and table of part numbers removed</li> <li>generic product name in the whole document changed to STM32F071x8/xB</li> </ul> </li> <li>Section 2: Description: <ul> <li>Figure 1: Block diagram updated</li> <li>Section 3: Functional overview:</li> <li>Figure 2: Clock tree updated</li> <li>Section 3.5.4: Low-power modes - added USART2 to comm. peripherals configurable to operate with HSI</li> </ul> </li> <li>Section 4: Pinouts and pin descriptions: <ul> <li>Package pinout figures updated (look and feel)</li> <li>Figure 8: WLCSP49 package pinout - now presented in top view</li> <li>Figure 3: UFBGA100 package pinout - names of PC14, PC15, PF0, PF1 complemented</li> <li>Table 13: STM32F071x8/xB pin definitions - pin types corrected for PF0 and PF1</li> </ul> </li> <li>Section 5: Memory mapping: <ul> <li>Figure 9: added information on STM32F071V8 difference versus STM32F071xB map</li> </ul> </li> </ul>

### Table 79. Document revision history

