



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f071cbt7tr

3.14.6	SysTick timer	23
3.15	Real-time clock (RTC) and backup registers	23
3.16	Inter-integrated circuit interface (I ² C)	24
3.17	Universal synchronous/asynchronous receiver/transmitter (USART)	25
3.18	Serial peripheral interface (SPI) / Inter-integrated sound interface (I ² S)	26
3.19	High-definition multimedia interface (HDMI) - consumer electronics control (CEC)	26
3.20	Clock recovery system (CRS)	27
3.21	Serial wire debug port (SW-DP)	27
4	Pinouts and pin descriptions	28
5	Memory mapping	43
6	Electrical characteristics	46
6.1	Parameter conditions	46
6.1.1	Minimum and maximum values	46
6.1.2	Typical values	46
6.1.3	Typical curves	46
6.1.4	Loading capacitor	46
6.1.5	Pin input voltage	46
6.1.6	Power supply scheme	47
6.1.7	Current consumption measurement	48
6.2	Absolute maximum ratings	49
6.3	Operating conditions	51
6.3.1	General operating conditions	51
6.3.2	Operating conditions at power-up / power-down	51
6.3.3	Embedded reset and power control block characteristics	52
6.3.4	Embedded reference voltage	53
6.3.5	Supply current characteristics	53
6.3.6	Wakeup time from low-power mode	64
6.3.7	External clock source characteristics	64
6.3.8	Internal clock source characteristics	68
6.3.9	PLL characteristics	72
6.3.10	Memory characteristics	72
6.3.11	EMC characteristics	73

Table 47.	Flash memory endurance and data retention	73
Table 48.	EMS characteristics	73
Table 49.	EMI characteristics	74
Table 50.	ESD absolute maximum ratings	75
Table 51.	Electrical sensitivities	75
Table 52.	I/O current injection susceptibility	76
Table 53.	I/O static characteristics	76
Table 54.	Output voltage characteristics	79
Table 55.	I/O AC characteristics	80
Table 56.	NRST pin characteristics	81
Table 57.	ADC characteristics	82
Table 58.	R_{AIN} max for $f_{ADC} = 14$ MHz	84
Table 59.	ADC accuracy	84
Table 60.	DAC characteristics	86
Table 61.	Comparator characteristics	88
Table 62.	TS characteristics	90
Table 63.	V_{BAT} monitoring characteristics	90
Table 64.	TIMx characteristics	90
Table 65.	IWDG min/max timeout period at 40 kHz (LSI)	91
Table 66.	WWDG min/max timeout value at 48 MHz (PCLK)	91
Table 67.	I ² C analog filter characteristics	92
Table 68.	SPI characteristics	92
Table 69.	I ² S characteristics	94
Table 70.	UFBGA100 package mechanical data	97
Table 71.	UFBGA100 recommended PCB design rules	98
Table 72.	LQPF100 package mechanical data	100
Table 73.	LQFP64 package mechanical data	103
Table 74.	WLCSP49 package mechanical data	107
Table 75.	LQFP48 package mechanical data	110
Table 76.	UFQFPN48 package mechanical data	113
Table 77.	Package thermal characteristics	115
Table 78.	Ordering information scheme	118
Table 79.	Document revision history	119

Figure 49.	Recommended footprint for UFQFPN48 package	113
Figure 50.	UFQFPN48 package marking example	114
Figure 51.	LQFP64 P_D max versus T_A	117

precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = 3.3$ V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA} , and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to [Table 28: Embedded internal reference voltage](#) for the value and precision of the internal reference voltage.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- Periodic wakeup unit with programmable resolution and period.
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I²C)

Up to two I²C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on most of the associated I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I²C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts

Table 10. STM32F071x8/xB USART implementation (continued)

USART modes/features ⁽¹⁾	USART1 and USART2	USART3 and USART4
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X = supported.

3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I²S)

Two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I²S interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F071x8/xB SPI/I²S implementation

SPI features ⁽¹⁾	SPI1 and SPI2
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I ² S mode	X
TI mode	X

1. X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory

Table 13. STM32F071x8/xB pin definitions (continued)

Pin numbers					Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UQFPN48	WLCSP49					Alternate functions	Additional functions
B5	92	58	42	C4	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	-
B4	93	59	43	D4	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_I04	-
A4	94	60	44	A5	BOOT0	I	B	-	Boot memory selection	
A3	95	61	45	B5	PB8	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC	-
B3	96	62	46	C5	PB9	I/O	FTf	-	SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-
C3	97	-	-	-	PE0	I/O	FT	-	EVENTOUT, TIM16_CH1	-
A2	98	-	-	-	PE1	I/O	FT	-	EVENTOUT, TIM17_CH1	-
D3	99	63	47	A6	VSS	S	-	-	Ground	
C4	100	64	48	A7	VDD	S	-	-	Digital power supply	

- PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF.
 - These GPIOs must not be used as current sources (e.g. to drive an LED).
- After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
- PC6, PC7, PC8, PC9, PA8, PA9, PA10, PA11, PA12, PA13, PF6, PA14, PA15, PC10, PC11, PC12, PD0, PD1 and PD2 I/Os are supplied by VDDIO2.
- After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 27. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}$	PVD current consumption	-	-	0.15	0.26 ⁽¹⁾	μA

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in [Table 28](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 28. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10 ⁽¹⁾	μs
$t_{S_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4 ⁽¹⁾	-	-	μs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DDA} = 3\text{ V}$	-	-	10 ⁽¹⁾	mV
T_{Coeff}	Temperature coefficient	-	- 100 ⁽¹⁾	-	100 ⁽¹⁾	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 13: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 33. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

Symbol	Parameter	f _{HCLK}	Typical consumption in Run mode		Typical consumption in Sleep mode		Unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	
I _{DD}	Current consumption from V _{DD} supply	48 MHz	23.5	13.5	14.6	3.5	mA
		36 MHz	18.3	10.5	11.1	2.9	
		32 MHz	16.0	9.6	10.0	2.7	
		24 MHz	12.3	7.6	7.8	2.2	
		16 MHz	8.6	5.3	5.5	1.7	
		8 MHz	4.8	3.1	3.1	1.2	
		4 MHz	3.1	2.1	2.2	1.1	
		2 MHz	2.1	1.6	1.6	1.0	
		1 MHz	1.6	1.3	1.4	1.0	
		500 kHz	1.3	1.2	1.2	1.0	
I _{DDA}	Current consumption from V _{DDA} supply	48 MHz	163.3				μA
		36 MHz	124.3				
		32 MHz	111.9				
		24 MHz	87.1				
		16 MHz	62.5				
		8 MHz	2.5				
		4 MHz	2.5				
		2 MHz	2.5				
		1 MHz	2.5				
		500 kHz	2.5				

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 53: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt

Table 52. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 and PF1 pins	-0	NA	mA
	Injected current on PC0 pin	-0	+5	
	Injected current on PA11 and PA12 pins with induced leakage current on adjacent pins less than -1 mA	-5	NA	
	Injected current on all other FT and FTf pins	-5	NA	
	Injected current on all other TTa, TC and RST pins	-5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 53](#) are derived from tests performed under the conditions summarized in [Table 24: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 53. I/O static characteristics

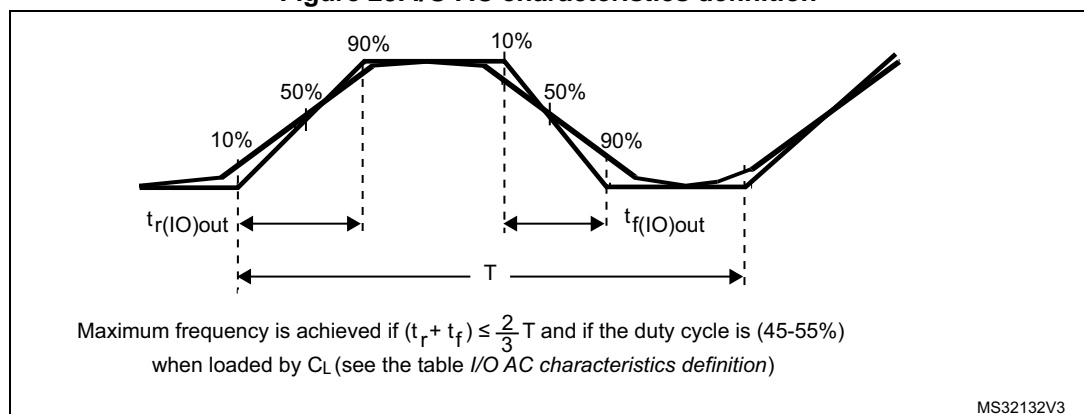
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3 V_{DDIOx} + 0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475 V_{DDIOx} - 0.2^{(1)}$	
		BOOT0	-	-	$0.3 V_{DDIOx} - 0.3^{(1)}$	
		All I/Os except BOOT0 pin	-	-	$0.3 V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445 V_{DDIOx} + 0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5 V_{DDIOx} + 0.2^{(1)}$	-	-	
		BOOT0	$0.2 V_{DDIOx} + 0.95^{(1)}$	-	-	
		All I/Os except BOOT0 pin	$0.7 V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(1)}$	-	mV
		FT and FTf I/O	-	$100^{(1)}$	-	
		BOOT0	-	$300^{(1)}$	-	

Table 55. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

OSPEEDRy [1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
Fm+ configuration (4)	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{\text{DDIOx}} \geq 2 \text{ V}$	-	2	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	12	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	34	
	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{\text{DDIOx}} < 2 \text{ V}$	-	0.5	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	16	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	44	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in [Figure 23](#).
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Figure 23. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} .

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 56. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{IL}(\text{NRST})}$	NRST input low level voltage	-	-	-	$0.3 V_{\text{DD}} + 0.07^{(1)}$	V
$V_{\text{IH}(\text{NRST})}$	NRST input high level voltage	-	$0.445 V_{\text{DD}} + 0.398^{(1)}$	-	-	

Table 57. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{TRIG}}^{(2)}$	External trigger frequency	$f_{\text{ADC}} = 14 \text{ MHz}$, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{\text{ADC}}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
$R_{\text{AIN}}^{(2)}$	External input impedance	See Equation 1 and Table 58 for details	-	-	50	k Ω
$R_{\text{ADC}}^{(2)}$	Sampling switch resistance	-	-	-	1	k Ω
$C_{\text{ADC}}^{(2)}$	Internal sample and hold capacitor	-	-	-	8	pF
$t_{\text{CAL}}^{(2)(3)}$	Calibration time	$f_{\text{ADC}} = 14 \text{ MHz}$	5.9			μs
		-	83			$1/f_{\text{ADC}}$
$W_{\text{LATENCY}}^{(2)(4)}$	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
$t_{\text{latr}}^{(2)}$	Trigger conversion latency	$f_{\text{ADC}} = f_{\text{PCLK}}/2 = 14 \text{ MHz}$	0.196			μs
		$f_{\text{ADC}} = f_{\text{PCLK}}/2$	5.5			$1/f_{\text{PCLK}}$
		$f_{\text{ADC}} = f_{\text{PCLK}}/4 = 12 \text{ MHz}$	0.219			μs
		$f_{\text{ADC}} = f_{\text{PCLK}}/4$	10.5			$1/f_{\text{PCLK}}$
		$f_{\text{ADC}} = f_{\text{HSI14}} = 14 \text{ MHz}$	0.179	-	0.250	μs
Jitter _{ADC}	ADC jitter on trigger conversion	$f_{\text{ADC}} = f_{\text{HSI14}}$	-	1	-	$1/f_{\text{HSI14}}$
$t_{\text{S}}^{(2)}$	Sampling time	$f_{\text{ADC}} = 14 \text{ MHz}$	0.107	-	17.1	μs
		-	1.5	-	239.5	$1/f_{\text{ADC}}$
$t_{\text{STAB}}^{(2)}$	Stabilization time	-	14			$1/f_{\text{ADC}}$
$t_{\text{CONV}}^{(2)}$	Total conversion time (including sampling time)	$f_{\text{ADC}} = 14 \text{ MHz}$, 12-bit resolution	1	-	18	μs
		12-bit resolution	14 to 252 (t_{S} for sampling + 12.5 for successive approximation)			$1/f_{\text{ADC}}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 μA on I_{DDA} and 60 μA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 58. R_{AIN} max for $f_{ADC} = 14$ MHz

T_s (cycles)	t_s (μs)	R_{AIN} max (kΩ) ⁽¹⁾
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 59. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Test conditions	Typ	Max ⁽⁴⁾	Unit
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ kΩ $V_{DDA} = 3$ V to 3.6 V $T_A = 25$ °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ kΩ $V_{DDA} = 2.7$ V to 3.6 V $T_A = -40$ to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ kΩ $V_{DDA} = 2.4$ V to 3.6 V $T_A = 25$ °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.

2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 6.3.14](#) does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA} , frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 25. ADC accuracy characteristics

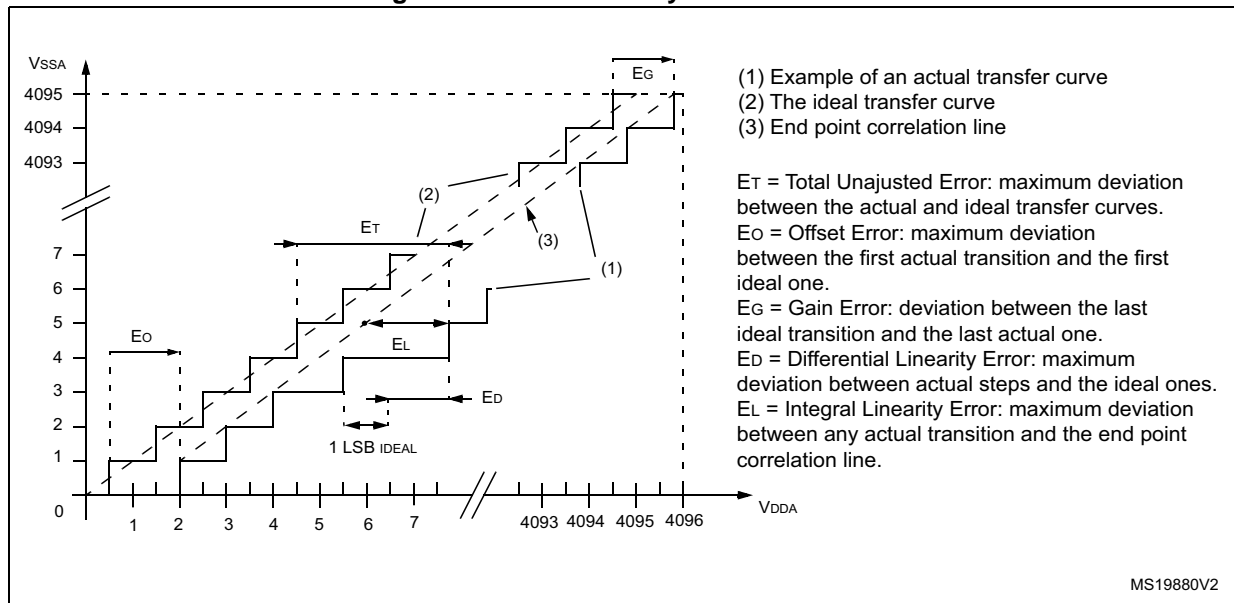
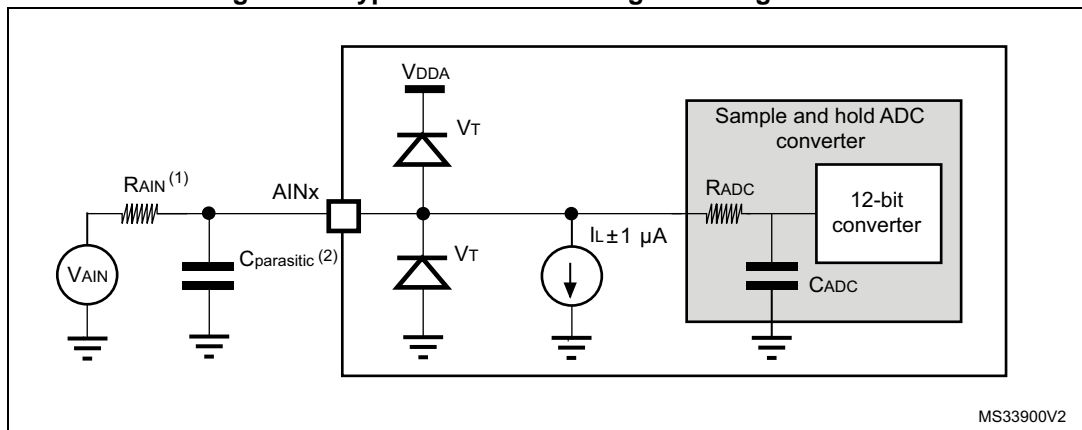


Figure 26. Typical connection diagram using the ADC



1. Refer to [Table 57: ADC characteristics](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

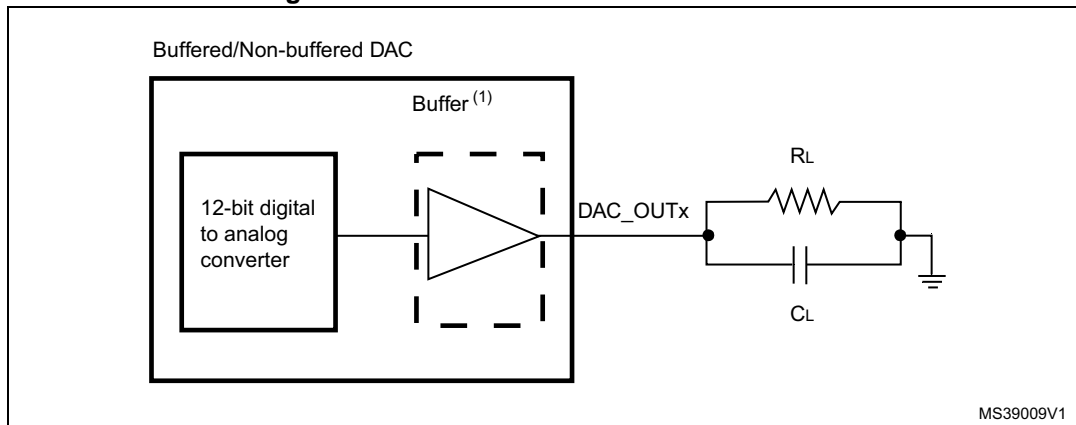
Power supply decoupling should be performed as shown in [Figure 12: Power supply scheme](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 60. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Gain error ⁽³⁾	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{\text{SETTLING}}^{(3)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB)	-	3	4	µs	$C_{\text{LOAD}} \leq 50 \text{ pF}$, $R_{\text{LOAD}} \geq 5 \text{ k}\Omega$
Update rate ⁽³⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{\text{LOAD}} \leq 50 \text{ pF}$, $R_{\text{LOAD}} \geq 5 \text{ k}\Omega$
$t_{\text{WAKEUP}}^{(3)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{\text{LOAD}} \leq 50 \text{ pF}$, $R_{\text{LOAD}} \geq 5 \text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ ⁽¹⁾	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-67	-40	dB	No R_{LOAD} , $C_{\text{LOAD}} = 50 \text{ pF}$

1. Guaranteed by design, not tested in production.
2. The DAC is in “quiescent mode” when it keeps the value steady on the output so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 27. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.19 Temperature sensor characteristics

Table 62. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
V_{30}	Voltage at 30 $^{\circ}\text{C}$ (± 5 $^{\circ}\text{C}$) ⁽²⁾	1.34	1.43	1.52	V
$t_{START}^{(1)}$	ADC_IN16 buffer startup time	-	-	10	μs
$t_{S_temp}^{(1)}$	ADC sampling time when reading the temperature	4	-	-	μs

1. Guaranteed by design, not tested in production.
2. Measured at $V_{DDA} = 3.3 \text{ V} \pm 10 \text{ mV}$. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to [Table 3: Temperature sensor calibration values](#).

6.3.20 V_{BAT} monitoring characteristics

Table 63. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	k Ω
Q	Ratio on V_{BAT} measurement	-	2	-	-
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$t_{S_vbat}^{(1)}$	ADC sampling time when reading the V_{BAT}	4	-	-	μs

1. Guaranteed by design, not tested in production.

6.3.21 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to [Section 6.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 64. TIMx characteristics

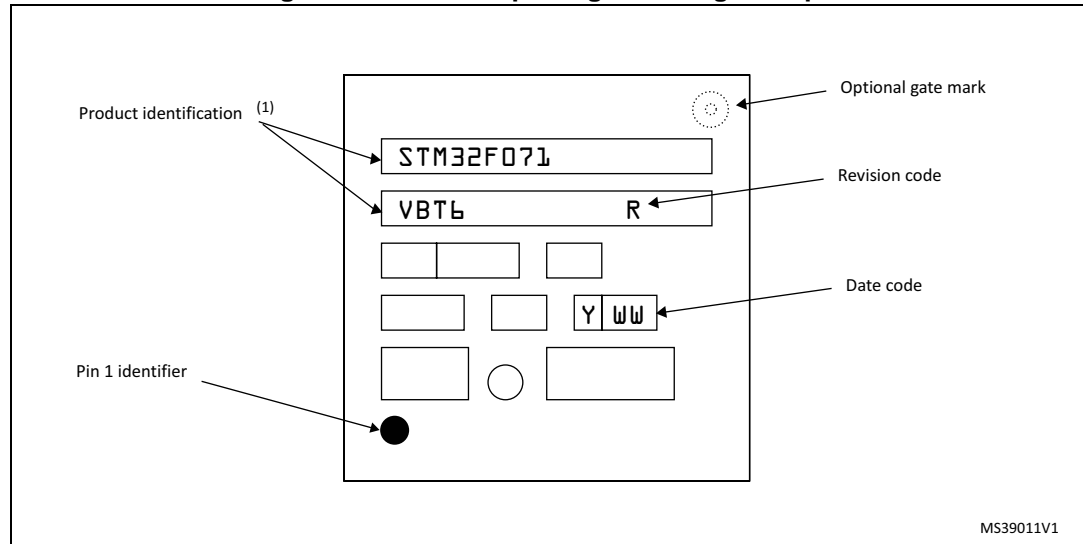
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	1365	-	μs
	32-bit counter maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	89.48	-	s

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 39. LQFP100 package marking example

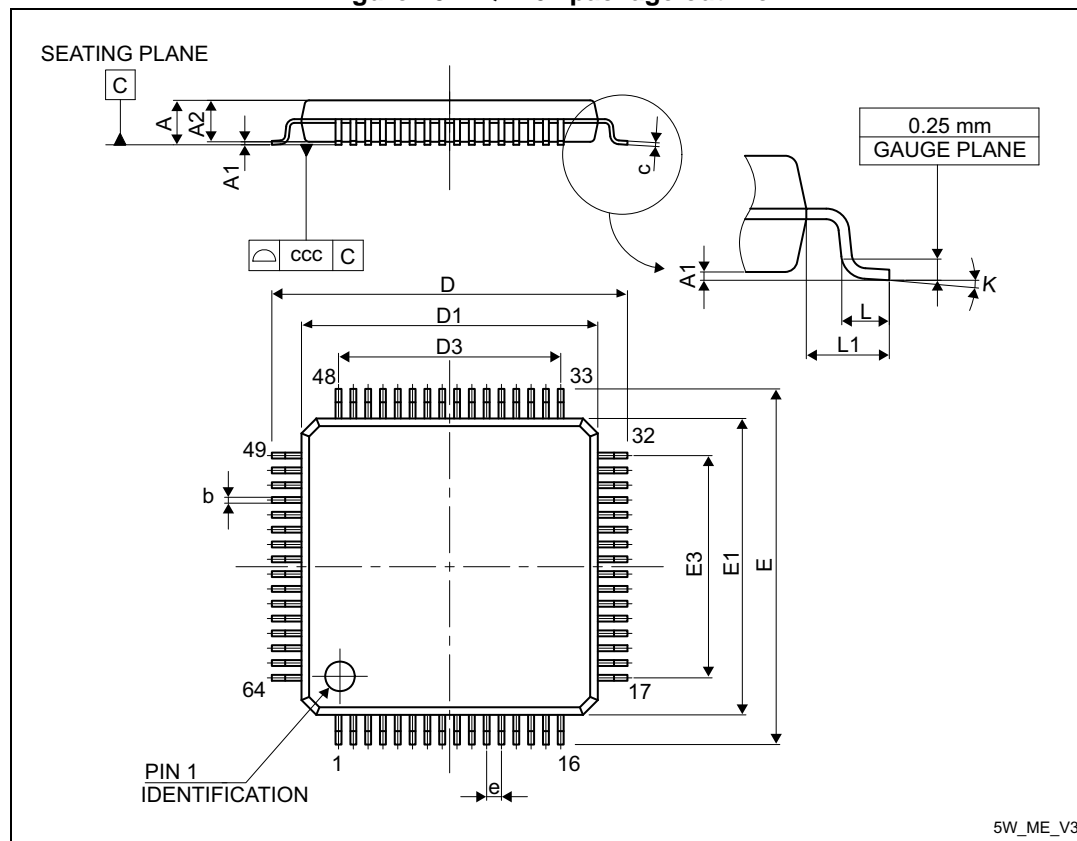


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 40. LQFP64 package outline



1. Drawing is not to scale.

Table 73. LQFP64 package mechanical data

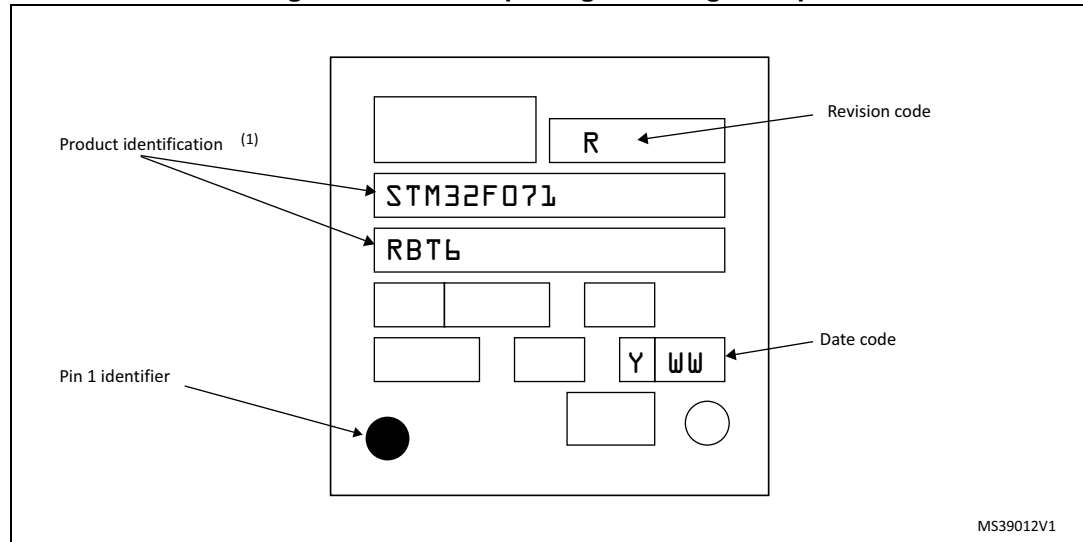
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LQFP64 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

9 Revision history

Table 79. Document revision history

Date	Revision	Changes
13-Jan-2014	1	Initial draft
21-Feb-2014	2	<p>Added part number STM32F071V8.</p> <p>Changed status of document from "Preliminary data" to "Production data".</p> <p>Updated "Reset and power management" data in <i>Features</i>.</p> <p>Updated $t_{S_vrefint}$ in <i>Table: Embedded internal reference voltage</i>.</p> <p>Updated V_{HSEH} and V_{HSEL} in <i>Table: High-speed external user clock characteristics</i>.</p> <p>Updated V_{LSEH} and V_{LSEL} in <i>Table: Low-speed external user clock characteristics</i>.</p> <p>Updated t_{S_temp} in <i>Table: TS characteristics</i>.</p> <p>Updated t_{S_vbat} in <i>Table: VBAT monitoring characteristics</i>.</p> <p>Updated <i>Section: I²C interface characteristics</i>.</p> <p>Updated <i>Figure: UFBGA100 package top view</i> and <i>Figure: WLCSP49 package top view</i>.</p> <p>Modified value of t_{s_sc} and removed row V_{BG} in <i>Table: Comparator characteristics</i>.</p>
17-Dec-2015	3	<p>Cover page:</p> <ul style="list-style-type: none"> part numbers moved to title and table of part numbers removed generic product name in the whole document changed to STM32F071x8/xB <p>Section 2: Description:</p> <ul style="list-style-type: none"> <i>Figure 1: Block diagram</i> updated <p>Section 3: Functional overview:</p> <ul style="list-style-type: none"> <i>Figure 2: Clock tree</i> updated <i>Section 3.5.4: Low-power modes</i> - added USART2 to comm. peripherals configurable to operate with HSI <p>Section 4: Pinouts and pin descriptions:</p> <ul style="list-style-type: none"> Package pinout figures updated (look and feel) <i>Figure 8: WLCSP49 package pinout</i> - now presented in top view <i>Figure 3: UFBGA100 package pinout</i> - names of PC14, PC15, PF0, PF1 complemented <i>Table 13: STM32F071x8/xB pin definitions</i> - pin types corrected for PF0 and PF1 <p>Section 5: Memory mapping:</p> <ul style="list-style-type: none"> <i>Figure 9</i>: added information on STM32F071V8 difference versus STM32F071xB map