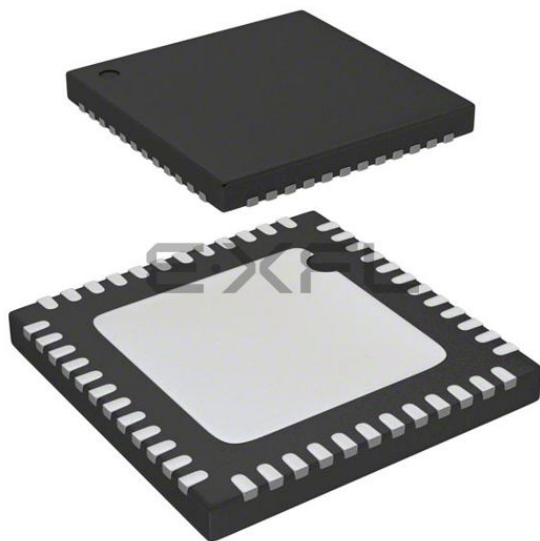




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f071cbu6

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Figure 4. LQFP100 package pinout

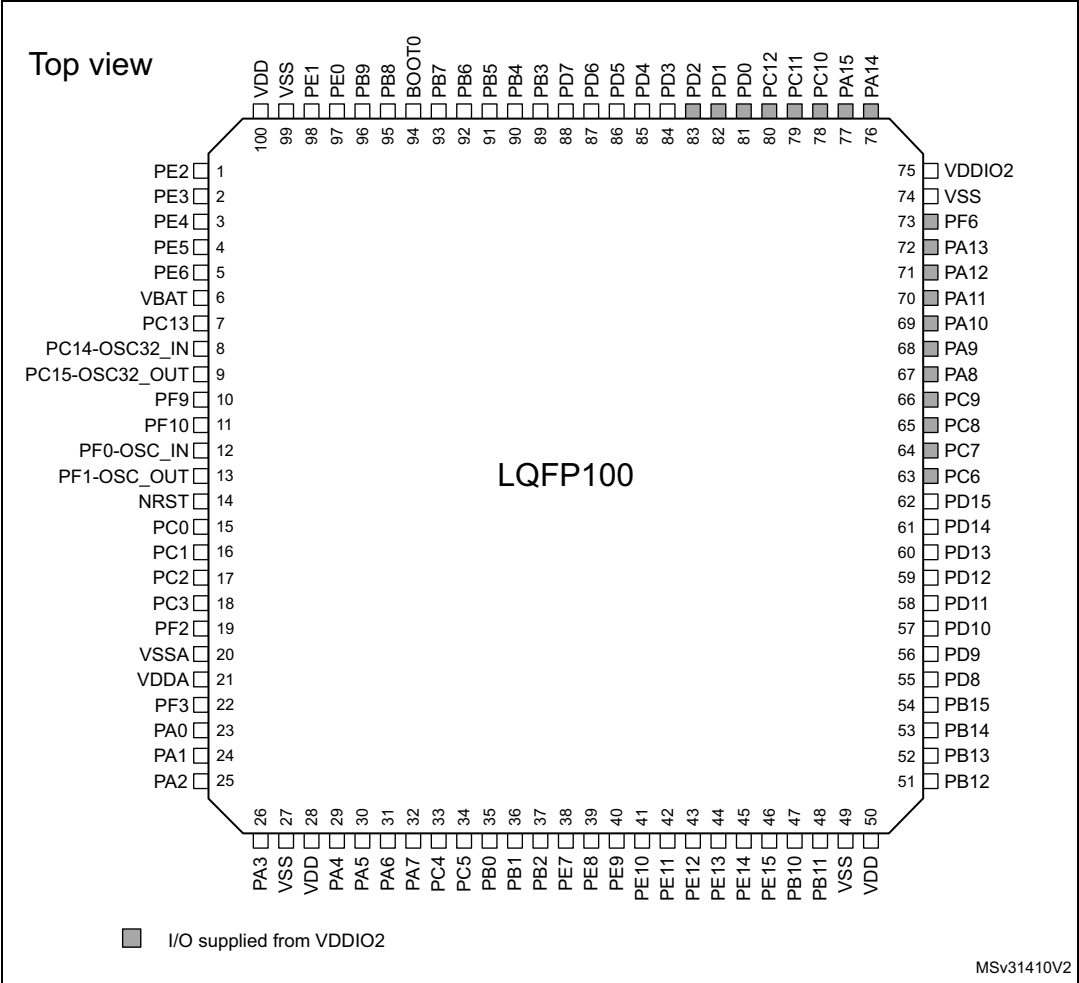


Table 13. STM32F071x8/xB pin definitions (continued)

Pin numbers					Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UQFPN48	WLCSP49					Alternate functions	Additional functions
M7	38	-	-	-	PE7	I/O	FT	-	TIM1_ETR	-
L7	39	-	-	-	PE8	I/O	FT	-	TIM1_CH1N	-
M8	40	-	-	-	PE9	I/O	FT	-	TIM1_CH1	-
L8	41	-	-	-	PE10	I/O	FT	-	TIM1_CH2N	-
M9	42	-	-	-	PE11	I/O	FT	-	TIM1_CH2	-
L9	43	-	-	-	PE12	I/O	FT	-	SPI1_NSS, I2S1_WS, TIM1_CH3N	-
M10	44	-	-	-	PE13	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM1_CH3	-
M11	45	-	-	-	PE14	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM1_CH4	-
M12	46	-	-	-	PE15	I/O	FT	-	SPI1_MOSI, I2S1_SD, TIM1_BKIN	-
L10	47	29	21	E3	PB10	I/O	FT	-	SPI2_SCK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	-
L11	48	30	22	G2	PB11	I/O	FT	-	USART3_RX, TIM2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA	-
F12	49	31	23	D3	VSS	S	-	-	Ground	
G12	50	32	24	F2	VDD	S	-	-	Digital power supply	
L12	51	33	25	E2	PB12	I/O	FT	-	TIM1_BKIN, TIM15_BKIN, SPI2_NSS, I2S2_WS, USART3_CK, TSC_G6_IO2, EVENTOUT	-
K12	52	34	26	G1	PB13	I/O	FTf	-	SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_CTS, TIM1_CH1N, TSC_G6_IO3	-
K11	53	35	27	F1	PB14	I/O	FTf	-	SPI2_MISO, I2S2_MCK, I2C2_SDA, USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-



Table 15. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	USART3_CK	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	USART3_RTS	-
PB2	-	-	-	TSC_G3_IO4	-	-
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1	-	-
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2	-	TIM17_BKIN
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	USART4_CTS	-
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC		-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT		SPI2_NSS, I2S2_WS
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK, I2S2_CK
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1	USART3_RX	-
PB12	SPI2_NSS, I2S2_WS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2	USART3_CK	TIM15_BKIN
PB13	SPI2_SCK, I2S2_CK	-	TIM1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL
PB14	SPI2_MISO, I2S2_MCK	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA
PB15	SPI2_MOSI, I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	-
PE8	TIM1_CH1N	-
PE9	TIM1_CH1	-
PE10	TIM1_CH2N	-
PE11	TIM1_CH2	-
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 19. Alternate functions available on port F

Pin name	AF
PF0	CRS_SYNC
PF1	-
PF2	EVENTOUT
PF3	EVENTOUT
PF6	-
PF9	TIM15_CH1
PF10	TIM15_CH2

Table 20. STM32F071x8/xB peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 5C00 - 0x4000 6BFF	4 KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in [Table 31](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 29. Typical and maximum current consumption from V_{DD} supply at $V_{DD} = 3.6$ V

Symbol	Parameter	Conditions	f _{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T _A ⁽¹⁾			Typ	Max @ T _A ⁽¹⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DD}	Supply current in Run mode, code executing from Flash memory	HSI48	48 MHz	24.3	26.9	27.2	27.9	13.1	14.8	14.9	15.5	mA
		HSE bypass, PLL on	48 MHz	24.1	26.8	27.0	27.7	13.0	14.6	14.8	15.4	
			32 MHz	16.0	18.3	18.6	19.2	8.76	9.56	9.73	10.6	
			24 MHz	12.3	13.7	14.3	14.7	7.36	7.94	8.37	8.81	
		HSE bypass, PLL off	8 MHz	4.52	5.25	5.28	5.61	2.89	3.17	3.26	3.34	
			1 MHz	1.25	1.39	1.58	1.87	0.93	1.06	1.15	1.34	
		HSI clock, PLL on	48 MHz	24.1	27.1	27.6	27.8	12.9	14.7	14.9	15.5	
			32 MHz	16.1	18.2	18.9	19.3	8.82	9.69	9.83	10.7	
			24 MHz	12.4	14.0	14.4	14.8	7.31	7.92	8.34	8.75	
		HSI clock, PLL off	8 MHz	4.52	5.25	5.35	5.61	2.87	3.16	3.25	3.33	

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 35: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 34. Switching output I/O current consumption

Symbol	Parameter	Conditions ⁽¹⁾	I/O toggling frequency (f _{SW})	Typ	Unit
I _{sw}	I/O current consumption	V _{DDIOx} = 3.3 V C = C _{INT}	4 MHz	0.07	mA
			8 MHz	0.15	
			16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
		V _{DDIOx} = 3.3 V C _{EXT} = 0 pF C = C _{INT} + C _{EXT} + C _S	4 MHz	0.18	
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V _{DDIOx} = 3.3 V C _{EXT} = 10 pF C = C _{INT} + C _{EXT} + C _S	4 MHz	0.32	
			8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
			48 MHz	4.442	
		V _{DDIOx} = 3.3 V C _{EXT} = 22 pF C = C _{INT} + C _{EXT} + C _S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V _{DDIOx} = 3.3 V C _{EXT} = 33 pF C = C _{INT} + C _{EXT} + C _S	4 MHz	0.64	
			8 MHz	1.25	
			16 MHz	3.24	
			24 MHz	5.02	
		V _{DDIOx} = 3.3 V C _{EXT} = 47 pF C = C _{INT} + C _{EXT} + C _S C = C _{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	
		V _{DDIOx} = 2.4 V C _{EXT} = 47 pF C = C _{INT} + C _{EXT} + C _S C = C _{int}	4 MHz	0.66	
			8 MHz	1.43	
			16 MHz	2.45	
			24 MHz	4.97	

1. C_S = 7 pF (estimated value).

6.3.6 Wakeup time from low-power mode

The wakeup times given in [Table 36](#) are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop or Standby mode, SYSCCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V _{DD} = V _{DDA}					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t _{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	3.2	3.1	2.9	2.9	2.8	5	μs
		Regulator in low power mode	7.0	5.8	5.2	4.9	4.6	9	
t _{WUSTANDBY}	Wakeup from Standby mode	-	60.4	55.6	53.5	52	51	-	
t _{WUSLEEP}	Wakeup from Sleep mode	-	4 SYSCCLK cycles					-	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 14: High-speed external clock source AC timing diagram](#).

Table 37. High-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Min	Typ	Max	Unit
f _{HSE_ext}	User external clock source frequency	-	8	32	MHz
V _{HSEH}	OSC_IN input pin high level voltage	0.7 V _{DDIOx}	-	V _{DDIOx}	V
V _{HSEL}	OSC_IN input pin low level voltage	V _{SS}	-	0.3 V _{DDIOx}	
t _{w(HSEH)} t _{w(HSEL)}	OSC_IN high or low time	15	-	-	ns
t _{r(HSE)} t _{f(HSE)}	OSC_IN rise or fall time	-	-	20	

Low-speed internal (LSI) RC oscillator

Table 44. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}^{(2)}$	LSI oscillator startup time	-	-	85	μ s
$I_{DDA(LSI)}^{(2)}$	LSI oscillator power consumption	-	0.75	1.2	μ A

1. $V_{DDA} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in [Table 45](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 45. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock ⁽¹⁾	1 ⁽²⁾	8.0	24 ⁽²⁾	MHz
	PLL input clock duty cycle	40 ⁽²⁾	-	60 ⁽²⁾	%
f_{PLL_OUT}	PLL multiplier output clock	16 ⁽²⁾	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200 ⁽²⁾	μ s
Jitter _{PLL}	Cycle-to-cycle jitter	-	-	300 ⁽²⁾	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT} .

2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 46. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
t_{prog}	16-bit programming time	$T_A = -40$ to $+105$ °C	40	53.5	60	μ s
t_{ERASE}	Page (2 KB) erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
t_{ME}	Mass erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

6.3.19 Temperature sensor characteristics

Table 62. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
V_{30}	Voltage at 30 $^{\circ}\text{C}$ (± 5 $^{\circ}\text{C}$) ⁽²⁾	1.34	1.43	1.52	V
$t_{START}^{(1)}$	ADC_IN16 buffer startup time	-	-	10	μs
$t_{S_temp}^{(1)}$	ADC sampling time when reading the temperature	4	-	-	μs

1. Guaranteed by design, not tested in production.
2. Measured at $V_{DDA} = 3.3 \text{ V} \pm 10 \text{ mV}$. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to [Table 3: Temperature sensor calibration values](#).

6.3.20 V_{BAT} monitoring characteristics

Table 63. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	k Ω
Q	Ratio on V_{BAT} measurement	-	2	-	-
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$t_{S_vbat}^{(1)}$	ADC sampling time when reading the V_{BAT}	4	-	-	μs

1. Guaranteed by design, not tested in production.

6.3.21 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to [Section 6.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 64. TIMx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	1365	-	μs
	32-bit counter maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	89.48	-	s

Table 70. UFBGA100 package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. Recommended footprint for UFBGA100 package

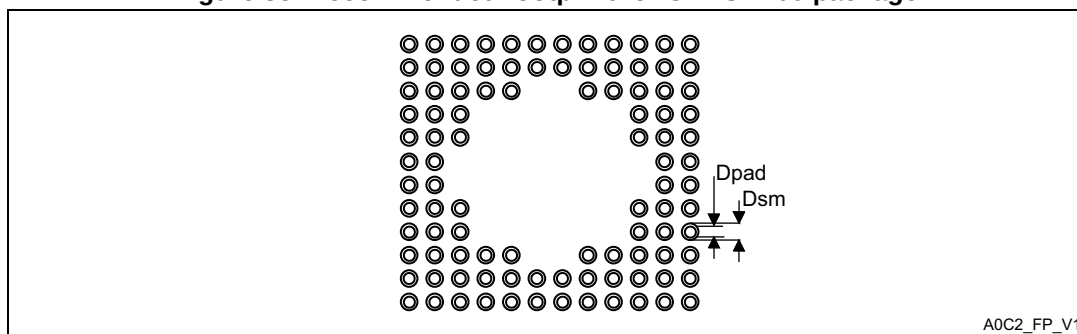


Table 71. UFBGA100 recommended PCB design rules

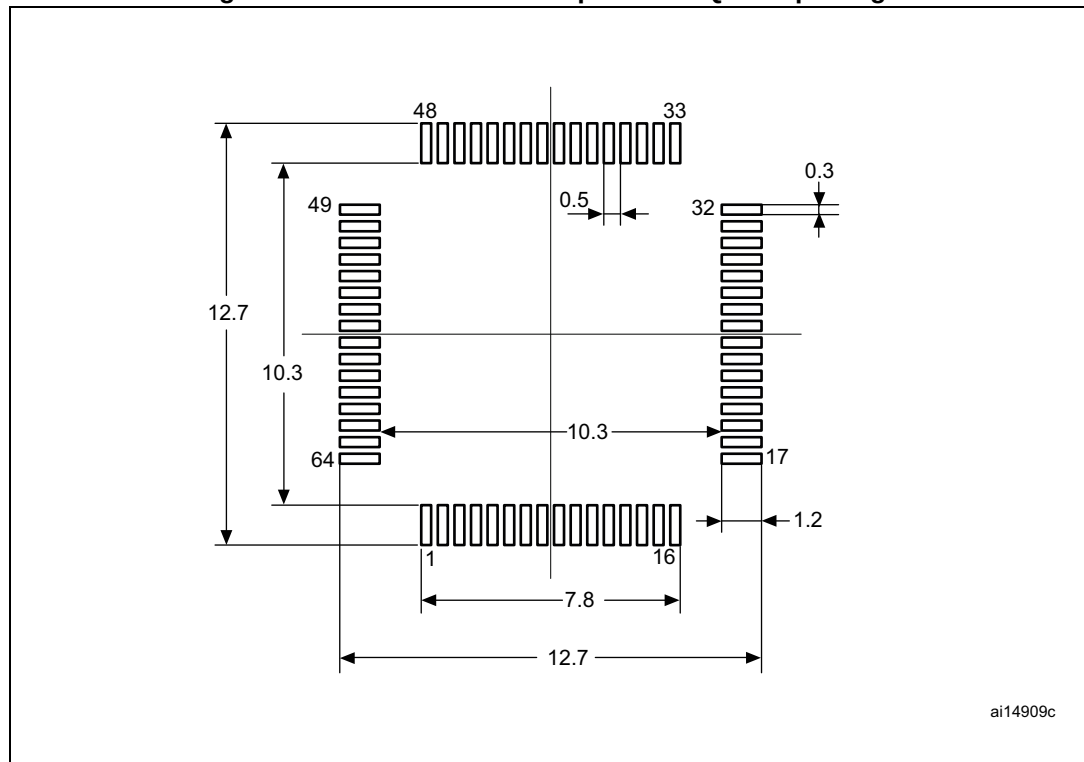
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Table 73. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. Recommended footprint for LQFP64 package



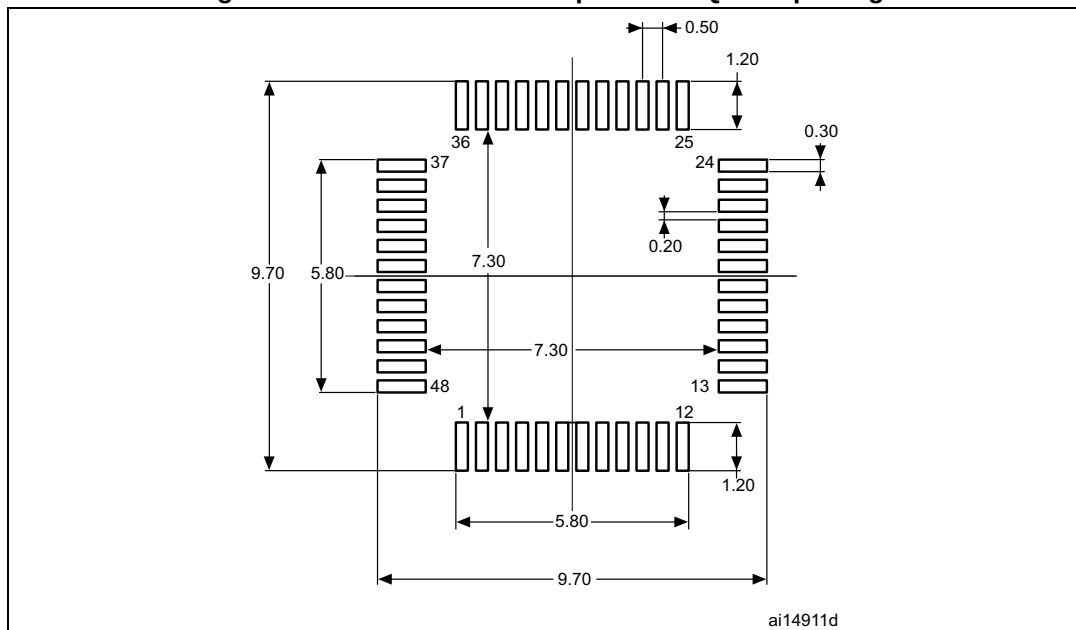
1. Dimensions are expressed in millimeters.

Table 75. LQFP48 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. Recommended footprint for LQFP48 package

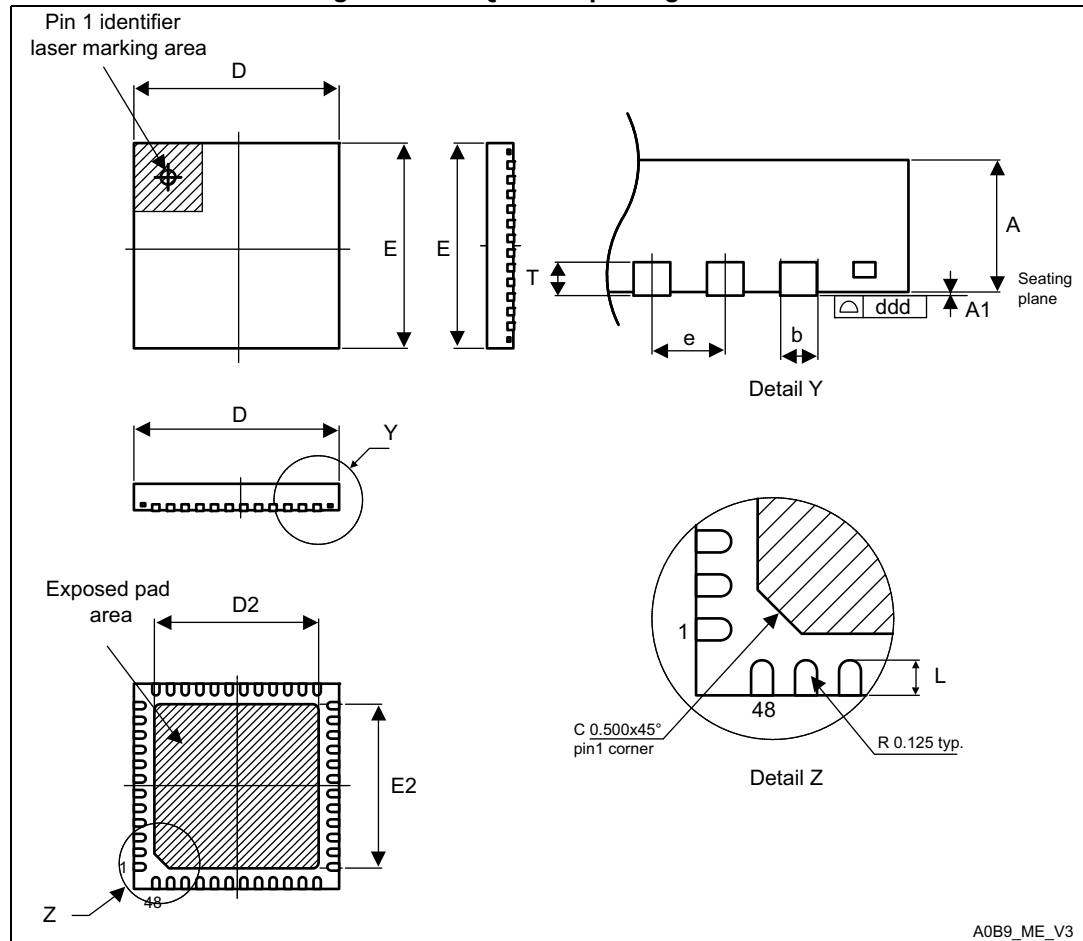


1. Dimensions are expressed in millimeters.

7.6 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 48. UFQFPN48 package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

7.7 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 24: General operating conditions](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 77. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	49	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Ordering information](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

9 Revision history

Table 79. Document revision history

Date	Revision	Changes
13-Jan-2014	1	Initial draft
21-Feb-2014	2	Added part number STM32F071V8. Changed status of document from “Preliminary data” to “Production data”. Updated “Reset and power management” data in <i>Features</i>. Updated $t_{S_vrefint}$ in <i>Table: Embedded internal reference voltage</i>. Updated V_{HSEH} and V_{HSEL} in <i>Table: High-speed external user clock characteristics</i>. Updated V_{LSEH} and V_{LSEL} in <i>Table: Low-speed external user clock characteristics</i>. Updated t_{S_temp} in <i>Table: TS characteristics</i>. Updated t_{S_vbat} in <i>Table: VBAT monitoring characteristics</i>. Updated <i>Section: I²C interface characteristics</i>. Updated <i>Figure: UFBGA100 package top view</i> and <i>Figure: WLCSP49 package top view</i>. Modified value of t_{s_sc} and removed row V_{BG} in <i>Table: Comparator characteristics</i>.
17-Dec-2015	3	Cover page: – part numbers moved to title and table of part numbers removed – generic product name in the whole document changed to STM32F071x8/xB Section 2: Description: – <i>Figure 1: Block diagram</i> updated Section 3: Functional overview: – <i>Figure 2: Clock tree</i> updated – <i>Section 3.5.4: Low-power modes</i> - added USART2 to comm. peripherals configurable to operate with HSI Section 4: Pinouts and pin descriptions: – Package pinout figures updated (look and feel) – <i>Figure 8: WLCSP49 package pinout</i> - now presented in top view – <i>Figure 3: UFBGA100 package pinout</i> - names of PC14, PC15, PF0, PF1 complemented – <i>Table 13: STM32F071x8/xB pin definitions</i> - pin types corrected for PF0 and PF1 Section 5: Memory mapping: – <i>Figure 9</i>: added information on STM32F071V8 difference versus STM32F071xB map

Table 79. Document revision history (continued)

Date	Revision	Changes
15-Sep-2016	5	Section 6: Electrical characteristics: – <i>Figure 29: SPI timing diagram - slave mode and CPHA = 0</i> and <i>Figure 30: SPI timing diagram - slave mode and CPHA = 1</i> updated - modified NSS timing waveforms (among other changes)
10-Jan-2017	6	Section 6: Electrical characteristics: – <i>Table 40: LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)</i> - information on configuring different drive capabilities removed. See the corresponding reference manual. – <i>Table 28: Embedded internal reference voltage</i> - V_{REFINT} values – <i>Table 60: DAC characteristics</i> - min. R_{LOAD} to V_{DDA} defined – <i>Figure 29: SPI timing diagram - slave mode and CPHA = 0</i> and <i>Figure 30: SPI timing diagram - slave mode and CPHA = 1</i> enhanced and corrected Section 8: Ordering information: – The name of the section changed from the previous “Part numbering”