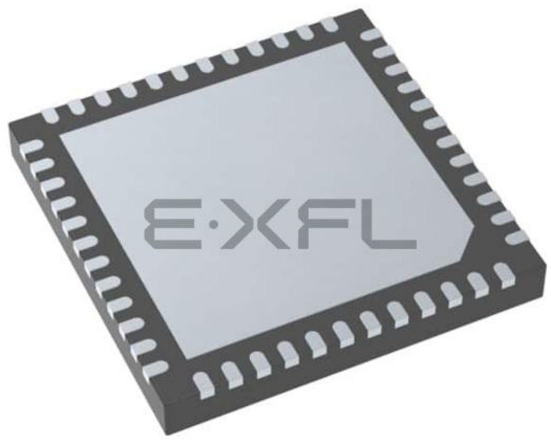

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f071cbu7tr

List of figures

Table 6. Number of capacitive sensing channels available on STM32F071x8/xB devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F071Vx	STM32F071Rx	STM32F071Cx
G1	3	3	3
G2	3	3	3
G3	3	3	2
G4	3	3	3
G5	3	3	3
G6	3	3	3
G7	3	0	0
G8	3	0	0
Number of capacitive sensing channels	24	18	17

3.14 Timers and watchdogs

The STM32F071x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

Table 7 compares the features of the different timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	integer from 1 to 65536	Yes	-	-

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.14.2 General-purpose timers (TIM2, 3, 14, 15, 16, 17)

There are six synchronizable general-purpose timers embedded in the STM32F071x8/xB devices (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F071x8/xB devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

Table 16. Alternate functions selected through GPIOC_AFR registers for port C

Pin name	AF0	AF1
PC0	EVENTOUT	-
PC1	EVENTOUT	-
PC2	EVENTOUT	SPI2_MISO, I2S2_MCK
PC3	EVENTOUT	SPI2_MOSI, I2S2_SD
PC4	EVENTOUT	USART3_TX
PC5	TSC_G3_IO1	USART3_RX
PC6	TIM3_CH1	-
PC7	TIM3_CH2	-
PC8	TIM3_CH3	-
PC9	TIM3_CH4	-
PC10	USART4_TX	USART3_TX
PC11	USART4_RX	USART3_RX
PC12	USART4_CK	USART3_CK
PC13	-	-
PC14	-	-
PC15	-	-

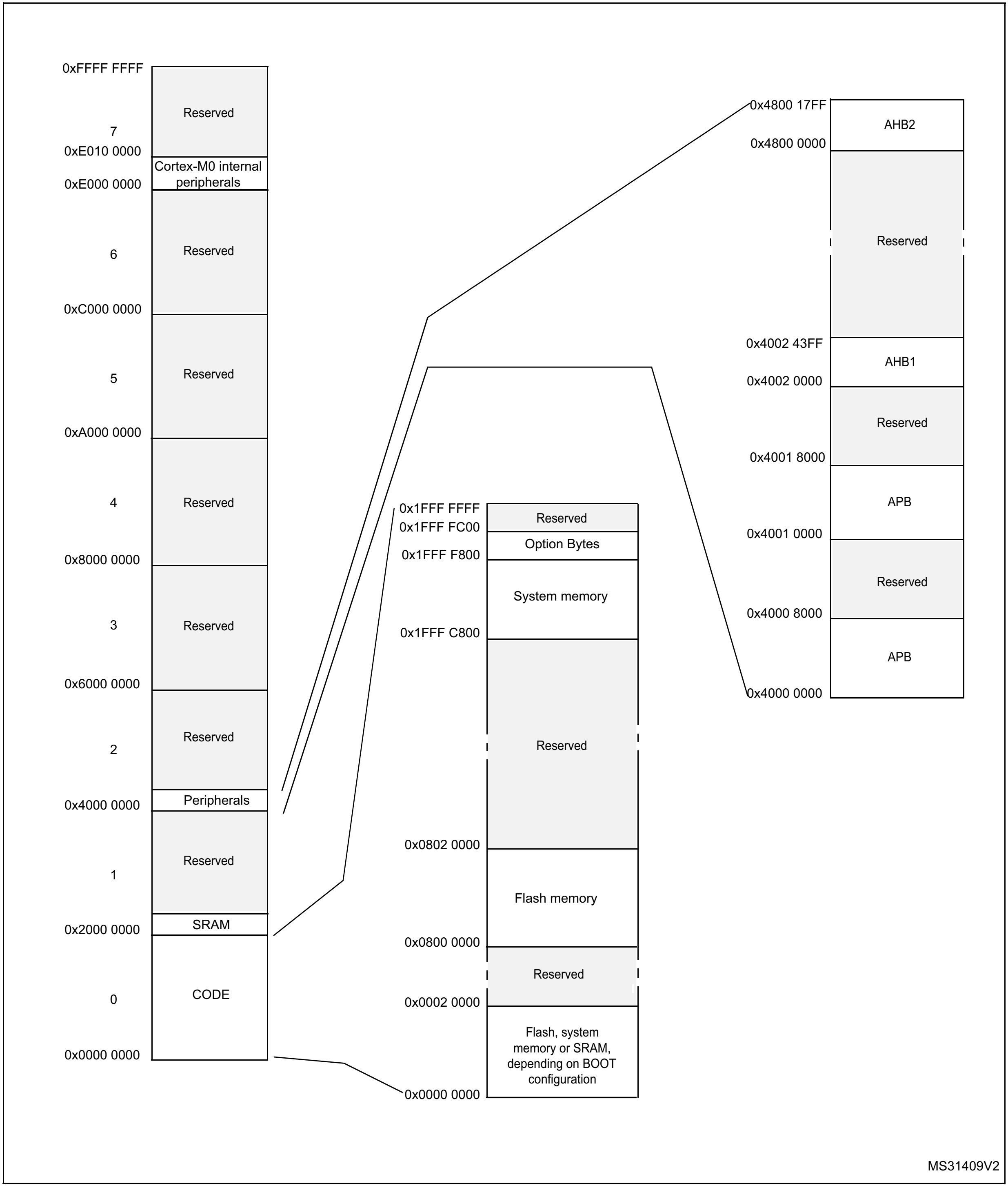
Table 17. Alternate functions selected through GPIOD_AFR registers for port D

Pin name	AF0	AF1
PD0	-	SPI2_NSS, I2S2_WS
PD1	-	SPI2_SCK, I2S2_CK
PD2	TIM3_ETR	USART3_RTS
PD3	USART2_CTS	SPI2_MISO, I2S2_MCK
PD4	USART2_RTS	SPI2_MOSI, I2S2_SD
PD5	USART2_TX	-
PD6	USART2_RX	-
PD7	USART2_CK	-
PD8	USART3_TX	-
PD9	USART3_RX	-
PD10	USART3_CK	-
PD11	USART3_CTS	-
PD12	USART3_RTS	TSC_G8_IO1
PD13	-	TSC_G8_IO2
PD14	-	TSC_G8_IO3
PD15	CRS_SYNC	TSC_G8_IO4

5 Memory mapping

To the difference of STM32F071xB memory map in *Figure 9*, the two bottom code memory spaces of STM32F071x8 end at 0x0000 FFFF and 0x0800 FFFF, respectively.

Figure 9. STM32F071xB memory map



6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme

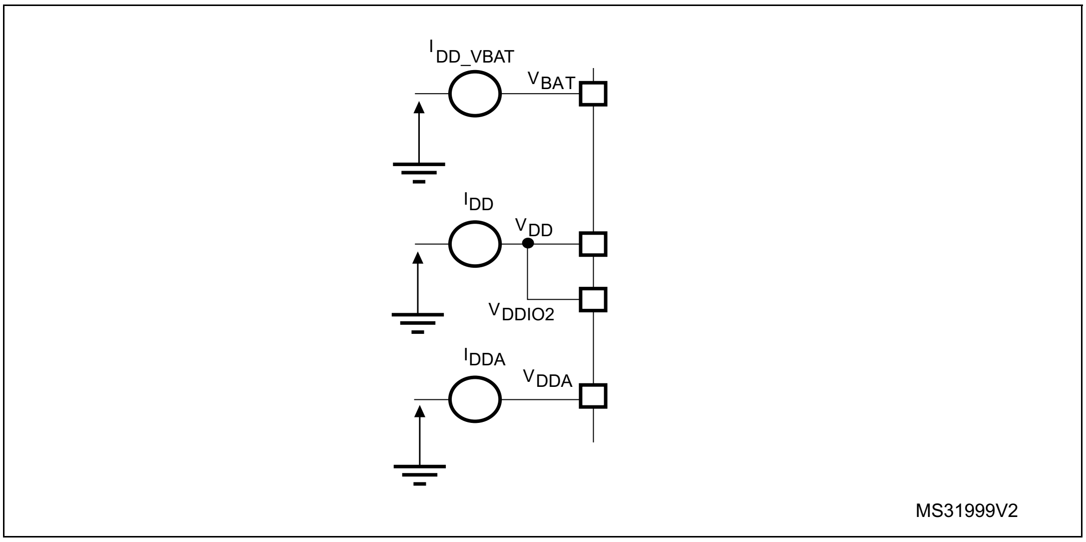


Table 22. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
	Total output current sourced by sum of all I/Os supplied by VDDIO2	-40	
$I_{INJ(PIN)}$(3)	Injected current on B, FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note (2) below *Table 59: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3.17 DAC electrical specifications

Table 60. DAC characteristics

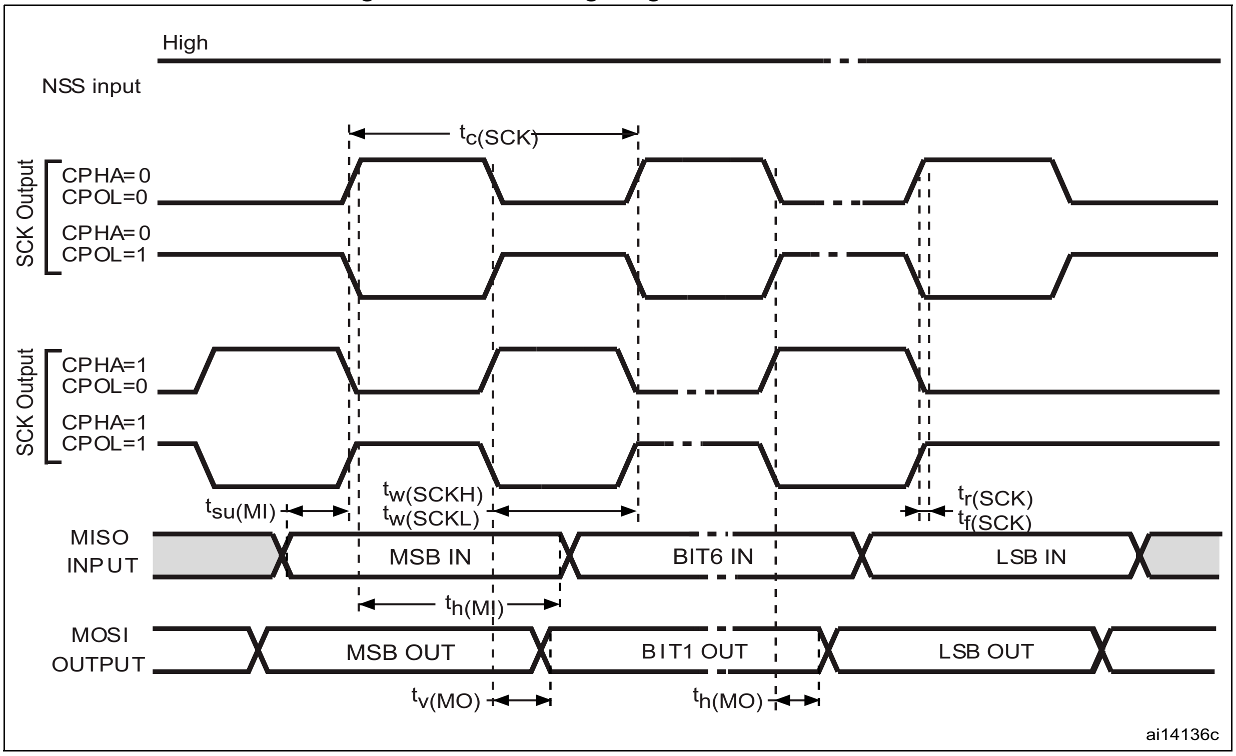
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	Load connected to V_{SSA}
		25	-	-	kΩ	Load connected to V_{DDA}
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{DDA} – 1LSB	V	
I_{DDA}(1)	DAC DC current consumption in quiescent mode(2)	-	-	600	µA	With no load, middle code (0x800) on the input
		-	-	700	µA	With no load, worst code (0xF1C) on the input
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	±10	mV	-
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{DDA} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{DDA} = 3.6 V

6.3.18 Comparator characteristics

Table 61. Comparator characteristics

Symbol	Parameter	Conditions		Min[1]	Typ	Max[1]	Unit
V_{DDA}	Analog supply voltage	-		V_{DD}	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	-
V_{SC}	V_{REFINT} scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1000 [2]	ms
		Next activations		-	-	0.2	
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Figure 31. SPI timing diagram - master mode

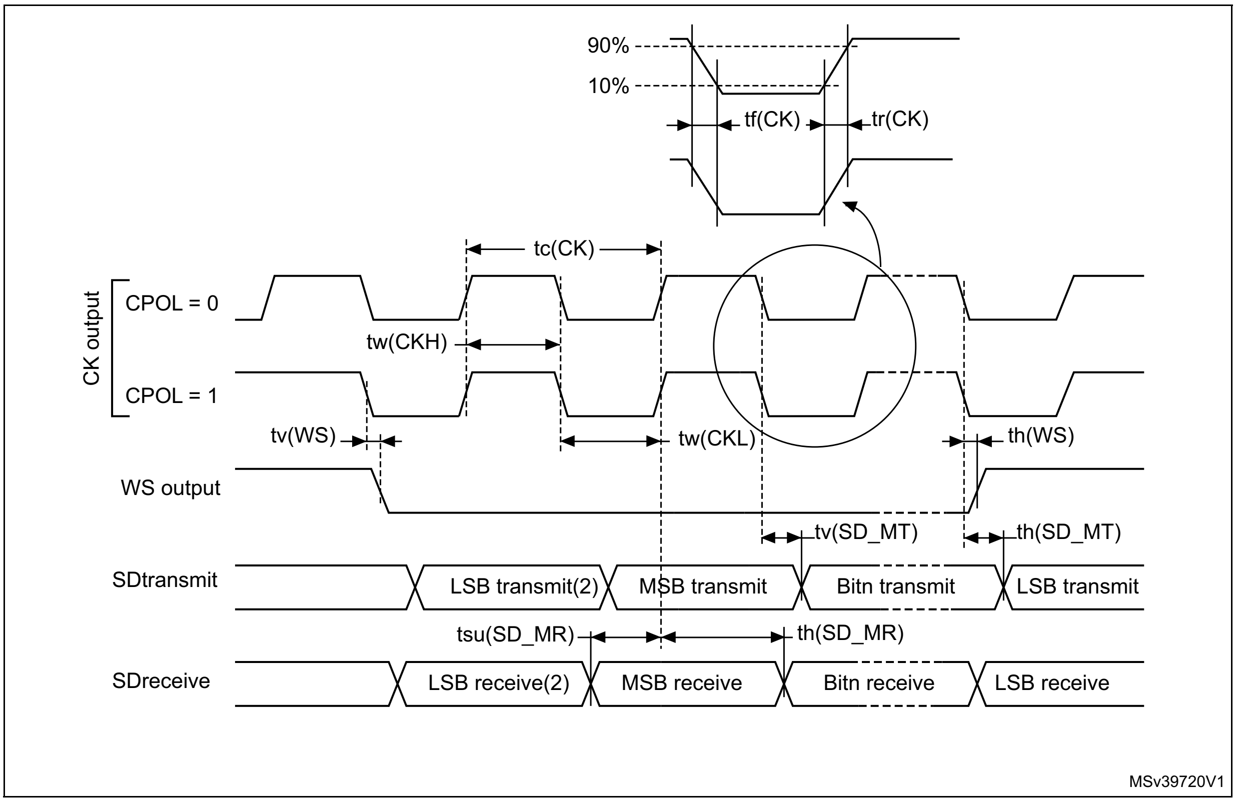


1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 69. I^2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I^2S clock rise time	Capacitive load C_L = 15 pF	-	10	ns
$t_{f(CK)}$	I^2S clock fall time		-	12	
$t_{w(CKH)}$	I^2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I^2S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I^2S slave input clock duty cycle	Slave mode	25	75	%

Figure 33. I²S master timing diagram (Philips protocol)



1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

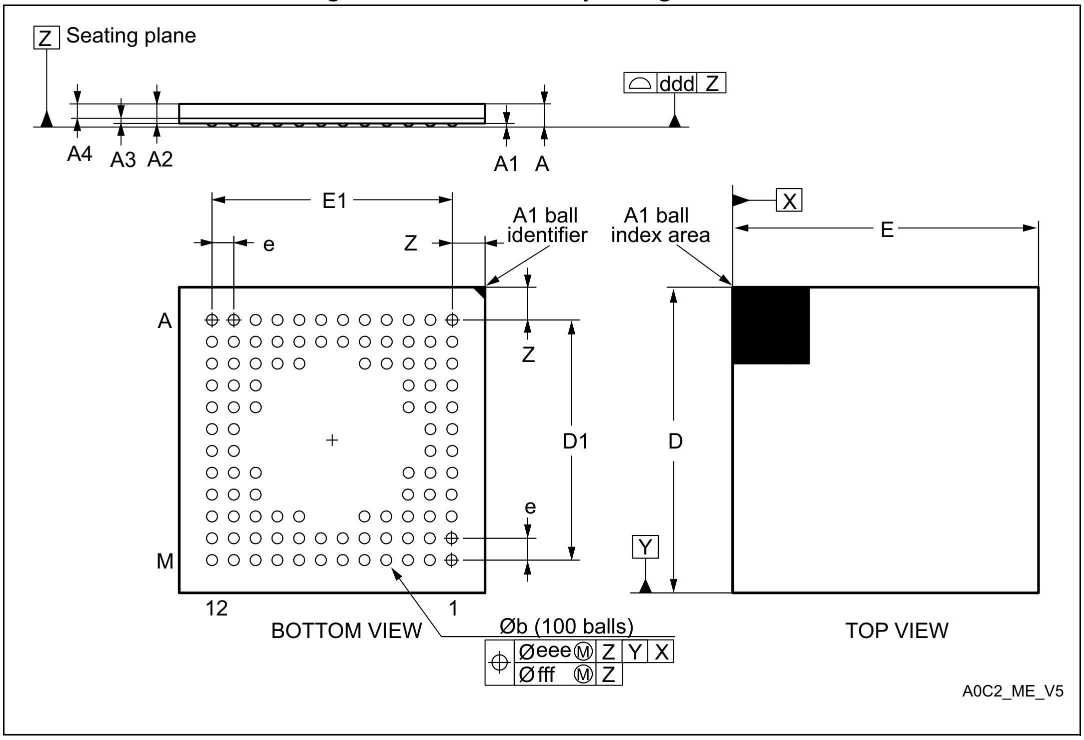
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra-fine-profile ball grid array package.

Figure 34. UFBGA100 package outline



1. Drawing is not to scale.

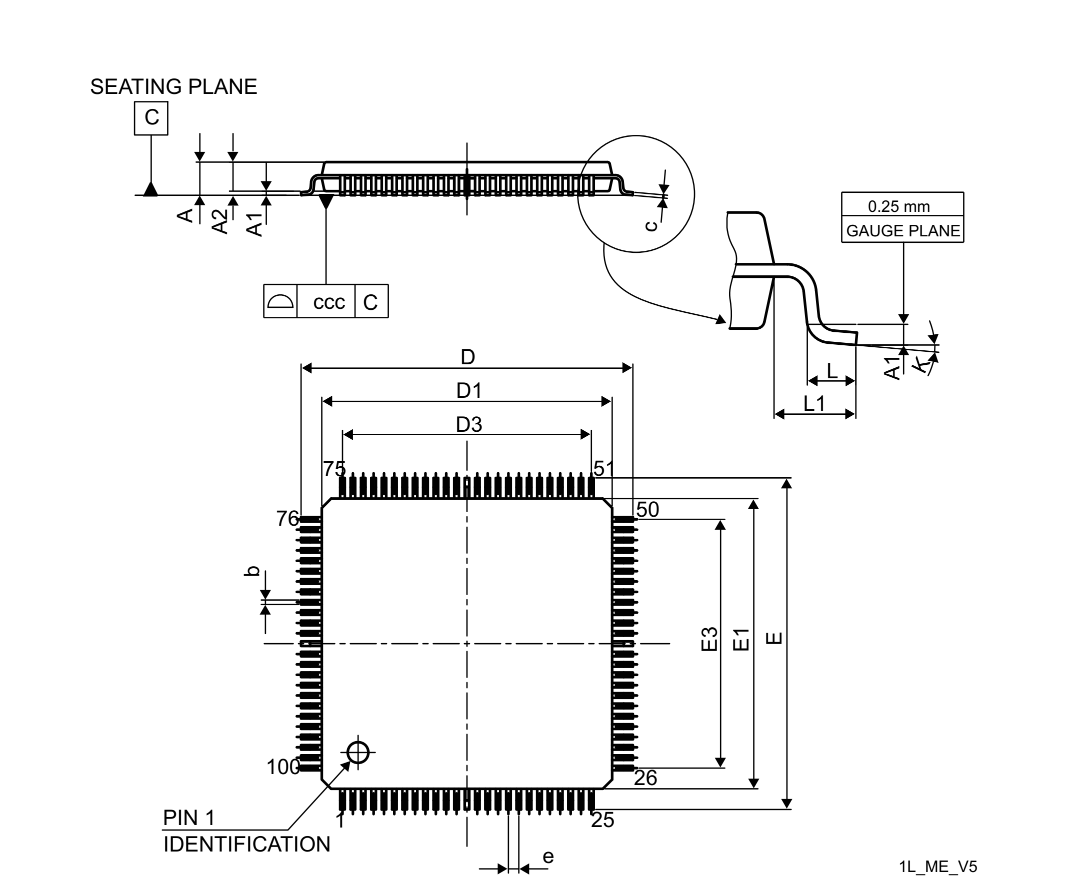
Table 70. UFBGA100 package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-

7.2 LQFP100 package information

LQFP100 is a100-pin, 14 x 14 mm low-profile quad flat package.

Figure 37. LQFP100 package outline



1. Drawing is not to scale.

Table 72. LQPF100 package mechanical data

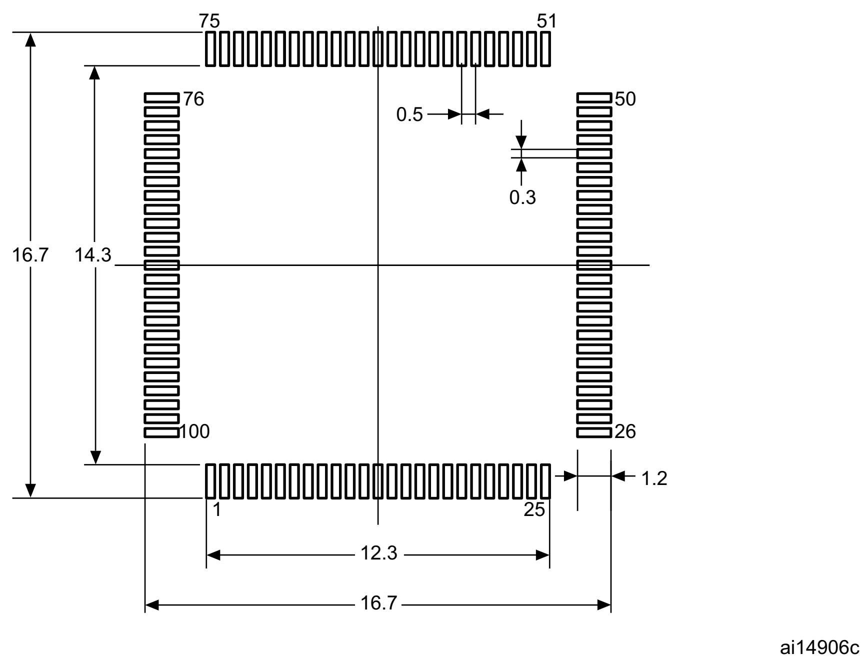
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 72. LQPF100 package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. Recommended footprint for LQFP100 package

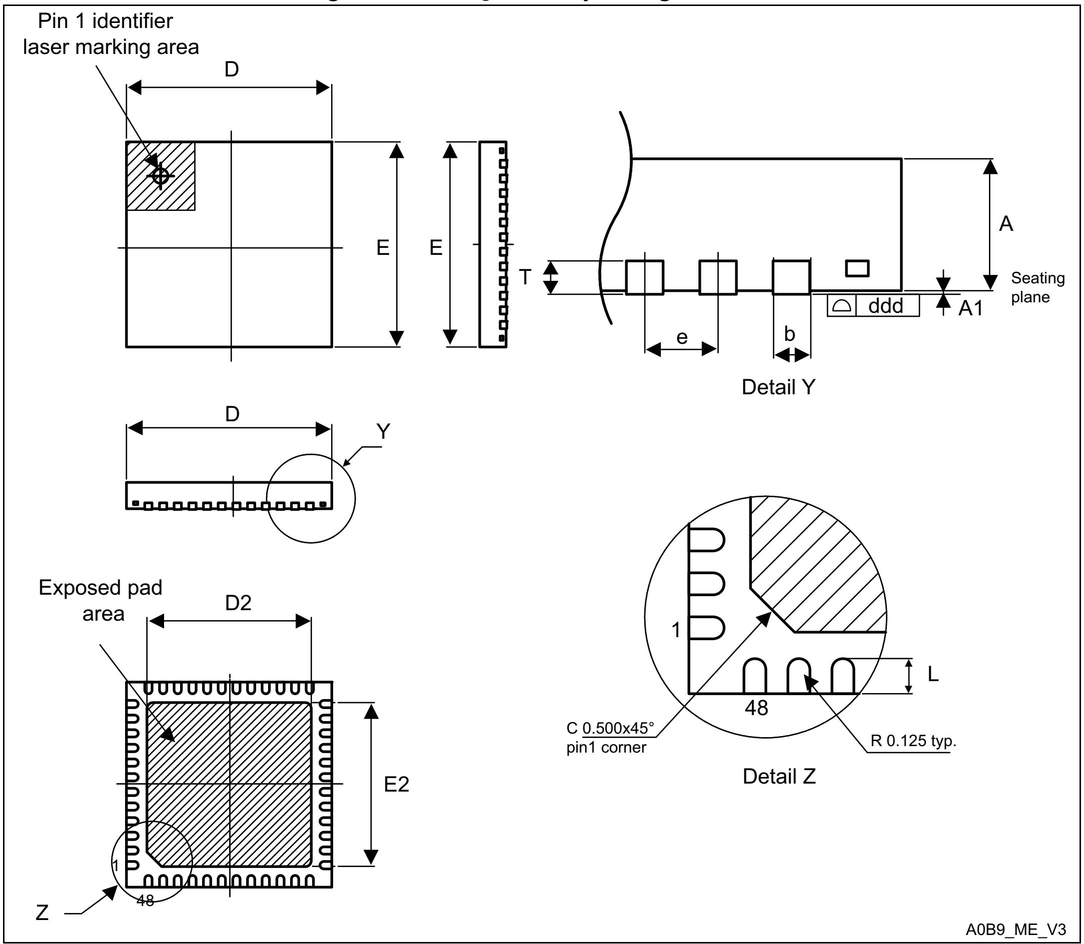


1. Dimensions are expressed in millimeters.

7.6 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 48. UFQFPN48 package outline



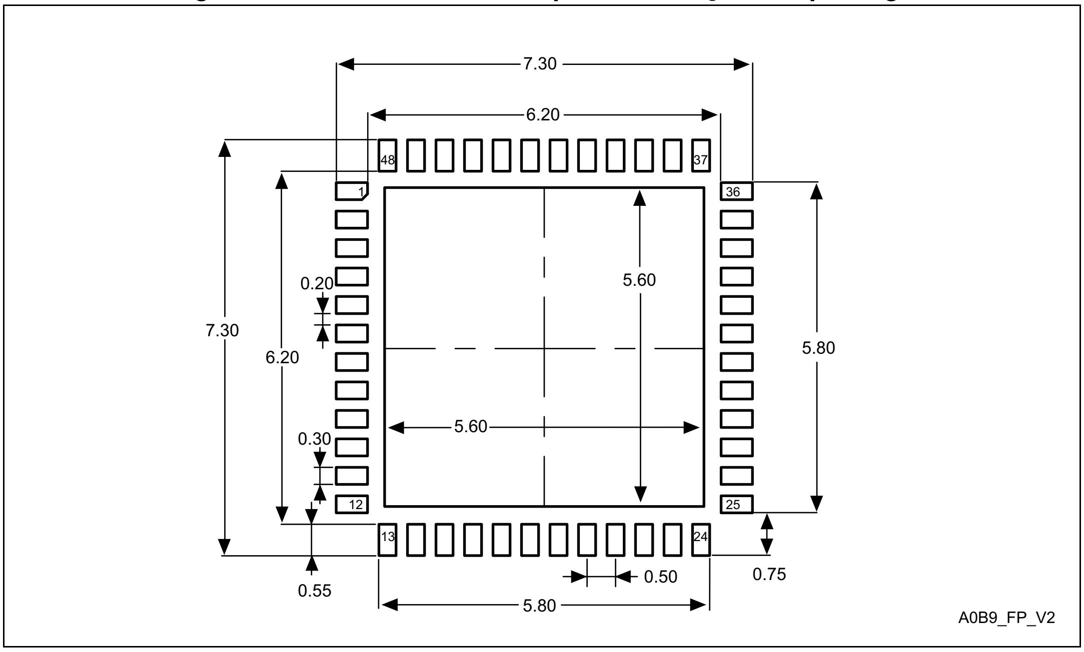
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 76. UFQFPN48 package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. Recommended footprint for UFQFPN48 package



1. Dimensions are expressed in millimeters.

7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 24: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 77. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	49	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

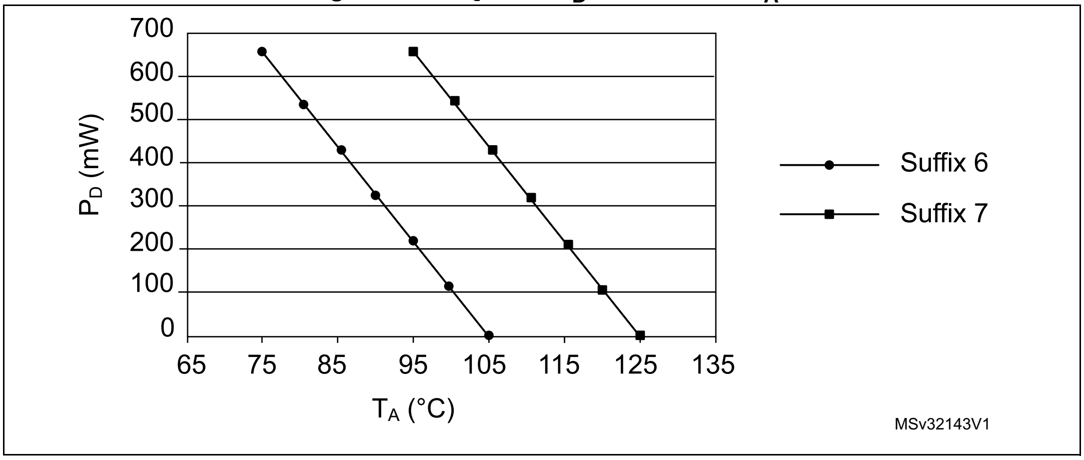
Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 51* to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.

Figure 51. LQFP64 P_D max versus T_A



8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 78. Ordering information scheme

Example: STM32 F 071 R B T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

071 = STM32F071xx

Pin count

C = 48/49 pins

R = 64 pins

V = 100 pins

User code memory size

8 = 64 Kbyte

B = 128 Kbyte

Package

H = UFBGA

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

6 = –40 to 85 °C

7 = –40 to 105 °C

Options

xxx = code ID of programmed parts (includes packing type)

TR = tape and reel packing

blank = tray packing

Table 79. Document revision history (continued)

Date	Revision	Changes
17-Dec-2015	3 (continued)	***Section 6: Electrical characteristics***: – *Table 21: Voltage characteristics* and *Table 22: Current characteristics* updated – *Table 24: General operating conditions* - added footnote for V_{IN} of TTa I/O – *Table 28: Embedded internal reference voltage*: added t_{START} parameter and removal of -40°-to-85° condition for V_{REFINT} and associated note – *Table 32: Typical and maximum current consumption from the V_{BAT} supply* - added max values – Merger of two tables into *Table 33: Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal* – *Table 35: Peripheral current consumption* - APB peripheral total current consumption corrected – *Table 40: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* - V_{DD} replaced with V_{DDIOx} – *Table 41: HSI oscillator characteristics* and *Figure 18: HSI oscillator accuracy characterization results for soldered parts* updated – *Table 42: HSI14 oscillator characteristics:* changed ACC_{HSI14} for 0-70° Ta range – *Table 46: Flash memory characteristics:* removed V_{prog} – *Table 49: EMI characteristics* updated – *Table 50: ESD absolute maximum ratings* updated – *Table 53: I/O static characteristics* - note removed – *Table 57: ADC characteristics* - updated some parameter values, test conditions and added footnotes (3) and (4) – *Table 60: DAC characteristics* - I_{DDA} max value (DAC DC current consumption) updated – *Table 61: Comparator characteristics* - min value added for V_{DDA} – *Figure 28: Maximum V_{REFINT} scaler startup time from power down* added – *Table 63: V_{BAT} monitoring characteristics:* changed the typical value for R parameter – *Table 69: I^2S characteristics*: table reorganized ***Section 7: Package information***: – information on packages generally updated ***Section 8: Ordering information***: – added tray packing to options
14-Jun-2016	4	Added STM32F071C8 part number ***Section 6: Electrical characteristics***: – V_{REFINT} values updated in *Table 28: Embedded internal reference voltage* – R_{LOAD} - added value for connection to V_{DD}