



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f071rbt6

List of figures

Figure 1.	Block diagram	12
Figure 2.	Clock tree	16
Figure 3.	UFBGA100 package pinout	28
Figure 4.	LQFP100 package pinout	29
Figure 5.	LQFP64 package pinout	30
Figure 6.	LQFP48 package pinout	30
Figure 7.	UFQFPN48 package pinout	31
Figure 8.	WLCSP49 package pinout	31
Figure 9.	STM32F071xB memory map	43
Figure 10.	Pin loading conditions	46
Figure 11.	Pin input voltage	46
Figure 12.	Power supply scheme	47
Figure 13.	Current consumption measurement scheme	48
Figure 14.	High-speed external clock source AC timing diagram	65
Figure 15.	Low-speed external clock source AC timing diagram	65
Figure 16.	Typical application with an 8 MHz crystal	67
Figure 17.	Typical application with a 32.768 kHz crystal	68
Figure 18.	HSI oscillator accuracy characterization results for soldered parts	69
Figure 19.	HSI14 oscillator accuracy characterization results	70
Figure 20.	HSI48 oscillator accuracy characterization results	71
Figure 21.	TC and TTa I/O input characteristics	78
Figure 22.	Five volt tolerant (FT and FTf) I/O input characteristics	78
Figure 23.	I/O AC characteristics definition	81
Figure 24.	Recommended NRST pin protection	82
Figure 25.	ADC accuracy characteristics	85
Figure 26.	Typical connection diagram using the ADC	85
Figure 27.	12-bit buffered / non-buffered DAC	87
Figure 28.	Maximum V_{REFINT} scaler startup time from power down	89
Figure 29.	SPI timing diagram - slave mode and CPHA = 0	93
Figure 30.	SPI timing diagram - slave mode and CPHA = 1	93
Figure 31.	SPI timing diagram - master mode	94
Figure 32.	I ² S slave timing diagram (Philips protocol)	95
Figure 33.	I ² S master timing diagram (Philips protocol)	96
Figure 34.	UFBGA100 package outline	97
Figure 35.	Recommended footprint for UFBGA100 package	98
Figure 36.	UFBGA100 package marking example	99
Figure 37.	LQFP100 package outline	100
Figure 38.	Recommended footprint for LQFP100 package	101
Figure 39.	LQFP100 package marking example	102
Figure 40.	LQFP64 package outline	103
Figure 41.	Recommended footprint for LQFP64 package	104
Figure 42.	LQFP64 package marking example	105
Figure 43.	WLCSP49 package outline	106
Figure 44.	WLCSP49 package marking example	108
Figure 45.	LQFP48 package outline	109
Figure 46.	Recommended footprint for LQFP48 package	110
Figure 47.	LQFP48 package marking example	111
Figure 48.	UFQFPN48 package outline	112

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- $V_{DD} = V_{DDIO1} = 2.0$ to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC are used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- $V_{DDIO2} = 1.65$ to 3.6 V: external power supply for marked I/Os. V_{DDIO2} is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA} , but it must not be provided without a valid supply on V_{DD} . The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to [Figure 12: Power supply scheme](#).

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD} .
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD} .

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} .

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.14.2 General-purpose timers (TIM2, 3, 14, 15, 16, 17)

There are six synchronizable general-purpose timers embedded in the STM32F071x8/xB devices (see [Table 7](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F071x8/xB devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input-only pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		FTf	5 V-tolerant I/O, FM+ capable
		TTa	3.3 V-tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F071x8/xB pin definitions

Pin numbers					Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UFQFPN48	WLCSP49					Alternate functions	Additional functions
B2	1	-	-	-	PE2	I/O	FT	-	TSC_G7_IO1, TIM3_ETR	-
A1	2	-	-	-	PE3	I/O	FT	-	TSC_G7_IO2, TIM3_CH1	-
B1	3	-	-	-	PE4	I/O	FT	-	TSC_G7_IO3, TIM3_CH2	-
C2	4	-	-	-	PE5	I/O	FT	-	TSC_G7_IO4, TIM3_CH3	-
D2	5	-	-	-	PE6	I/O	FT	-	TIM3_CH4	WKUP3, RTC_TAMP3
E2	6	1	1	B7	VBAT	S	-	-	Backup power supply	
C1	7	2	2	D5	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT



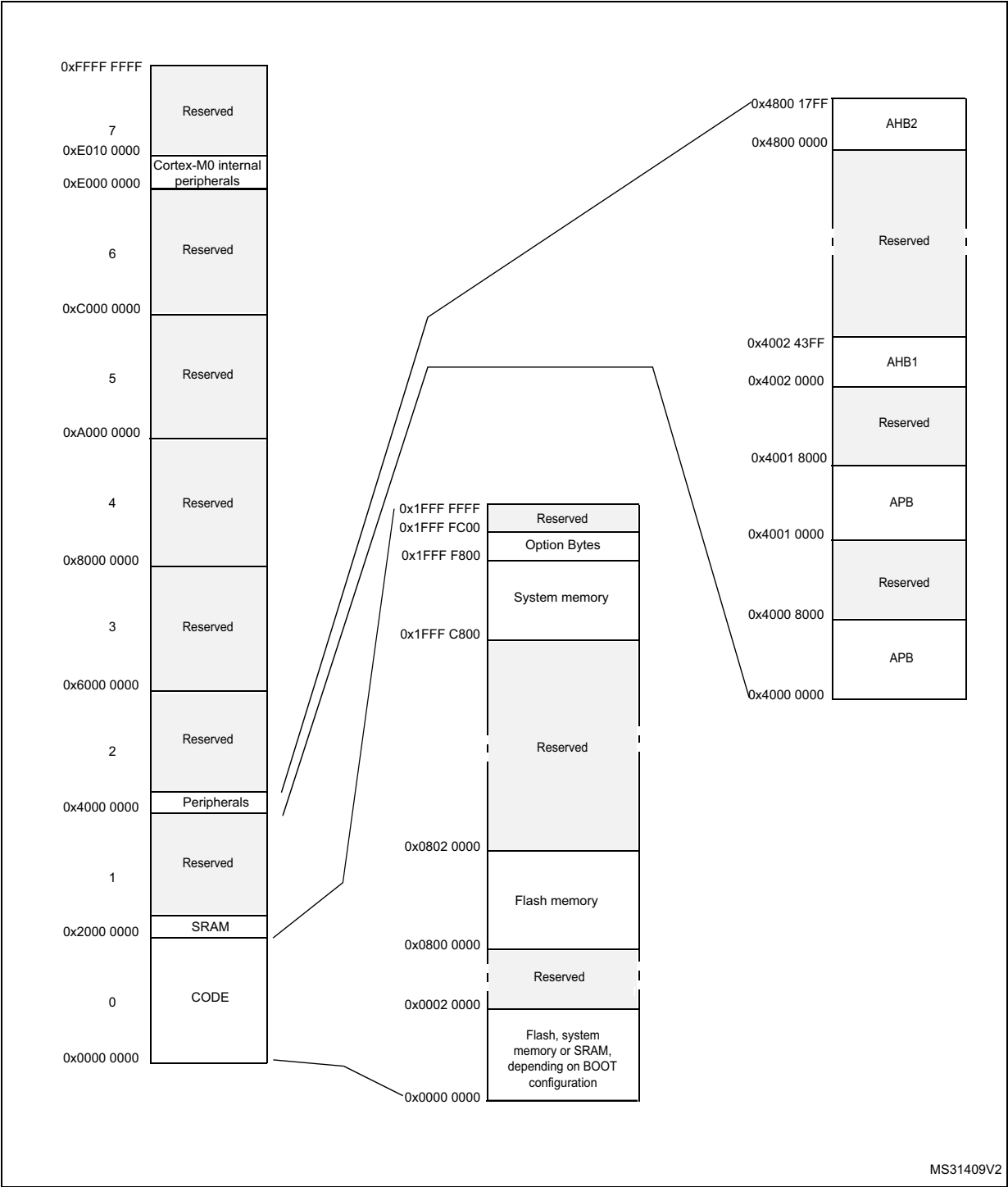
Table 15. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	USART3_CK	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	USART3_RTS	-
PB2	-	-	-	TSC_G3_IO4	-	-
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1	-	-
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2	-	TIM17_BKIN
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	USART4_CTS	-
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC		-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT		SPI2_NSS, I2S2_WS
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK, I2S2_CK
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1	USART3_RX	-
PB12	SPI2_NSS, I2S2_WS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2	USART3_CK	TIM15_BKIN
PB13	SPI2_SCK, I2S2_CK	-	TIM1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL
PB14	SPI2_MISO, I2S2_MCK	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA
PB15	SPI2_MOSI, I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-

5 Memory mapping

To the difference of STM32F071xB memory map in [Figure 9](#), the two bottom code memory spaces of STM32F071x8 end at 0x0000 FFFF and 0x0800 FFFF, respectively.

Figure 9. STM32F071xB memory map



MS31409V2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = V_{DDA} = 3.3\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

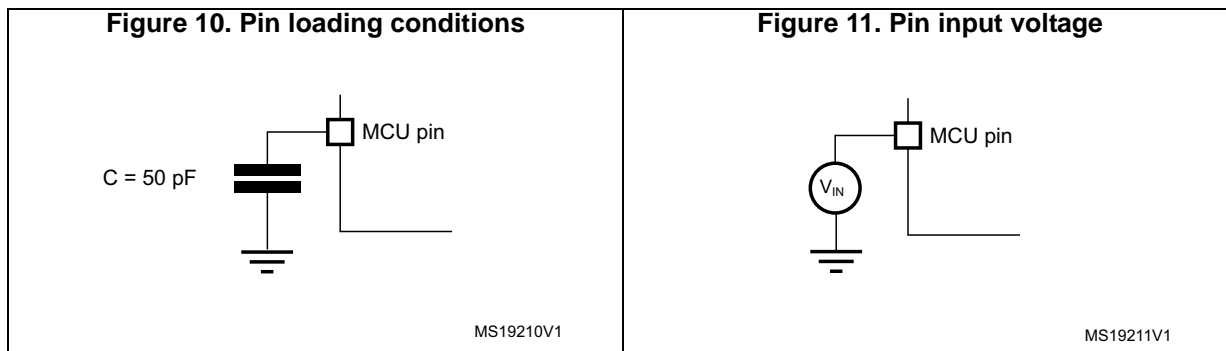
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 10](#).

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 11](#).



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 21: Voltage characteristics](#), [Table 22: Current characteristics](#) and [Table 23: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage	- 0.3	4.0	V
$V_{DDIO2}-V_{SS}$	External I/O supply voltage	- 0.3	4.0	V
$V_{DDA}-V_{SS}$	External analog supply voltage	- 0.3	4.0	V
$V_{DD}-V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
$V_{BAT}-V_{SS}$	External backup supply voltage	- 0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DDIOx} + 4.0^{(3)}$	V
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	V
	BOOT0	0	9.0	V
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	V
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.12: Electrical sensitivity characteristics		-

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 22: Current characteristics](#) for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 27. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}$	PVD current consumption	-	-	0.15	0.26 ⁽¹⁾	μA

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in [Table 28](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 28. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ °C} < T_A < +105\text{ °C}$	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10 ⁽¹⁾	μs
$t_{S_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4 ⁽¹⁾	-	-	μs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DDA} = 3\text{ V}$	-	-	10 ⁽¹⁾	mV
T_{Coeff}	Temperature coefficient	-	- 100 ⁽¹⁾	-	100 ⁽¹⁾	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 13: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 29. Typical and maximum current consumption from V_{DD} supply at $V_{DD} = 3.6$ V (continued)

Symbol	Parameter	Conditions	f _{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T _A ⁽¹⁾			Typ	Max @ T _A ⁽¹⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DD}	Supply current in Run mode, code executing from RAM	HSI48	48 MHz	23.1	25.4	25.8	26.6	12.8	13.5	13.7	13.9	mA
		HSE bypass, PLL on	48 MHz	23.0	25.3 ⁽²⁾	25.7	26.5 ⁽²⁾	12.6	13.3 ⁽²⁾	13.5	13.8 ⁽²⁾	
			32 MHz	15.4	17.3	17.8	18.3	7.96	8.92	9.17	9.73	
			24 MHz	11.4	12.9	13.5	13.7	6.48	8.04	8.23	8.41	
		HSE bypass, PLL off	8 MHz	4.21	4.6	4.89	5.25	2.07	2.3	2.35	2.94	
			1 MHz	0.78	0.9	0.92	1.15	0.36	0.48	0.59	0.82	
		HSI clock, PLL on	48 MHz	23.1	24.5	25.0	25.2	12.6	13.7	13.9	14.0	
			32 MHz	15.4	17.4	17.7	18.2	8.05	8.85	9.16	9.94	
			24 MHz	11.5	13.0	13.6	13.9	6.49	8.06	8.21	8.47	
		HSI clock, PLL off	8 MHz	4.34	4.75	5.03	5.41	2.11	2.36	2.38	2.98	
	Supply current in Sleep mode	HSI48	48 MHz	15.1	16.6	16.8	17.5	3.08	3.43	3.56	3.61	
		HSE bypass, PLL on	48 MHz	15.0	16.5 ⁽²⁾	16.7	17.3 ⁽²⁾	2.93	3.28 ⁽²⁾	3.41	3.46 ⁽²⁾	
			32 MHz	9.9	11.4	11.6	11.9	2.0	2.24	2.32	2.49	
			24 MHz	7.43	8.17	8.71	8.82	1.63	1.82	1.88	1.9	
		HSE bypass, PLL off	8 MHz	2.83	3.09	3.26	3.66	0.76	0.88	0.91	0.93	
			1 MHz	0.42	0.54	0.55	0.67	0.28	0.39	0.41	0.43	
		HSI clock, PLL on	48 MHz	15.0	17.2	17.3	17.9	3.04	3.37	3.41	3.46	
			32 MHz	9.93	11.3	11.6	11.7	2.11	2.35	2.44	2.65	
			24 MHz	7.53	8.45	8.87	8.95	1.64	1.83	1.9	1.93	
		HSI clock, PLL off	8 MHz	2.95	3.24	3.41	3.8	0.8	0.92	0.94	0.97	

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 30. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Para- meter	Conditions (1)	f _{HCLK}	V _{DDA} = 2.4 V				V _{DDA} = 3.6 V				Unit
				Typ	Max @ T _A ⁽²⁾			Typ	Max @ T _A ⁽²⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSI48	48 MHz	311	326	334	343	322	337	345	354	μA
		HSE bypass, PLL on	48 MHz	152	170 ⁽³⁾	178	182 ⁽³⁾	165	184 ⁽³⁾	196	200 ⁽³⁾	
			32 MHz	105	121	126	128	113	129	136	138	
			24 MHz	81.9	95.9	99.5	101	88.7	102	107	108	
		HSE bypass, PLL off	8 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
			1 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
		HSI clock, PLL on	48 MHz	223	244	255	260	245	265	279	284	
			32 MHz	176	195	203	206	193	212	221	224	
			24 MHz	154	171	178	181	168	185	192	195	
		HSI clock, PLL off	8 MHz	74.2	83.4	86.4	87.3	83.4	92.5	95.3	96.6	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

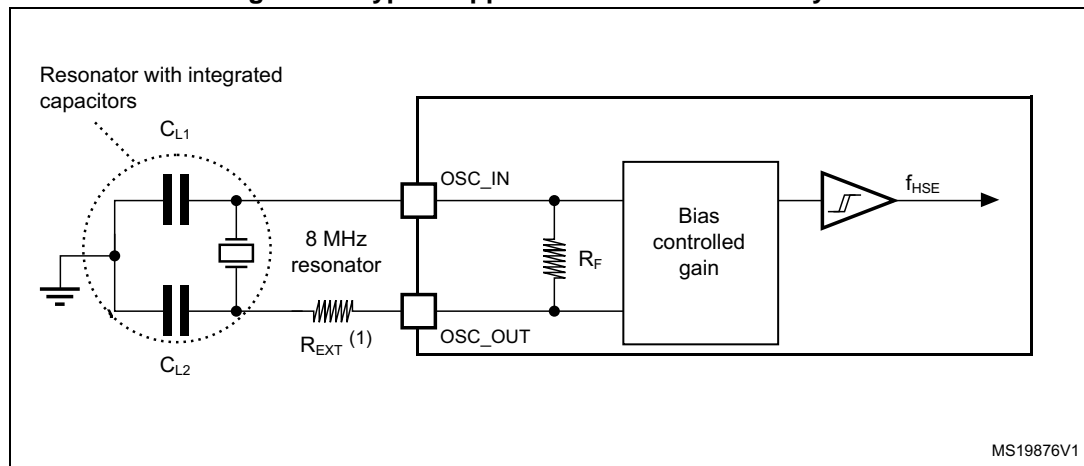
Table 31. Typical and maximum consumption in Stop and Standby modes

Sym- bol	Para- meter	Conditions	Typ @V _{DD} (V _{DD} = V _{DDA})						Max ⁽¹⁾			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	15.4	15.5	15.6	15.7	15.8	15.9	23 ⁽²⁾	49	68 ⁽²⁾	μA
		Regulator in low-power mode, all oscillators OFF	3.2	3.3	3.4	3.5	3.6	3.7	8 ⁽²⁾	33	51 ⁽²⁾	
	Supply current in Standby mode	LSI ON and IWDG ON	0.8	1.0	1.1	1.2	1.3	1.4	-	-	-	
		LSI OFF and IWDG OFF	0.6	0.7	0.9	0.9	1.0	1.1	2.1 ⁽²⁾	2.6	3.1 ⁽²⁾	
I _{DDA}	Supply current in Stop mode	V _{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	2.1	2.2	2.3	2.5	2.6	2.8	3.5 ⁽²⁾	3.6	4.6 ⁽²⁾
			Regulator in low-power mode, all oscillators OFF	2.1	2.2	2.3	2.5	2.6	2.8	3.5 ⁽²⁾	3.6	4.6 ⁽²⁾
	Supply current in Standby mode	V _{DDA} monitoring ON	LSI ON and IWDG ON	2.5	2.7	2.8	3.0	3.2	3.5	-	-	-
			LSI OFF and IWDG OFF	1.9	2.1	2.2	2.3	2.5	2.6	3.5 ⁽²⁾	3.6	4.6 ⁽²⁾
	Supply current in Stop mode	V _{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.3	1.3	1.4	1.4	1.5	1.5	-	-	-
			Regulator in low-power mode, all oscillators OFF	1.3	1.3	1.4	1.4	1.5	1.5	-	-	-
	Supply current in Standby mode	V _{DDA} monitoring OFF	LSI ON and IWDG ON	1.7	1.8	1.9	2.0	2.1	2.2	-	-	-
			LSI OFF and IWDG OFF	1.2	1.2	1.2	1.3	1.3	1.4	-	-	-

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 40](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Typ	Max ⁽²⁾	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.5	0.9	μA
		medium-low drive capability	-	-	1	
		medium-high drive capability	-	-	1.3	
		high drive capability	-	-	1.6	
g_m	Oscillator transconductance	low drive capability	5	-	-	$\mu A/V$
		medium-low drive capability	8	-	-	
		medium-high drive capability	15	-	-	
		high drive capability	25	-	-	
$t_{SU(LSE)}^{(3)}$	Startup time	V_{DDIOX} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

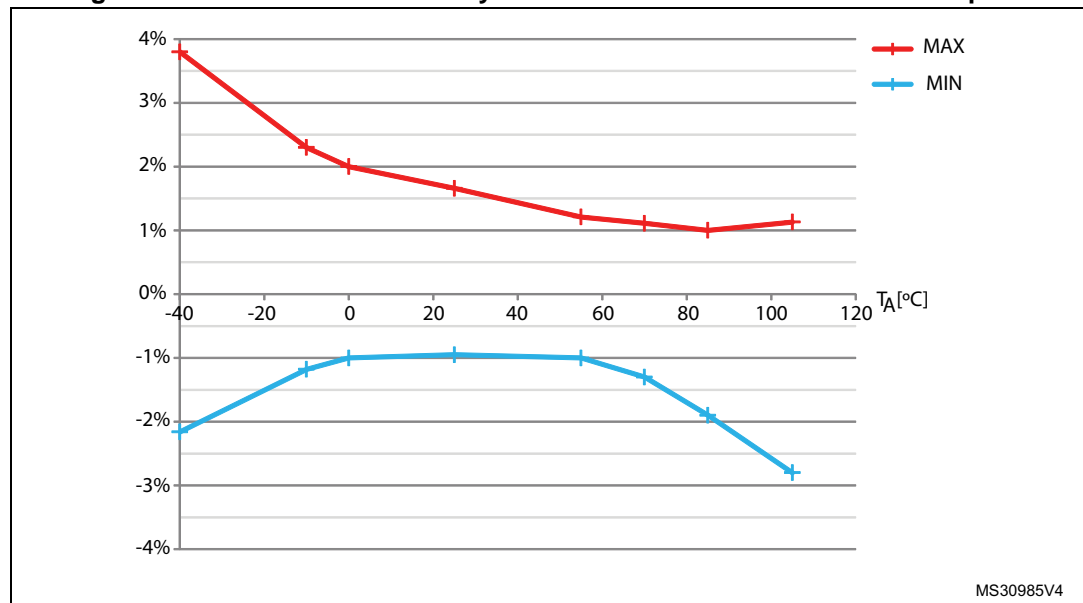
High-speed internal (HSI) RC oscillator

Table 41. HSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1 ⁽²⁾	%
DuCy _(HSI)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
ACC _{HSI}	Accuracy of the HSI oscillator	$T_A = -40$ to 105°C	-2.8 ⁽³⁾	-	3.8 ⁽³⁾	%
		$T_A = -10$ to 85°C	-1.9 ⁽³⁾	-	2.3 ⁽³⁾	
		$T_A = 0$ to 85°C	-1.9 ⁽³⁾	-	2 ⁽³⁾	
		$T_A = 0$ to 70°C	-1.3 ⁽³⁾	-	2 ⁽³⁾	
		$T_A = 0$ to 55°C	-1 ⁽³⁾	-	2 ⁽³⁾	
		$T_A = 25^\circ\text{C}^{(4)}$	-1	-	1	
$t_{\text{su(HSI)}}$	HSI oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs
$I_{\text{DDA(HSI)}}$	HSI oscillator power consumption	-	-	80	100 ⁽²⁾	μA

1. $V_{\text{DDA}} = 3.3\text{ V}$, $T_A = -40$ to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 18. HSI oscillator accuracy characterization results for soldered parts



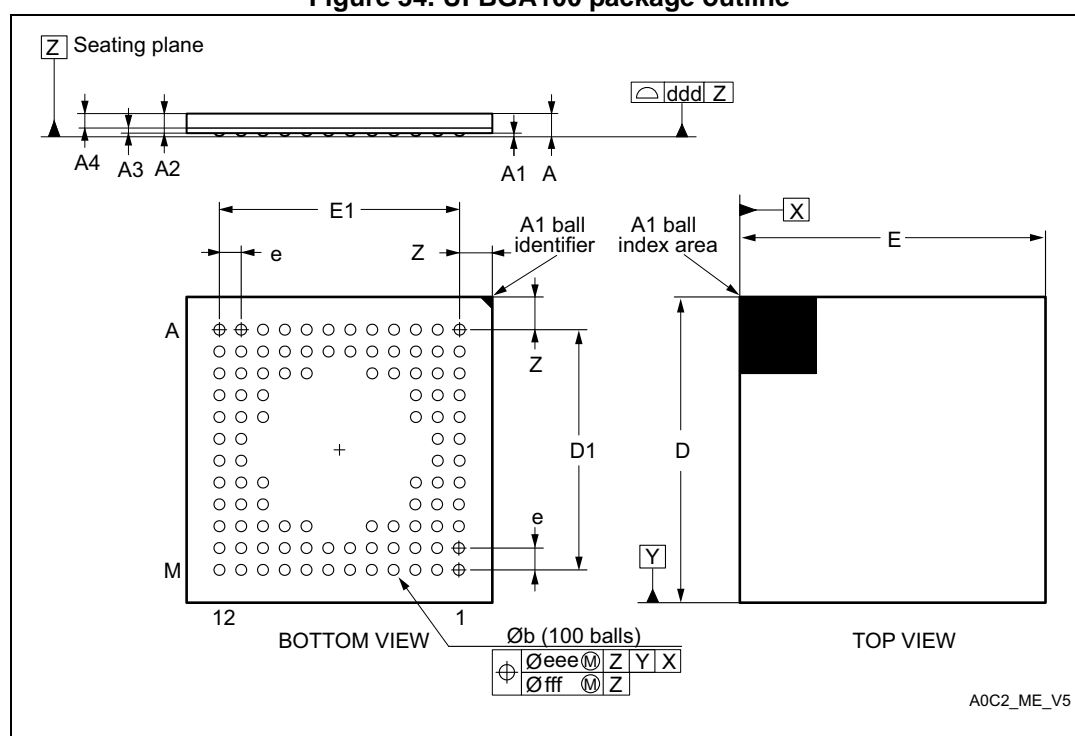
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

7.1 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra-fine-profile ball grid array package.

Figure 34. UFBGA100 package outline



1. Drawing is not to scale.

Table 70. UFBGA100 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-

Table 70. UFBGA100 package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. Recommended footprint for UFBGA100 package

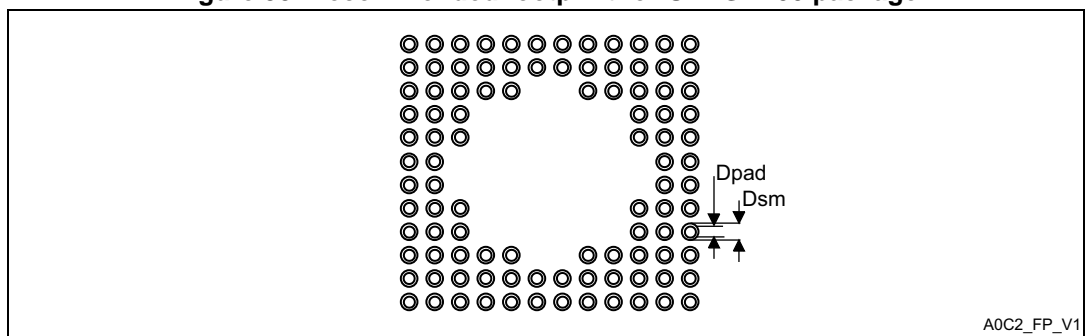


Table 71. UFBGA100 recommended PCB design rules

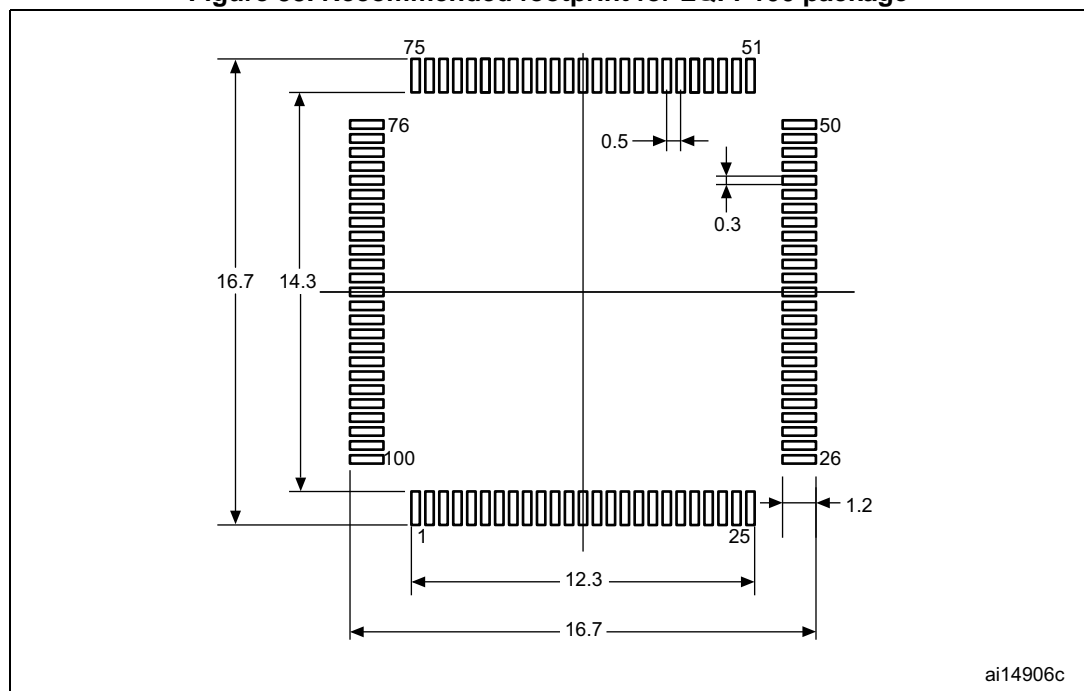
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Table 72. LQPF100 package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. Recommended footprint for LQFP100 package

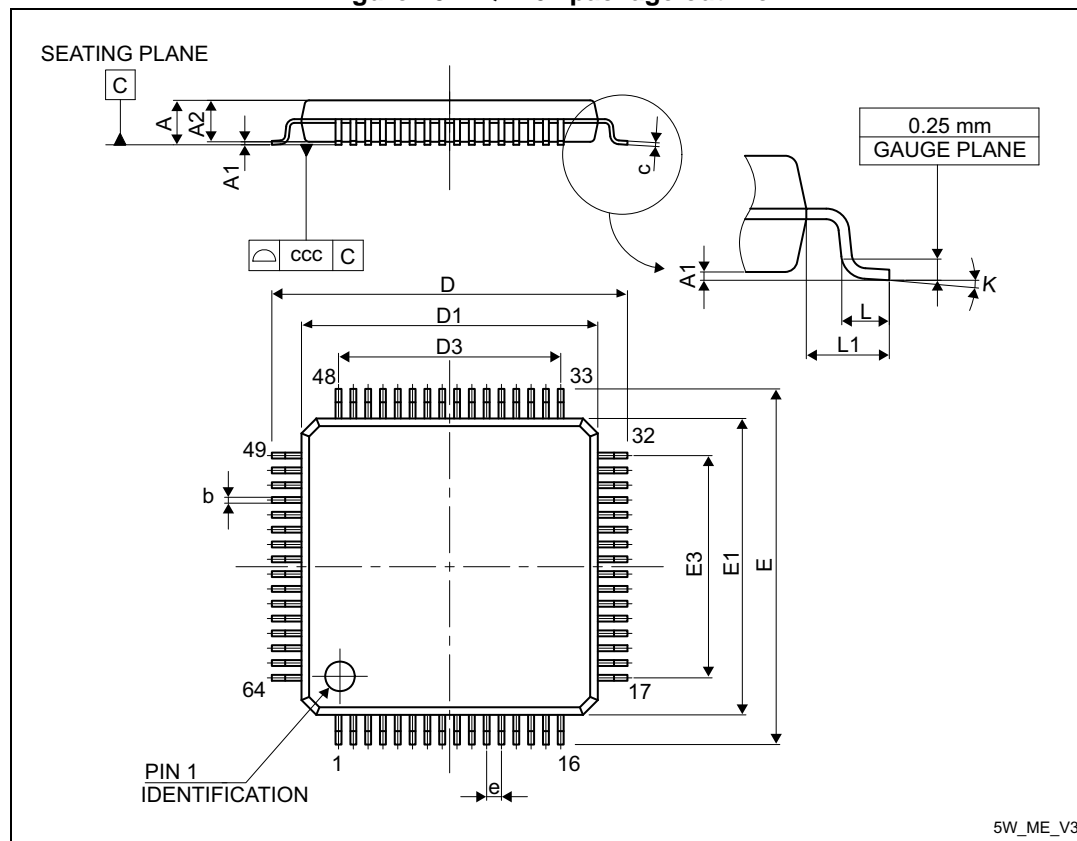


1. Dimensions are expressed in millimeters.

7.3 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 40. LQFP64 package outline



1. Drawing is not to scale.

Table 73. LQFP64 package mechanical data

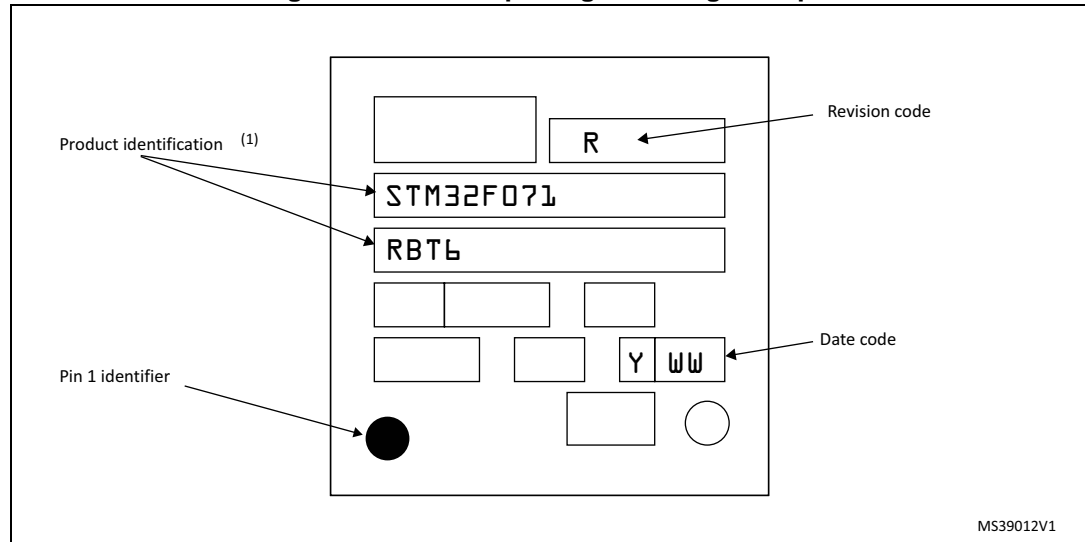
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LQFP64 package marking example



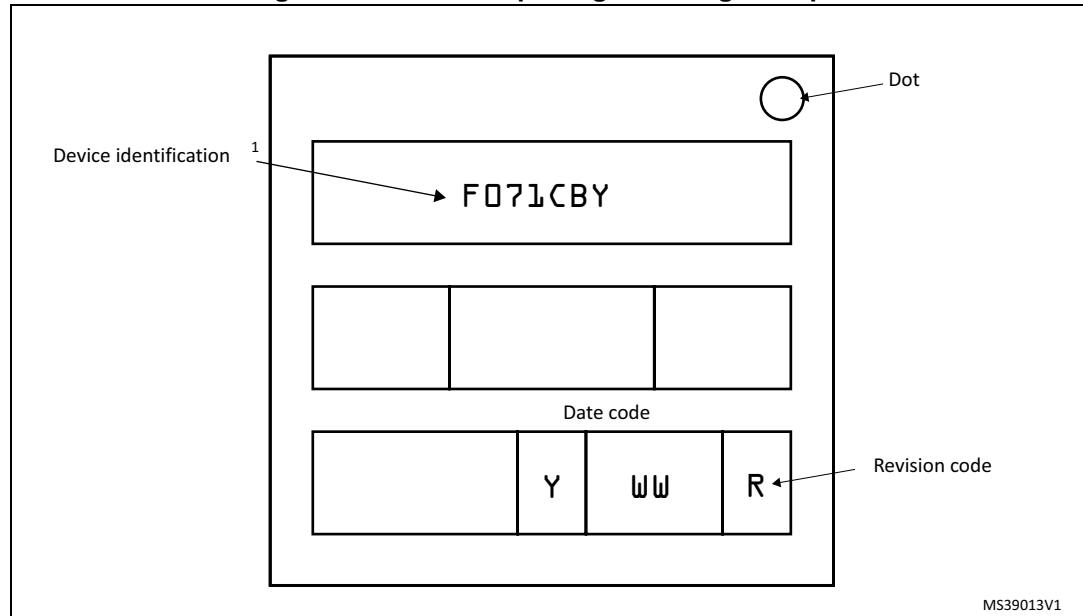
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 44. WLCSP49 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.