**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 87 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 19x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f071v8t7 |

3.14.6 SysTick timer . . . . . 23
3.15 Real-time clock (RTC) and backup registers . . . . . 23
3.16 Inter-integrated circuit interface ($I^2C$) . . . . . 24
3.17 Universal synchronous/asynchronous receiver/transmitter (USART) . . . 25
3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface ($I^2S$) . 26
3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC) . . . . . 26
3.20 Clock recovery system (CRS) . . . . . 27
3.21 Serial wire debug port (SW-DP) . . . . . 27

**4 Pinouts and pin descriptions . . . . . 28**

**5 Memory mapping . . . . . 43**

**6 Electrical characteristics . . . . . 46**

6.1 Parameter conditions . . . . . 46
6.1.1 Minimum and maximum values . . . . . 46
6.1.2 Typical values . . . . . 46
6.1.3 Typical curves . . . . . 46
6.1.4 Loading capacitor . . . . . 46
6.1.5 Pin input voltage . . . . . 46
6.1.6 Power supply scheme . . . . . 47
6.1.7 Current consumption measurement . . . . . 48
6.2 Absolute maximum ratings . . . . . 49
6.3 Operating conditions . . . . . 51
6.3.1 General operating conditions . . . . . 51
6.3.2 Operating conditions at power-up / power-down . . . . . 51
6.3.3 Embedded reset and power control block characteristics . . . . . 52
6.3.4 Embedded reference voltage . . . . . 53
6.3.5 Supply current characteristics . . . . . 53
6.3.6 Wakeup time from low-power mode . . . . . 64
6.3.7 External clock source characteristics . . . . . 64
6.3.8 Internal clock source characteristics . . . . . 68
6.3.9 PLL characteristics . . . . . 72
6.3.10 Memory characteristics . . . . . 72
6.3.11 EMC characteristics . . . . . 73

Table 47. Flash memory endurance and data retention . . . 73
Table 48. EMS characteristics . . . 73
Table 49. EMI characteristics . . . 74
Table 50. ESD absolute maximum ratings . . . 75
Table 51. Electrical sensitivities . . . 75
Table 52. I/O current injection susceptibility . . . 76
Table 53. I/O static characteristics . . . 76
Table 54. Output voltage characteristics . . . 79
Table 55. I/O AC characteristics . . . 80
Table 56. NRST pin characteristics . . . 81
Table 57. ADC characteristics . . . 82
Table 58. $R_{AIN}$ max for $f_{ADC}$ = 14 MHz . . . 84
Table 59. ADC accuracy . . . 84
Table 60. DAC characteristics . . . 86
Table 61. Comparator characteristics . . . 88
Table 62. TS characteristics . . . 90
Table 63. $V_{BAT}$ monitoring characteristics . . . 90
Table 64. TIMx characteristics . . . 90
Table 65. IWDG min/max timeout period at 40 kHz (LSI) . . . 91
Table 66. WWDG min/max timeout value at 48 MHz (PCLK) . . . 91
Table 67. $I^2C$ analog filter characteristics . . . 92
Table 68. SPI characteristics . . . 92
Table 69. $I^2S$ characteristics . . . 94
Table 70. UFBGA100 package mechanical data . . . 97
Table 71. UFBGA100 recommended PCB design rules . . . 98
Table 72. LQPF100 package mechanical data . . . 100
Table 73. LQFP64 package mechanical data . . . 103
Table 74. WLCSP49 package mechanical data . . . 107
Table 75. LQFP48 package mechanical data . . . 110
Table 76. UFQFPN48 package mechanical data . . . 113
Table 77. Package thermal characteristics . . . 115
Table 78. Ordering information scheme . . . 118
Table 79. Document revision history . . . 119

# 3 Functional overview

*Figure 1* shows the general block diagram of the STM32F071x8/xB devices.

## 3.1 ARM®-Cortex®-M0 core

The ARM® Cortex®-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F071x8/xB devices embed ARM core and are compatible with all ARM tools and software.

## 3.2 Memories

The device has the following features:

- 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 64 to 128 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

## 3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15, or PA9/PA10 or $I^2C$ on pins PB6/PB7.

### 3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 87 GPIOs can be connected to the 16 external interrupt lines.

## 3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

### 3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 3. Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA}$= 3.3 V (± 10 mV) | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2 | TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{DDA}$= 3.3 V (± 10 mV) | 0x1FFF F7C2 - 0x1FFF F7C3 |

### 3.10.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and comparators. $V_{REFINT}$ is internally connected to the ADC_IN17 input channel. The

Table 6. Number of capacitive sensing channels available on STM32F071x8/xB devices

| Analog I/O group | Number of capacitive sensing channels | | |
|---|---|---|---|
| | STM32F071Vx | STM32F071Rx | STM32F071Cx |
| G1 | 3 | 3 | 3 |
| G2 | 3 | 3 | 3 |
| G3 | 3 | 3 | 2 |
| G4 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 |
| G6 | 3 | 3 | 3 |
| G7 | 3 | 0 | 0 |
| G8 | 3 | 0 | 0 |
| Number of capacitive sensing channels | 24 | 18 | 17 |

## 3.14 Timers and watchdogs

The STM32F071x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

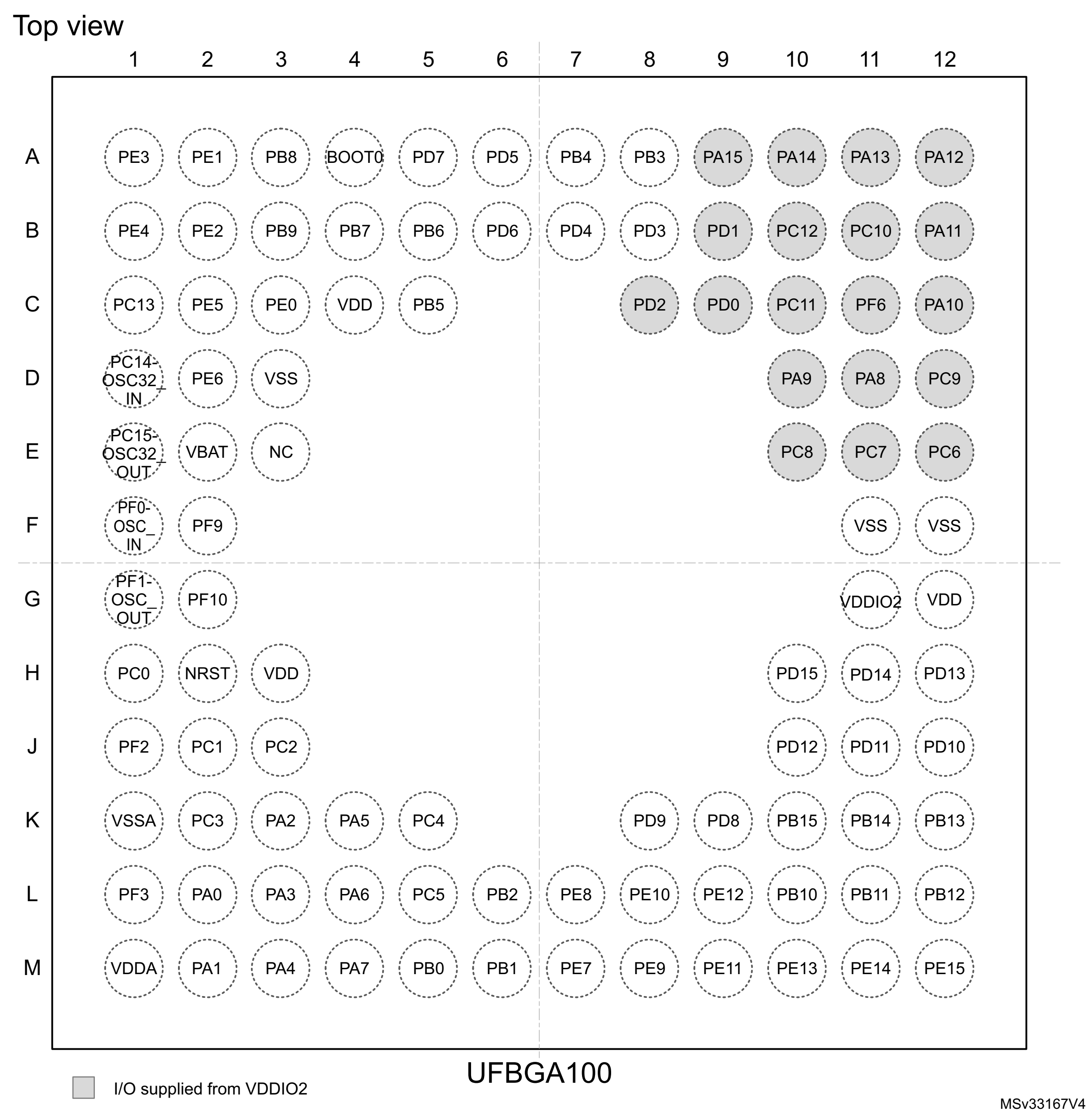
*Table 7* compares the features of the different timers.

Table 7. Timer feature comparison

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | 3 |
| General purpose | TIM2 | 32-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM3 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM14 | 16-bit | Up | integer from 1 to 65536 | No | 1 | - |
| | TIM15 | 16-bit | Up | integer from 1 to 65536 | Yes | 2 | 1 |
| | TIM16<br>TIM17 | 16-bit | Up | integer from 1 to 65536 | Yes | 1 | 1 |
| Basic | TIM6<br>TIM7 | 16-bit | Up | integer from 1 to 65536 | Yes | - | - |

# 4 Pinouts and pin descriptions

Figure 3. UFBGA100 package pinout



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PE3 | PE1 | PB8 | BOOT0 | PD7 | PD5 | PB4 | PB3 | PA15 | PA14 | PA13 | PA12 |
| B | PE4 | PE2 | PB9 | PB7 | PB6 | PD6 | PD4 | PD3 | PD1 | PC12 | PC10 | PA11 |
| C | PC13 | PE5 | PE0 | VDD | PB5 | | | PD2 | PD0 | PC11 | PF6 | PA10 |
| D | PC14-OSC32_IN | PE6 | VSS | | | | | | | PA9 | PA8 | PC9 |
| E | PC15-OSC32_OUT | VBAT | NC | | | | | | | PC8 | PC7 | PC6 |
| F | PF0-OSC_IN | PF9 | | | | | | | | | VSS | VSS |
| G | PF1-OSC_OUT | PF10 | | | | | | | | | VDDIO2 | VDD |
| H | PC0 | NRST | VDD | | | | | | | PD15 | PD14 | PD13 |
| J | PF2 | PC1 | PC2 | | | | | | | PD12 | PD11 | PD10 |
| K | VSSA | PC3 | PA2 | PA5 | PC4 | | | PD9 | PD8 | PB15 | PB14 | PB13 |
| L | PF3 | PA0 | PA3 | PA6 | PC5 | PB2 | PE8 | PE10 | PE12 | PB10 | PB11 | PB12 |
| M | VDDA | PA1 | PA4 | PA7 | PB0 | PB1 | PE7 | PE9 | PE11 | PE13 | PE14 | PE15 |

▨ I/O supplied from VDDIO2

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

| Pin name | AF0 | AF1 |
|---|---|---|
| PE0 | TIM16_CH1 | EVENTOUT |
| PE1 | TIM17_CH1 | EVENTOUT |
| PE2 | TIM3_ETR | TSC_G7_IO1 |
| PE3 | TIM3_CH1 | TSC_G7_IO2 |
| PE4 | TIM3_CH2 | TSC_G7_IO3 |
| PE5 | TIM3_CH3 | TSC_G7_IO4 |
| PE6 | TIM3_CH4 | - |
| PE7 | TIM1_ETR | - |
| PE8 | TIM1_CH1N | - |
| PE9 | TIM1_CH1 | - |
| PE10 | TIM1_CH2N | - |
| PE11 | TIM1_CH2 | - |
| PE12 | TIM1_CH3N | SPI1_NSS, I2S1_WS |
| PE13 | TIM1_CH3 | SPI1_SCK, I2S1_CK |
| PE14 | TIM1_CH4 | SPI1_MISO, I2S1_MCK |
| PE15 | TIM1_BKIN | SPI1_MOSI, I2S1_SD |

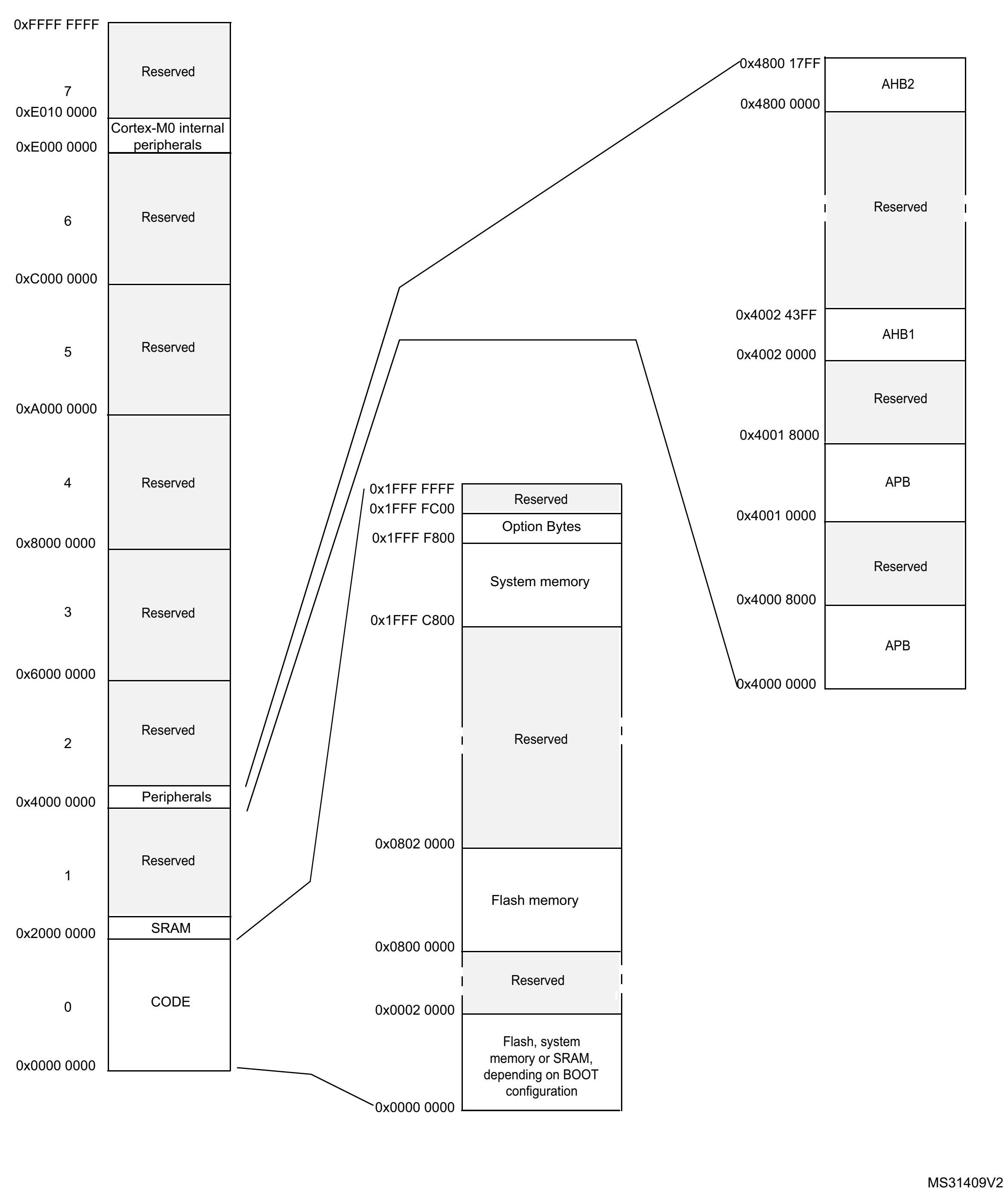
Table 19. Alternate functions available on port F

| Pin name | AF |
|---|---|
| PF0 | CRS_SYNC |
| PF1 | - |
| PF2 | EVENTOUT |
| PF3 | EVENTOUT |
| PF6 | - |
| PF9 | TIM15_CH1 |
| PF10 | TIM15_CH2 |

# 5 Memory mapping

To the difference of STM32F071xB memory map in *Figure 9*, the two bottom code memory spaces of STM32F071x8 end at 0x0000 FFFF and 0x0800 FFFF, respectively.

**Figure 9. STM32F071xB memory map**



# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A = T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD} = V_{DDA}$ = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

**Figure 10. Pin loading conditions**

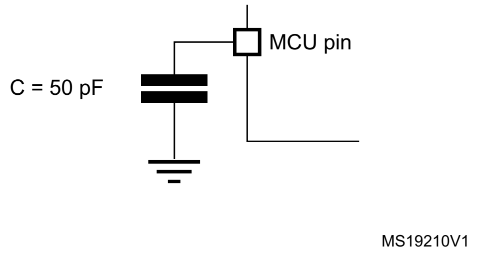
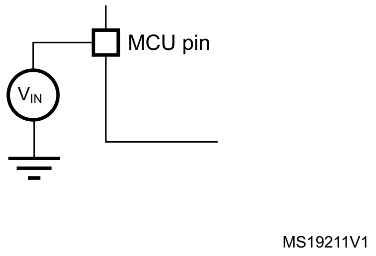


**Figure 11. Pin input voltage**



### 6.1.7 Current consumption measurement

**Figure 13. Current consumption measurement scheme**

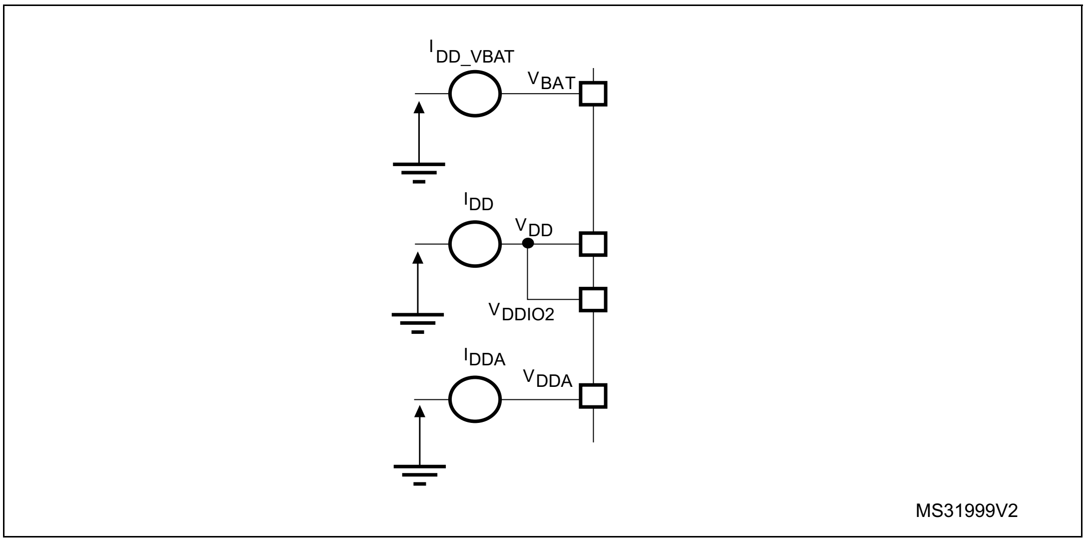


Table 27. Programmable voltage detector characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD6}$ | PVD threshold 6 | Rising edge | 2.66 | 2.78 | 2.9 | V |
| | | Falling edge | 2.56 | 2.68 | 2.8 | V |
| $V_{PVD7}$ | PVD threshold 7 | Rising edge | 2.76 | 2.88 | 3 | V |
| | | Falling edge | 2.66 | 2.78 | 2.9 | V |
| $V_{PVDhyst}$(1) | PVD hysteresis | - | - | 100 | - | mV |
| $I_{DD(PVD)}$ | PVD current consumption | - | - | 0.15 | 0.26(1) | µA |

1. Guaranteed by design, not tested in production.

## 6.3.4 Embedded reference voltage

The parameters given in *Table 28* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 28. Embedded internal reference voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | $–40\ °C < T_A < +105\ °C$ | 1.2 | 1.23 | 1.25 | V |
| $t_{START}$ | ADC_IN17 buffer startup time | - | - | - | 10(1) | µs |
| $t_{S\_vrefint}$ | ADC sampling time when reading the internal reference voltage | - | 4(1) | - | - | µs |
| $\Delta V_{REFINT}$ | Internal reference voltage spread over the temperature range | $V_{DDA} = 3\ V$ | - | - | 10(1) | mV |
| $T_{Coeff}$ | Temperature coefficient | - | - 100(1) | - | 100(1) | ppm/°C |

1. Guaranteed by design, not tested in production.

## 6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

### Table 31. Typical and maximum consumption in Stop and Standby modes

| Sym-bol | Para-meter | Conditions | | Typ @$V_{DD}$ ($V_{DD}$ = $V_{DDA}$) | | | | | | Max[1] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Stop mode | Regulator in run mode, all oscillators OFF | | 15.4 | 15.5 | 15.6 | 15.7 | 15.8 | 15.9 | 23[2] | 49 | 68[2] | µA |
| | | Regulator in low-power mode, all oscillators OFF | | 3.2 | 3.3 | 3.4 | 3.5 | 3.6 | 3.7 | 8[2] | 33 | 51[2] | |
| | Supply current in Standby mode | LSI ON and IWDG ON | | 0.8 | 1.0 | 1.1 | 1.2 | 1.3 | 1.4 | - | - | - | |
| | | LSI OFF and IWDG OFF | | 0.6 | 0.7 | 0.9 | 0.9 | 1.0 | 1.1 | 2.1[2] | 2.6 | 3.1[2] | |
| $I_{DDA}$ | Supply current in Stop mode | $V_{DDA}$ monitoring ON | Regulator in run mode, all oscillators OFF | 2.1 | 2.2 | 2.3 | 2.5 | 2.6 | 2.8 | 3.5[2] | 3.6 | 4.6[2] | |
| | | | Regulator in low-power mode, all oscillators OFF | 2.1 | 2.2 | 2.3 | 2.5 | 2.6 | 2.8 | 3.5[2] | 3.6 | 4.6[2] | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | 2.5 | 2.7 | 2.8 | 3.0 | 3.2 | 3.5 | - | - | - | |
| | | | LSI OFF and IWDG OFF | 1.9 | 2.1 | 2.2 | 2.3 | 2.5 | 2.6 | 3.5[2] | 3.6 | 4.6[2] | |
| | Supply current in Stop mode | $V_{DDA}$ monitoring OFF | Regulator in run mode, all oscillators OFF | 1.3 | 1.3 | 1.4 | 1.4 | 1.5 | 1.5 | - | - | - | |
| | | | Regulator in low-power mode, all oscillators OFF | 1.3 | 1.3 | 1.4 | 1.4 | 1.5 | 1.5 | - | - | - | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | 1.7 | 1.8 | 1.9 | 2.0 | 2.1 | 2.2 | - | - | - | |
| | | | LSI OFF and IWDG OFF | 1.2 | 1.2 | 1.2 | 1.3 | 1.3 | 1.4 | - | - | - | |

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of $I_{DD}$ and $I_{DDA}$).

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

#### I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 35: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DDIOx}$ is the I/O supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

$C_S$ is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Figure 21. TC and TTa I/O input characteristics

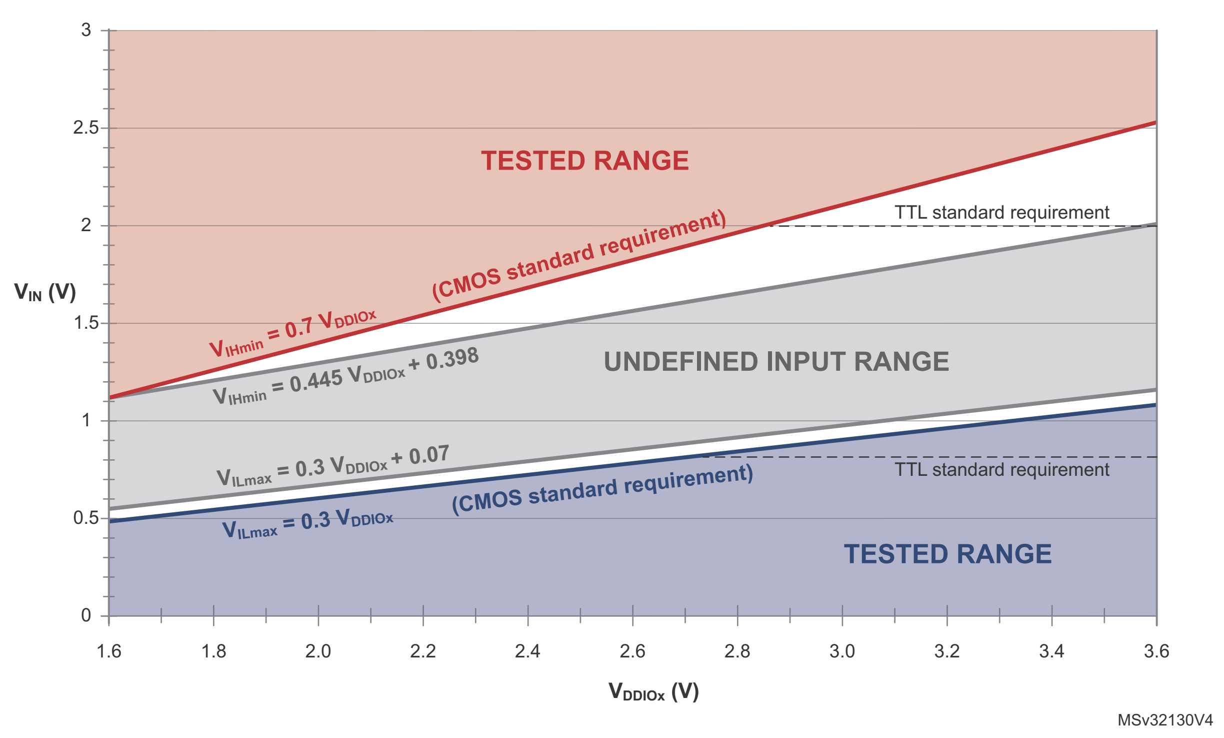
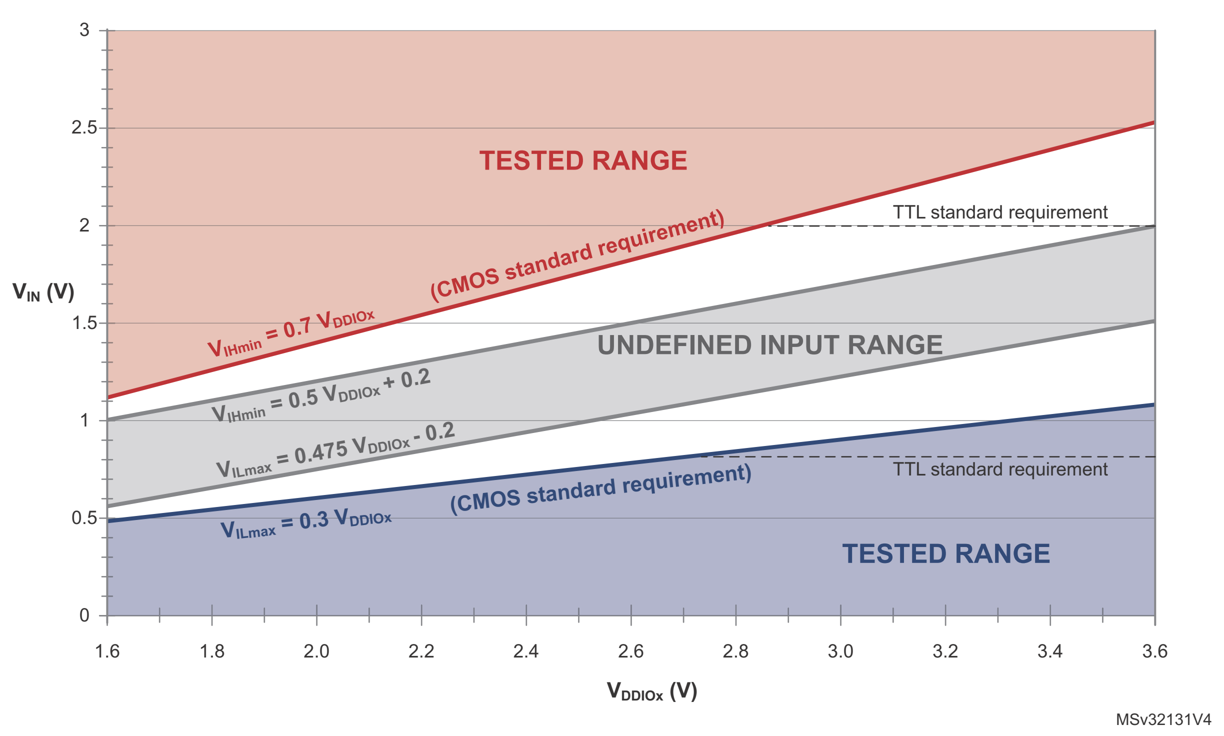


Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics

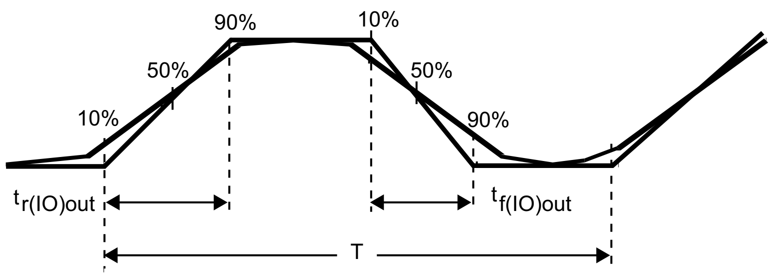


### Table 55. I/O AC characteristics(1)(2) (continued)

| OSPEEDRy [1:0] value(1) | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Fm+ configuration (4) | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DDIOx} \geq 2$ V | - | 2 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 12 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 34 | |
| | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DDIOx} < 2$ V | - | 0.5 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 16 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 44 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10 | - | ns |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 23*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

**Figure 23. I/O AC characteristics definition**



Maximum frequency is achieved if $(t_r + t_f) \leq \frac{2}{3}T$ and if the duty cycle is (45-55%) when loaded by $C_L$ (see the table *I/O AC characteristics definition*)

## 6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

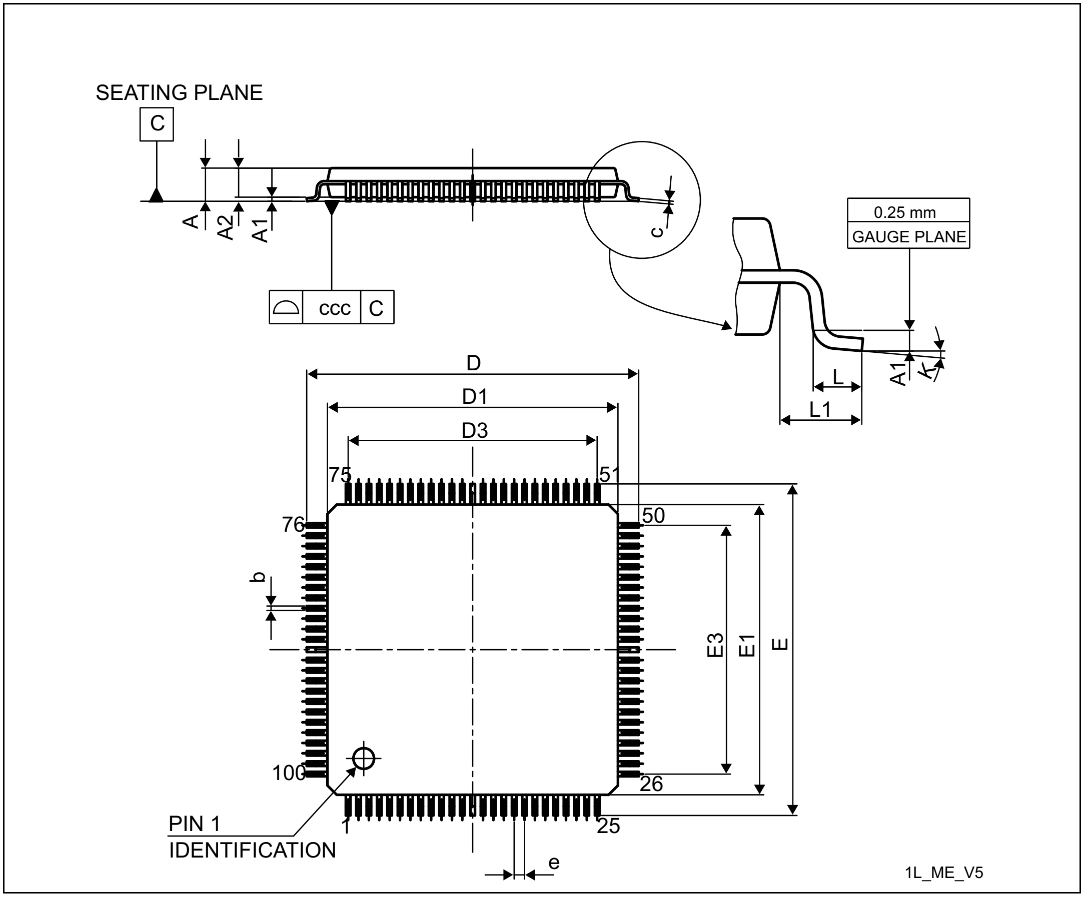
### Table 56. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low level voltage | - | - | - | 0.3 $V_{DD}$+0.07(1) | V |
| $V_{IH(NRST)}$ | NRST input high level voltage | - | 0.445 $V_{DD}$+0.398(1) | - | - | |

## 7.2 LQFP100 package information

**LQFP100 is a100-pin, 14 x 14 mm low-profile quad flat package.**

Figure 37. LQFP100 package outline



1. Drawing is not to scale.

Table 72. LQPF100 package mechanical data

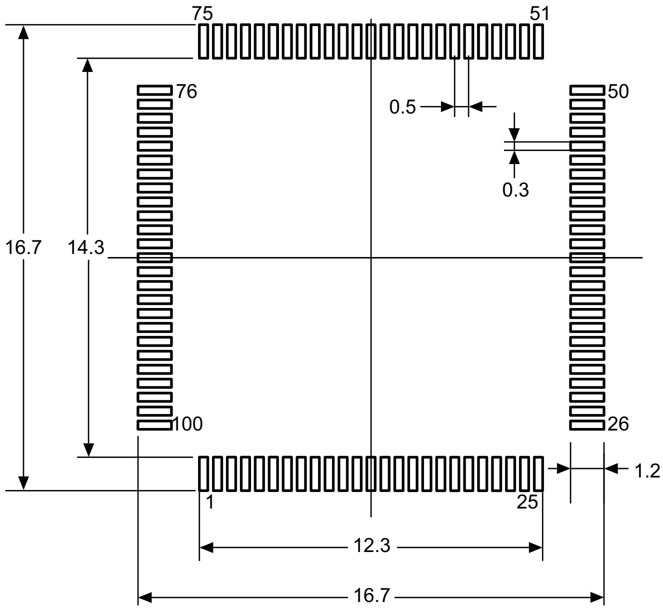
| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.000 | - | - | 0.4724 | - |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |

Table 72. LQPF100 package mechanical data (continued)

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. Recommended footprint for LQFP100 package



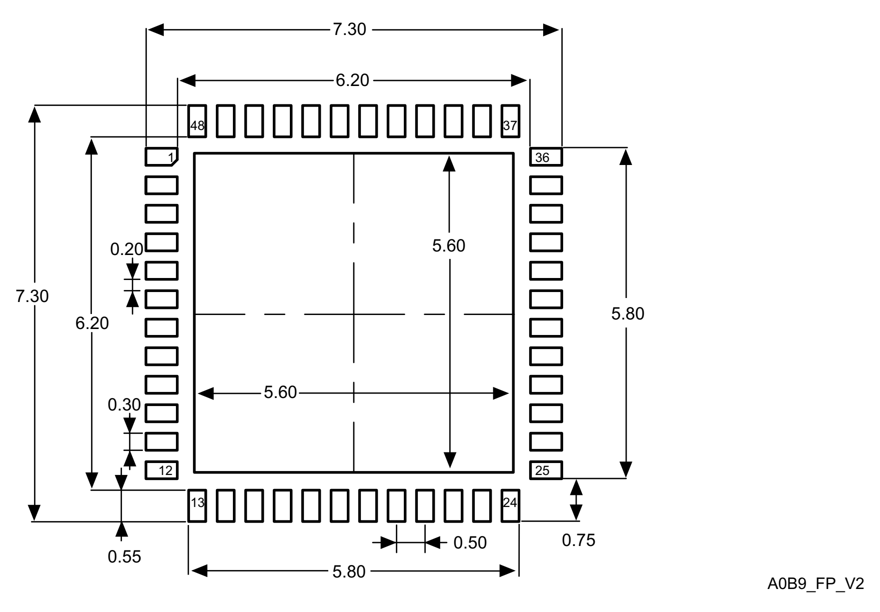
1. Dimensions are expressed in millimeters.

### Table 76. UFQFPN48 package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| D2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| E2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. Recommended footprint for UFQFPN48 package



1. Dimensions are expressed in millimeters.

As applications do not commonly use the STM32F071x8/xB at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax}$ = 50 mA × 3.5 V= 175 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW:

$P_{Dmax}$= 175 + 272 = 447 mW

Using the values obtained in *Table 77* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax}$ = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

*Note:* *With this given $P_{Dmax}$ we can find the $T_{Amax}$ allowed for a given device temperature range (order code suffix 6 or 7).*

*Suffix 6: $T_{Amax}$ = $T_{Jmax}$ - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C*

*Suffix 7: $T_{Amax}$ = $T_{Jmax}$ - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C*

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum temperature $T_{Amax}$ = 100 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax}$ = 20 mA × 3.5 V= 70 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax}$ = 70 + 64 = 134 mW

Thus: $P_{Dmax}$ = 134 mW

Using the values obtained in *Table 77* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax}$ = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

# 8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

**Table 78. Ordering information scheme**

**Example**: STM32 F 071 R B T 6 x

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = General-purpose

**Sub-family**

071 = STM32F071xx

**Pin count**

C = 48/49 pins
R = 64 pins
V = 100 pins

**User code memory size**

8 = 64 Kbyte
B = 128 Kbyte

**Package**

H = UFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

**Temperature range**

6 = –40 to 85 °C
7 = –40 to 105 °C

**Options**

xxx = code ID of programmed parts (includes packing type)
TR = tape and reel packing
blank = tray packing