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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.48x11.48)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc932a1fa-112

- In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC932A1 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

2.3 Comparison to the P89LPC932

The P89LPC932A1 includes several improvements compared to the P89LPC932. Please see *P89LPC932A1 User manual* for additional detailed information.

- Byte-erasability has been added to the user code memory space.
- All of the errata described in the P89LPC932 Errata sheet have been fixed.
- Serial ICP has been added.

5. Functional diagram

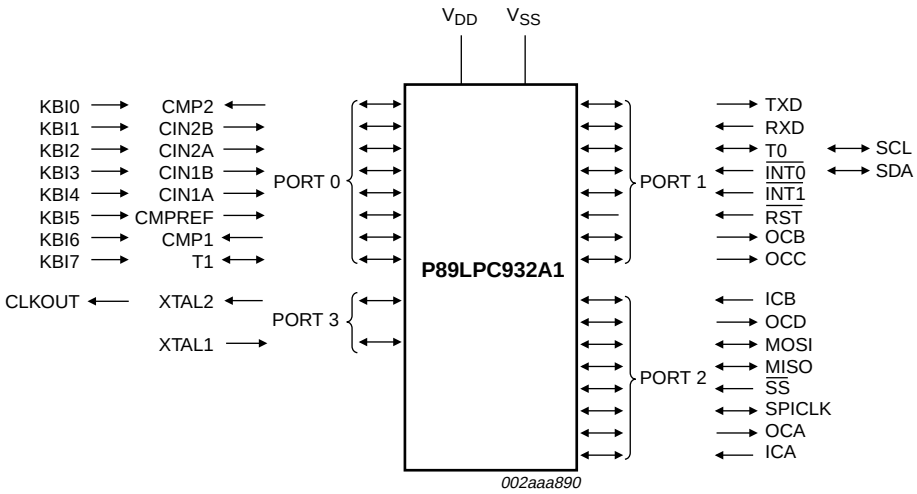


Fig 2. Functional diagram of P89LPC932A1

6. Pinning information

6.1 Pinning

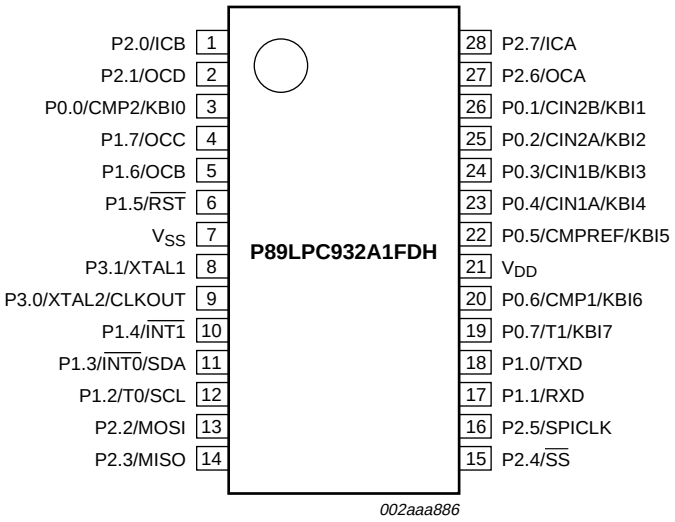


Fig 3. P89LPC932A1 TSSOP28 pin configuration

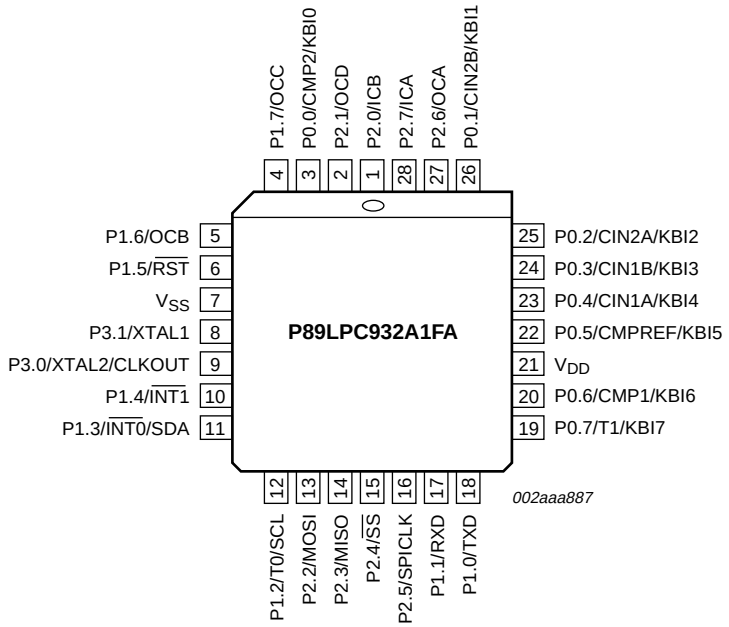


Fig 4. P89LPC932A1 PLCC28 pin configuration

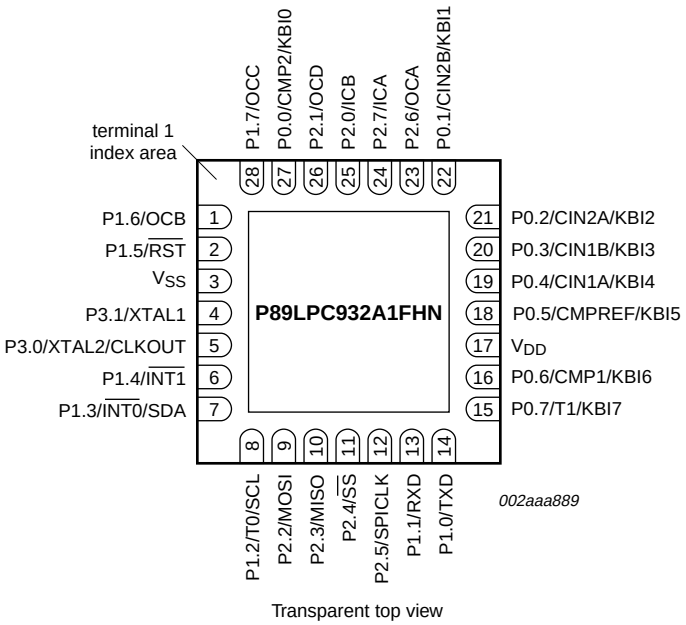


Fig 5. P89LPC932A1 HVQFN28 pin configuration

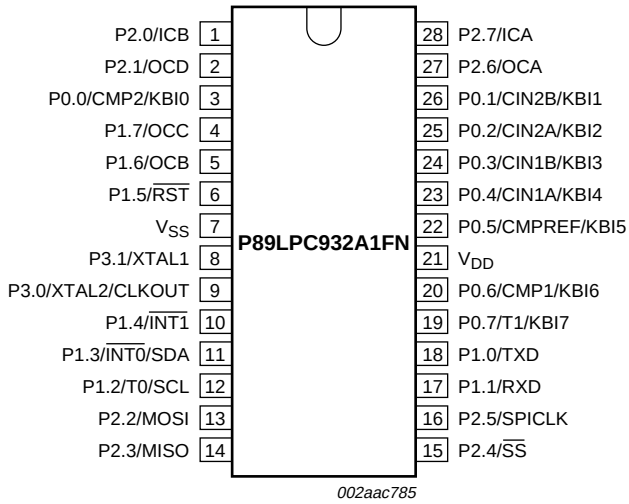


Fig 6. P89LPC932A1 DIP28 pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Type	Description
	TSSOP28, PLCC28, DIP28	HVQFN28		
P0.0 to P0.7			I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 8 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/KBI0	3	27	I/O	**P0.0 —** Port 0 bit 0.
			O	**CMP2 —** Comparator 2 output.
			I	**KBI0 —** Keyboard input 0.
P0.1/CIN2B/KBI1	26	22	I/O	**P0.1 —** Port 0 bit 1.
			I	**CIN2B —** Comparator 2 positive input B.
			I	**KBI1 —** Keyboard input 1.
P0.2/CIN2A/KBI2	25	21	I/O	**P0.2 —** Port 0 bit 2.
			I	**CIN2A —** Comparator 2 positive input A.
			I	**KBI2 —** Keyboard input 2.
P0.3/CIN1B/KBI3	24	20	I/O	**P0.3 —** Port 0 bit 3.
			I	**CIN1B —** Comparator 1 positive input B.
			I	**KBI3 —** Keyboard input 3.

Table 3. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
I2DAT	I^2C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
ICRAH	Input capture A register high	ABH									00	0000 0000
ICRAL	Input capture A register low	AAH									00	0000 0000
ICRBH	Input capture B register high	AFH									00	0000 0000
ICRBL	Input capture B register low	AEH									00	0000 0000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	EIEE	EST	-	ECCU	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[2]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRT H	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[2]	x000 0000
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1*	Interrupt priority 1	F8H	PIEE	PST	-	PCCU	PSPI	PC	PKBI	PI2C	00[2]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PIEEH	PSTH	-	PCCUH	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
OCRAH	Output compare A register high	EFH									00	0000 0000
OCRAL	Output compare A register low	EEH									00	0000 0000

Table 3. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT.2	ENCINT.1	ENCINT.0	00	xxxx x000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TL2	CCU timer low	CCH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TOR2H	CCU reload register high	CFH									00	0000 0000
TOR2L	CCU reload register low	CEH									00	0000 0000
TPCR2H	Prescaler control register high	CBH	-	-	-	-	-	-	TPCR2H.1	TPCR2H.0	00	xxxx xx00
TPCR2L	Prescaler control register low	CAH	TPCR2L.7	TPCR2L.6	TPCR2L.5	TPCR2L.4	TPCR2L.3	TPCR2L.2	TPCR2L.1	TPCR2L.0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0		[5] [4]
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK		[6] [4]
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[2] All ports are in input only (high-impedance) state after power-up.

[3] The RSTSRC register reflects the cause of the P89LPC932A1 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

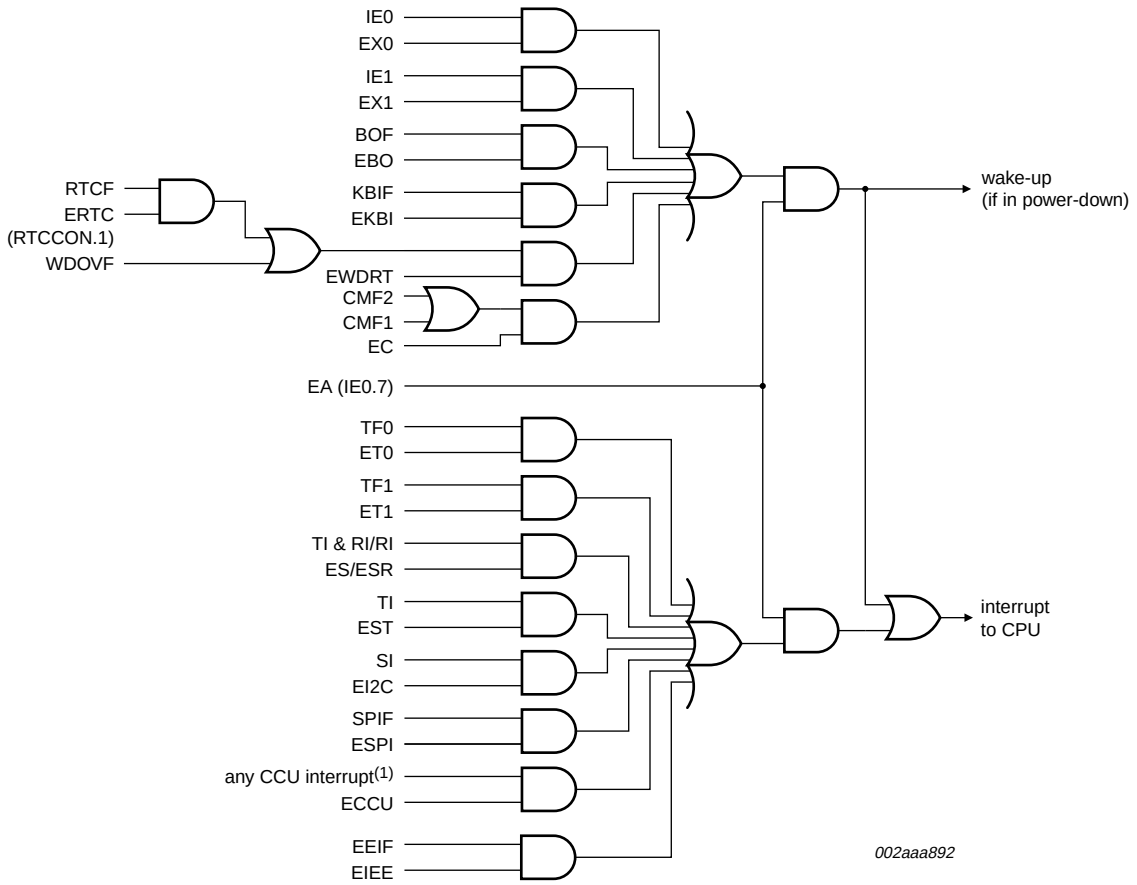
[4] The only reset source that affects these SFRs is power-on reset.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

In edge-triggered mode, if successive samples of the $\overline{INTn}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC932A1 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 7.15 “Power reduction modes” for details.



(1) See Section 7.19 “CCU”

Fig 8. Interrupt sources, interrupt enables, and power-down wake-up sources

7.13 I/O ports

The P89LPC932A1 has four I/O ports: Port 0, Port 1, Port 2, and Port 3. Ports 0, 1 and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 5.

Table 5. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (28-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{RST}$ pin supported	25

7.13.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.13.2 Port 0 analog functions

The P89LPC932A1 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

7.13.3 Additional port features

After power-up, all pins are in Input-only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC932A1 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 8 “Static characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.14 Power monitoring functions

The P89LPC932A1 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

7.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If brownout detection is the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 8 “Static characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC932A1 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

7.19.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

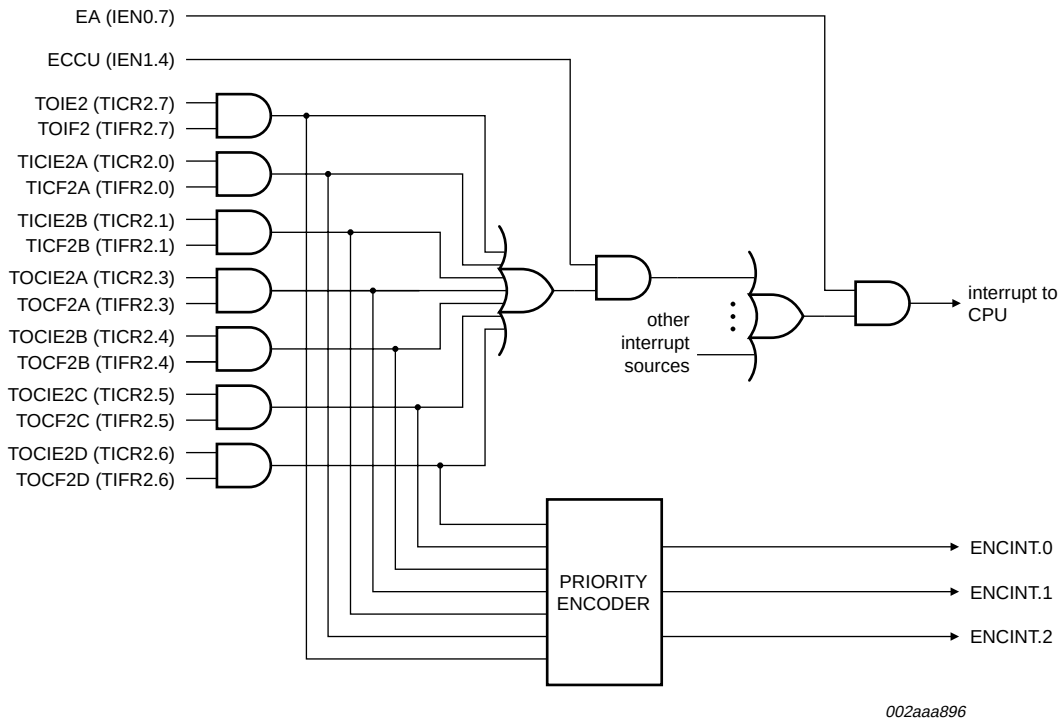


Fig 12. Capture/compare unit interrupts

7.20 UART

The P89LPC932A1 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC932A1 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

7.20.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.20.5 “Baud rate generator and selection”).

7.23 Analog comparators

Two analog comparators are provided on the P89LPC932A1. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 20. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

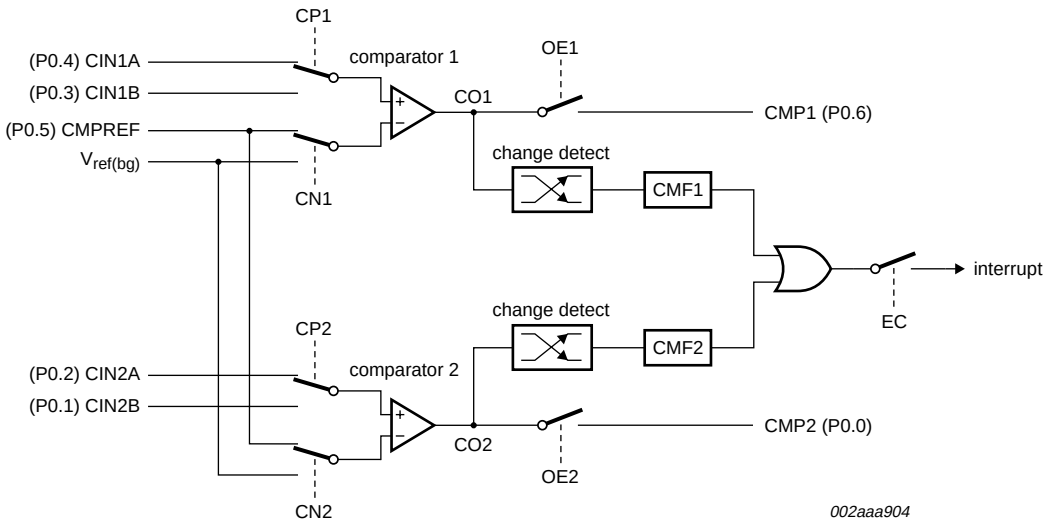


Fig 20. Comparator input and output connections

7.23.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{REF}, is 1.23 V ± 10 %.

7.23.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

7.27 Data EEPROM

The P89LPC932A1 has 512 B of on-chip data EEPROM. The data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This data EEPROM provides 400000 minimum erase/program cycles for each byte.

- **Byte mode:** In this mode, data can be read and written one byte at a time.
- **Row fill:** In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00H.
- **Sector fill:** In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00H.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

7.28 Flash program memory

7.28.1 General description

The P89LPC932A1 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC932A1 flash reliably stores memory contents even after 400000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC932A1 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

7.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 400000 typical erase/program cycles for each byte.
- 20 year minimum data retention.

7.28.3 Flash organization

The program memory consists of eight 1 kB sectors on the P89LPC932A1 device. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 byte to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.28.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

7.28.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock - serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

7.28.6 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC932A1 through a two-wire serial interface. The ICP facility has made ICP in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC932A1 *User manual*.

7.28.7 In-application programming

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The IAP facility has made IAP in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF00H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

Table 8. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = –40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{TL}	logical 1-to-0 transition current, all ports	V_I = 1.5 V at V_{DD} = 3.6 V	[9]	–30	-	–450	µA
$R_{RST(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0		2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage			1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/ °C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 8 “Limiting values” on page 45 for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 9. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
t_{SPILAG}	SPI enable lag time	see Figure 26, 27					
	2.0 MHz (slave)		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 24, 25, 26, 27					
	master		2/CCLK	-	165	-	ns
	slave		3/CCLK	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 24, 25, 26, 27					
	master		2/CCLK	-	165	-	ns
	slave		3/CCLK	-	250	-	ns
t_{SPIDSU}	SPI data set-up time (master or slave)	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIDH}	SPI data hold time (master or slave)	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIA}	SPI access time (slave)	see Figure 26, 27	0	120	0	120	ns
t_{SPIDIS}	SPI disable time (slave)	see Figure 26, 27	0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 24, 25, 26, 27					
	2.0 MHz		-	240	-	240	ns
	3.0 MHz		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 24, 25, 26, 27	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] Parameters are valid over operating temperature range unless otherwise specified.

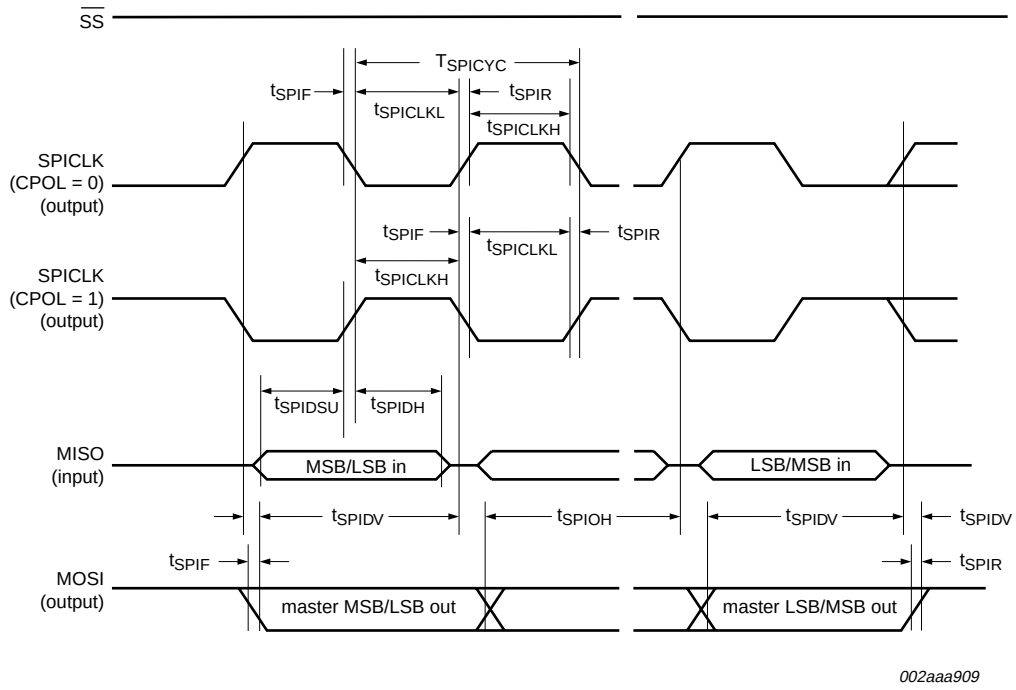


Fig 25. SPI master timing (CPHA = 1)

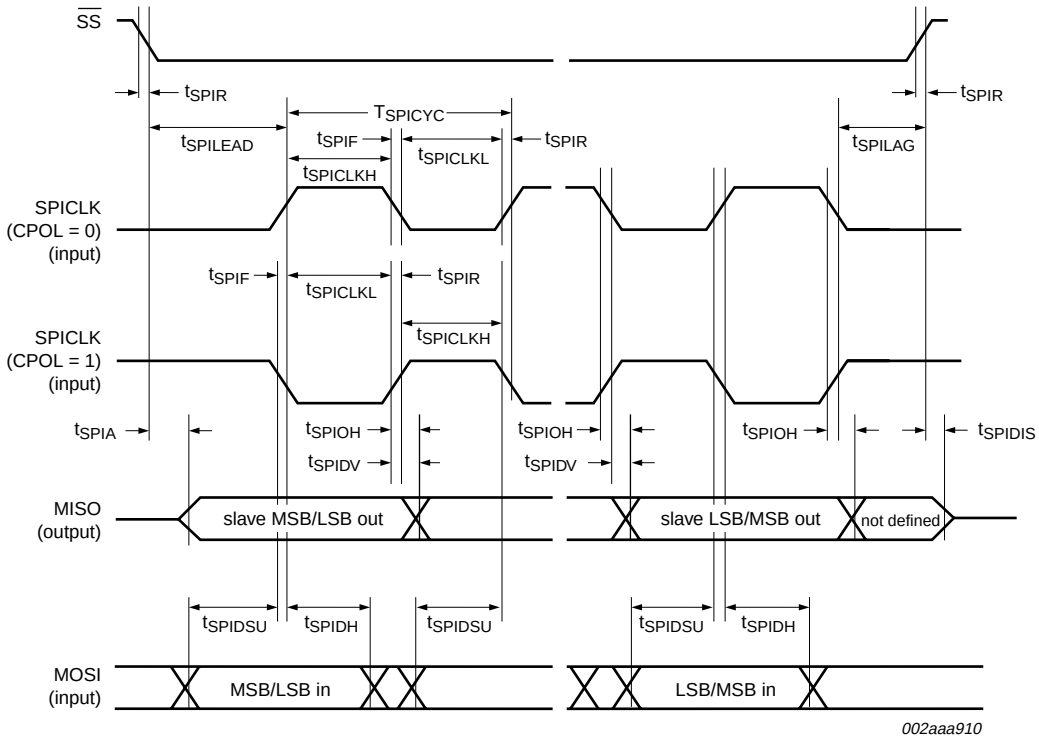
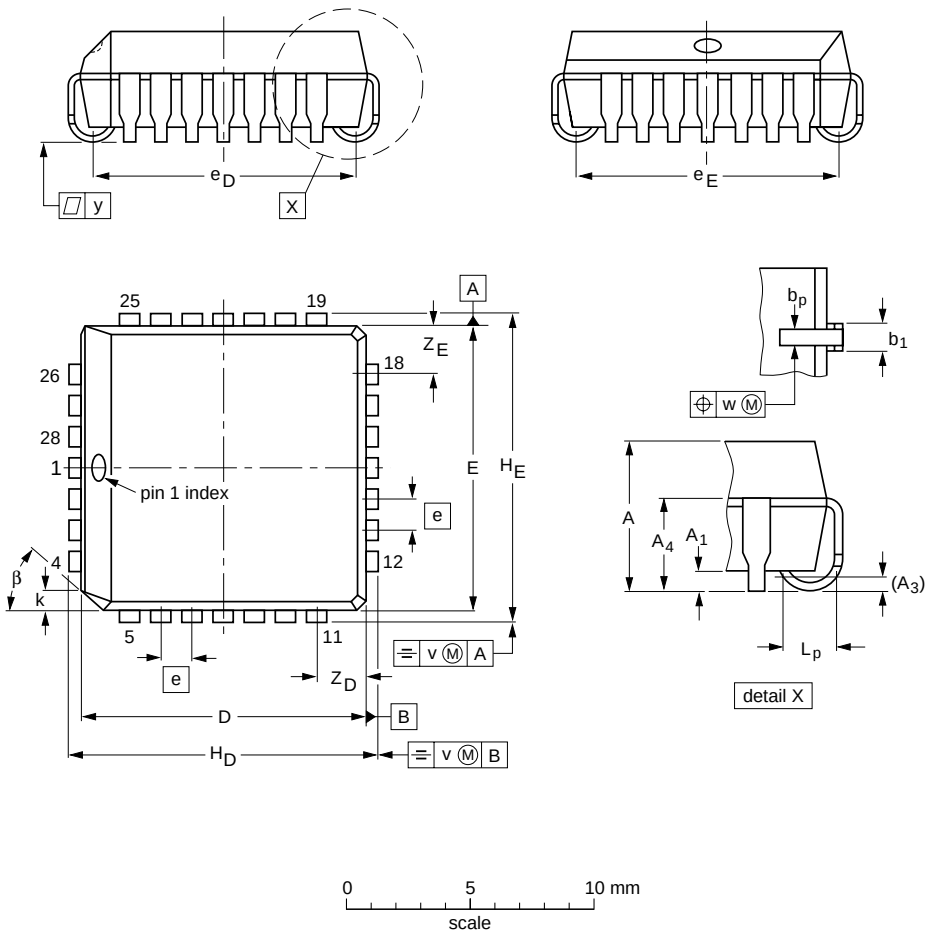


Fig 26. SPI slave timing (CPHA = 0)

12. Package outline

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

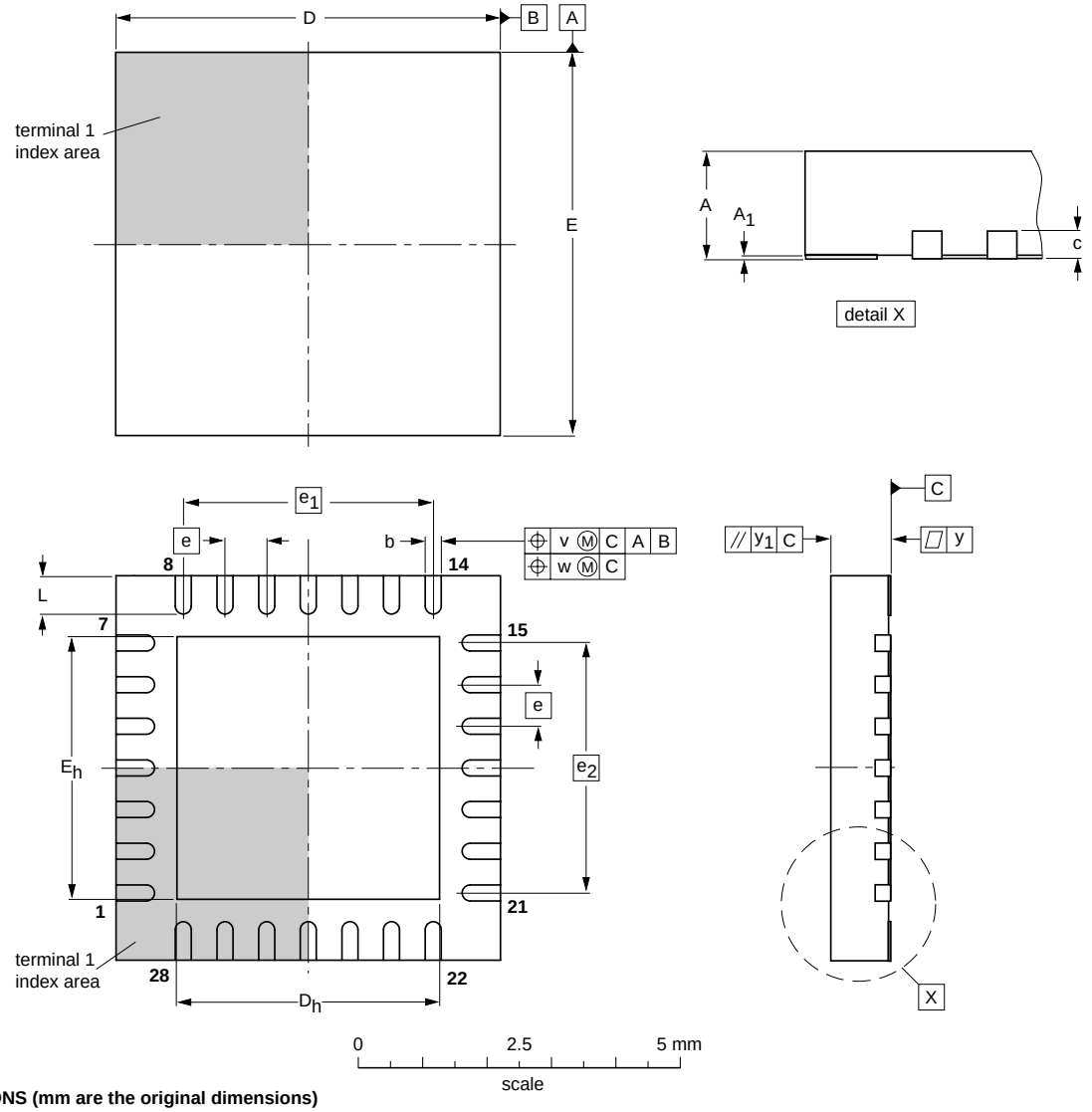
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

Fig 29. Package outline SOT261-2 (PLCC28)

HVQFN28: plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 6 x 6 x 0.85 mm **SOT788-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.35 0.25	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.65	3.9	3.9	0.75 0.50	0.1	0.05	0.05	0.1

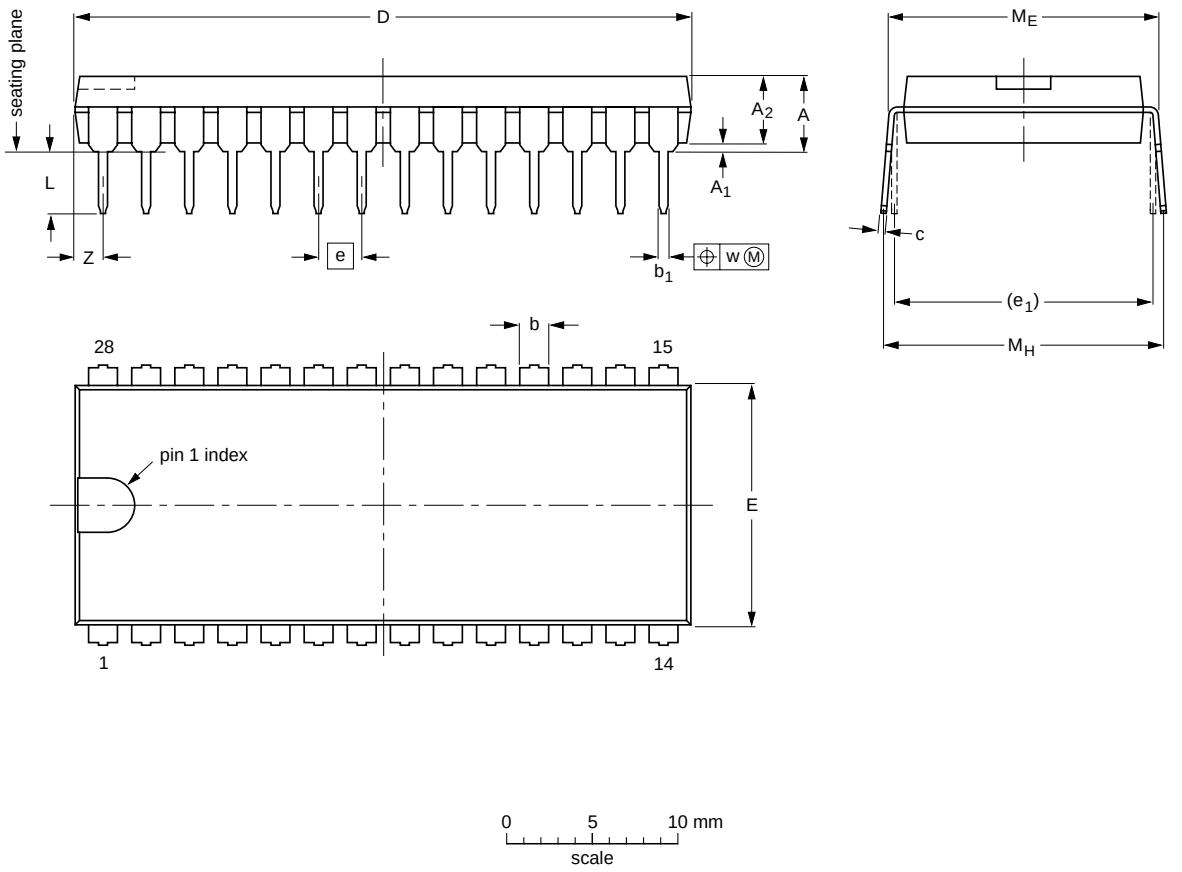
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT788-1	- - -	MO-220	- - -			02-10-22

Fig 31. Package outline SOT788-1 (HVQFN28)

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	36 35	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.2	0.02	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT117-1	051G05	MO-015	SC-510-28			~~99-12-27~~ 03-02-13

Fig 32. Package outline SOT117-1 (DIP28)

13. Abbreviations

Table 13. Acronym list

Acronym	Description
CCU	Capture/Compare Unit
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
LED	Light Emitting Diode
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC932A1_3	20070312	Product data sheet	-	P89LPC932A1_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added new part type P89LPC932A1FN.			
P89LPC932A1_2	20050510	Product data sheet	-	P89LPC932A1_1
P89LPC932A1_1	20040720	Product data sheet	-	-