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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc932a1fdh-529

Table 2. Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28, DIP28	HVQFN28		
P2.7/ICA	28	24	I/O	**P2.7 —** Port 2 bit 7.
			I	**ICA —** Input Capture A.
P3.0 to P3.1			I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 8 “Static characteristics” for details. All pins have Schmitt trigger inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	9	5	I/O	**P3.0 —** Port 3 bit 0.
			O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
			O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	8	4	I/O	**P3.1 —** Port 3 bit 1.
			I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V_{SS}	7	3	I	**Ground:** 0 V reference.
V_{DD}	21	17	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/Output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

Table 3. Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
OCRBH	Output compare B register high	FBH									00	0000 0000
OCRBL	Output compare B register low	FAH									00	0000 0000
OCRCH	Output compare C register high	FDH									00	0000 0000
OCRCL	Output compare C register low	FCH									00	0000 0000
OCRDH	Output compare D register high	FFH									00	0000 0000
OCRDL	Output compare D register low	FEH									00	0000 0000
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0		[2]
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	OCC	OCB	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/ SDA	T0/SCL	RXD	TXD		[2]
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P2*	Port 2	A0H	ICA	OCA	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	OCD	ICB		[2]
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2		[2]
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[2]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[2]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000

7.7 CCLK wake-up delay

The P89LPC932A1 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

7.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.9 Low power select

The P89LPC932A1 is designed to run at 12 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

7.10 Memory organization

The various P89LPC932A1 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  ‘External’ Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC932A1 has 512 bytes of on-chip XDATA memory.

After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1).
- Power-on detect.
- Brownout detect.
- Watchdog timer.
- Software reset.
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.16.1 Reset vector

Following reset, the P89LPC932A1 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the Boot Vector as the high byte of the address and the low byte of the address = 00H.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see P89LPC932A1 *User manual*). Otherwise, instructions will be fetched from address 0000H.

7.17 Timers/counters 0 and 1

The P89LPC932A1 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counter. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the ‘Timer’ function, the register is incremented every machine cycle.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.17.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.17.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.17.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.17.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.17.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

7.17.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.18 RTC/system timer

The P89LPC932A1 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered-down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CCLK or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the RTC and its associated SFRs to the default state.

7.19 CCU

This unit features:

- A 16-bit timer with 16-bit reload on overflow.
- Selectable clock, with prescaler to divide clock source by any integral number between 1 and 1024.
- Four Compare/PWM outputs with selectable polarity
- Symmetrical/Asymmetrical PWM selection
- Two Capture inputs with event counter and digital noise rejection filter
- Seven interrupts with common interrupt vector (one Overflow, two Capture, four Compare)
- Safe 16-bit read/write via shadow registers.

7.19.1 CCU clock

The CCU runs on the CCU Clock (CCUCLK), which is either PCLK in basic timer mode, or the output of a Phase-Locked Loop (PLL). The PLL is designed to use a clock source between 0.5 MHz to 1 MHz that is multiplied by 32 to produce a CCUCLK between 16 MHz and 32 MHz in PWM mode (asymmetrical or symmetrical). The PLL contains a 4-bit divider to help divide PCLK into a frequency between 0.5 MHz and 1 MHz.

7.19.2 CCUCLK prescaling

This CCUCLK can further be divided down by a prescaler. The prescaler is implemented as a 10-bit free-running counter with programmable reload at overflow.

7.19.3 Basic timer operation

The Timer is a free-running up/down counter with a direction control bit. If the timer counting direction is changed while the counter is running, the count sequence will be reversed. The timer can be written or read at any time.

When a reload occurs, the CCU Timer Overflow Interrupt Flag will be set, and an interrupt generated if enabled. The 16-bit CCU Timer may also be used as an 8-bit up/down timer.

7.19.4 Output compare

There are four output compare channels A, B, C and D. Each output compare channel needs to be enabled in order to operate and the user will have to set the associated I/O pin to the desired output mode to connect the pin. When the contents of the timer matches that of a capture compare control register, the Timer Output Compare Interrupt Flag (TOCFx) becomes set. An interrupt will occur if enabled.

7.19.5 Input capture

Input capture is always enabled. Each time a capture event occurs on one of the two input capture pins, the contents of the timer is transferred to the corresponding 16-bit input capture register. The capture event can be programmed to be either rising or falling edge triggered. A simple noise filter can be enabled on the input capture by enabling the Input Capture Noise Filter bit. If set, the capture logic needs to see four consecutive samples of the same value in order to recognize an edge as a capture event. An event counter can be set to delay a capture by a number of capture events.

7.20.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.20.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

7.20.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.23.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

7.24 Keypad interrupt

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

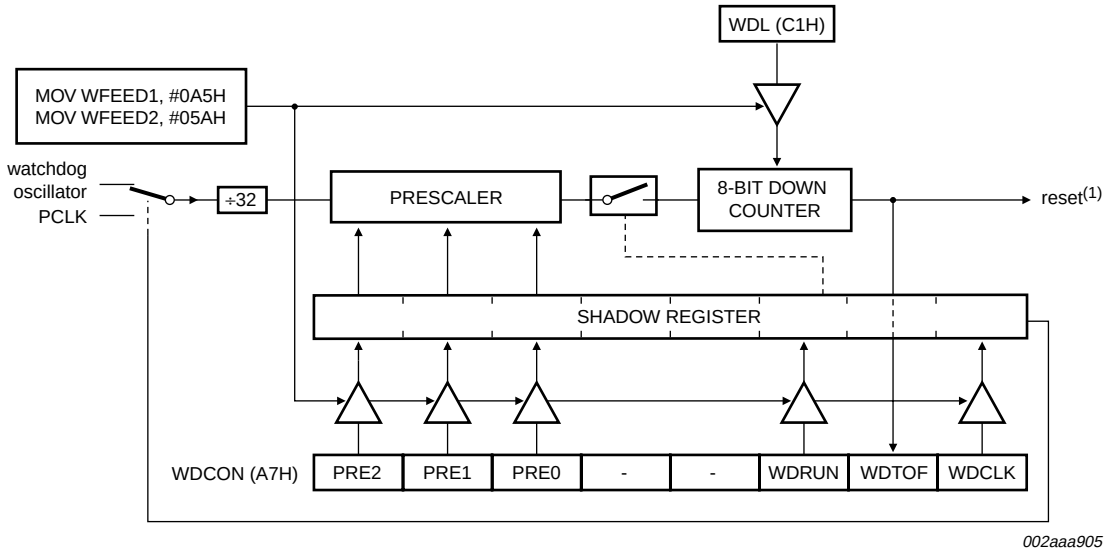
The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

7.25 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 21 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered-down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few µs to a few seconds. Please refer to the P89LPC932A1 *User manual* for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 21. Watchdog timer in Watchdog mode (WDTE = 1)

7.26 Additional features

7.26.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.26.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.27 Data EEPROM

The P89LPC932A1 has 512 B of on-chip data EEPROM. The data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This data EEPROM provides 400000 minimum erase/program cycles for each byte.

- **Byte mode:** In this mode, data can be read and written one byte at a time.
- **Row fill:** In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00H.
- **Sector fill:** In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00H.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

7.28 Flash program memory

7.28.1 General description

The P89LPC932A1 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC932A1 flash reliably stores memory contents even after 400000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC932A1 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

7.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 400000 typical erase/program cycles for each byte.
- 20 year minimum data retention.

7.28.3 Flash organization

The program memory consists of eight 1 kB sectors on the P89LPC932A1 device. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 byte to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.28.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

7.28.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock - serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

7.28.6 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC932A1 through a two-wire serial interface. The ICP facility has made ICP in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC932A1 *User manual*.

7.28.7 In-application programming

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The IAP facility has made IAP in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF00H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC932A1 *User manual*.

7.28.8 In-system programming

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC932A1 through the serial port. This firmware is provided by NXP and embedded within each P89LPC932A1 device. The ISP facility has made ISP in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

7.28.9 Power-on reset code execution

The P89LPC932A1 contains two special flash elements: the Boot Vector and the Boot Status Bit. Following reset, the P89LPC932A1 examines the contents of the Boot Status Bit. If the Boot Status Bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status Bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 6 shows the factory default Boot Vector settings for these devices. **Note: These settings are different than the original P89LPC932. Tools designed to support the** P89LPC932A1 **should be used to program this device, such as Flash Magic version 1.98, or later.** A factory-provided boot loader is preprogrammed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this boot loader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.** A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Table 6. Default Boot Vector values and ISP entry points

Device	Default Boot Vector	Default boot loader entry point	Default boot loader code range	1 kB sector range
P89LPC932A1	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.28.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC932A1 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the Boot Vector (1FH) is changed, it will no longer point to the factory preprogrammed ISP boot loader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	operating bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature range		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per I/O pin		-	20	mA
$I_{OL(I/O)}$	LOW-level output current per I/O pin		-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current		-	100	mA
V_n	voltage on any pin (except V_{SS})	with respect to V_{DD}	-	+3.5	V
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 7 “Limiting values”:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Table 8. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = –40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{TL}	logical 1-to-0 transition current, all ports	V_I = 1.5 V at V_{DD} = 3.6 V	[9]	–30	-	–450	µA
$R_{RST(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0		2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage			1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/ °C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 8 “Limiting values” on page 45 for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 10. Dynamic characteristics (18 MHz) *…continued*

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 24, 25, 26, 27					
	master		2/CCLK	-	111	-	ns
	slave		3/CCLK	-	167	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 24, 25, 26, 27					
	master		2/CCLK	-	111	-	ns
	slave		3/CCLK	-	167	-	ns
t_{SPIDSU}	SPI data set-up time (master or slave)	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIDH}	SPI data hold time (master or slave)	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIA}	SPI access time (slave)	see Figure 26, 27	0	80	0	80	ns
t_{SPIDIS}	SPI disable time (slave)	see Figure 26, 27	0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 24, 25, 26, 27					
	2.0 MHz		-	160	-	160	ns
	3.0 MHz		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 24, 25, 26, 27	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] Parameters are valid over operating temperature range unless otherwise specified.

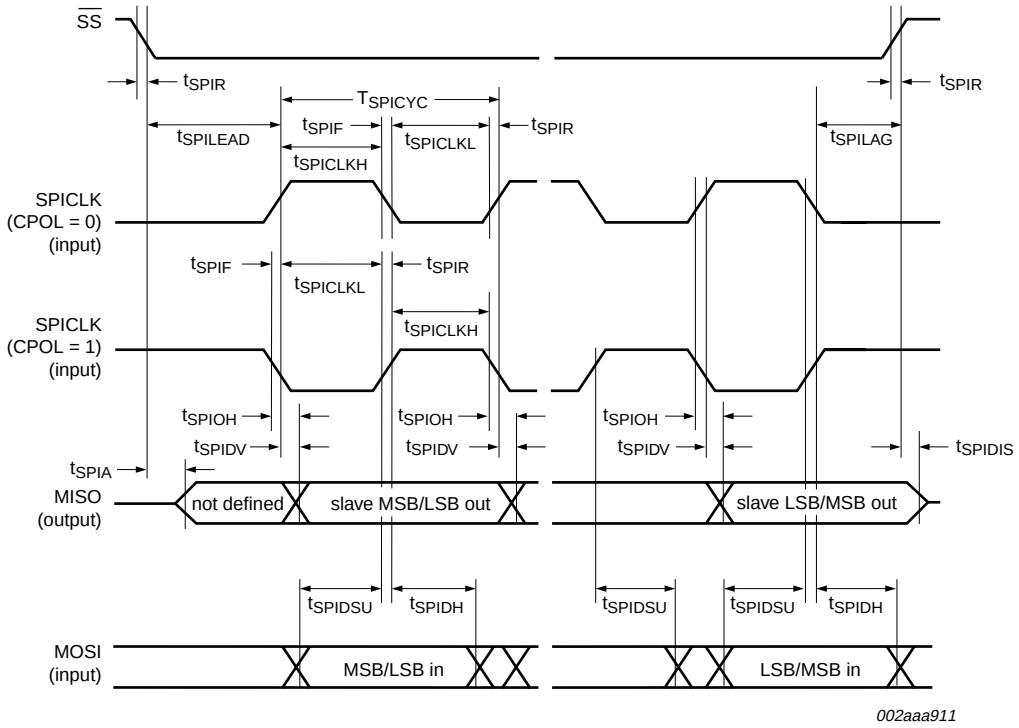


Fig 27. SPI slave timing (CPHA = 1)

10.2 ISP entry mode

Table 11. Dynamic characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	V_{DD} active to $\overline{RST}$ active delay time		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

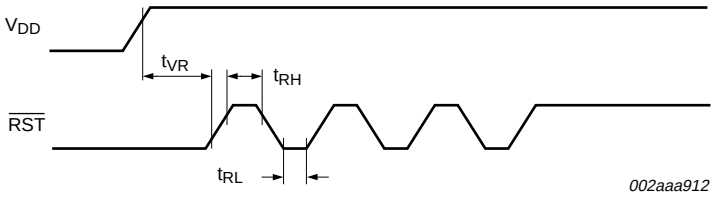


Fig 28. ISP entry waveform

11. Other characteristics

11.1 Comparator electrical characteristics

Table 12. Comparator electrical characteristics

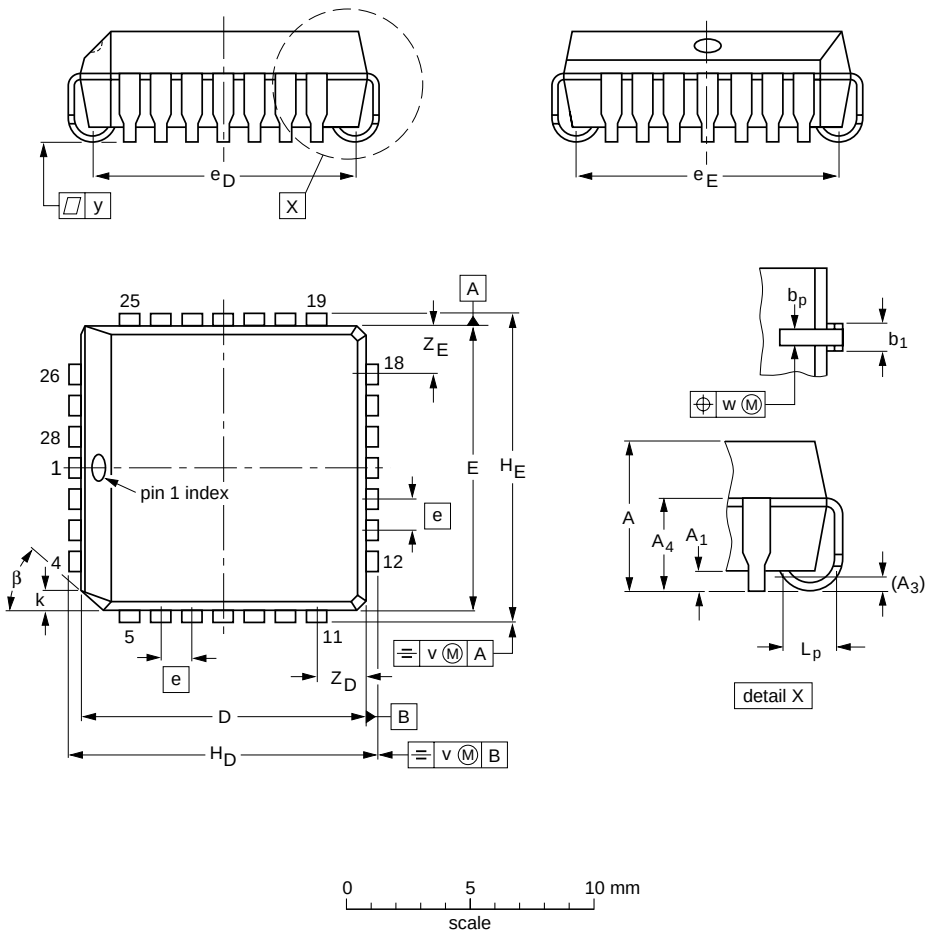
V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±10	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	µs
I_{LI}	input leakage current	0 V < V_I < V_{DD}	-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

12. Package outline

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

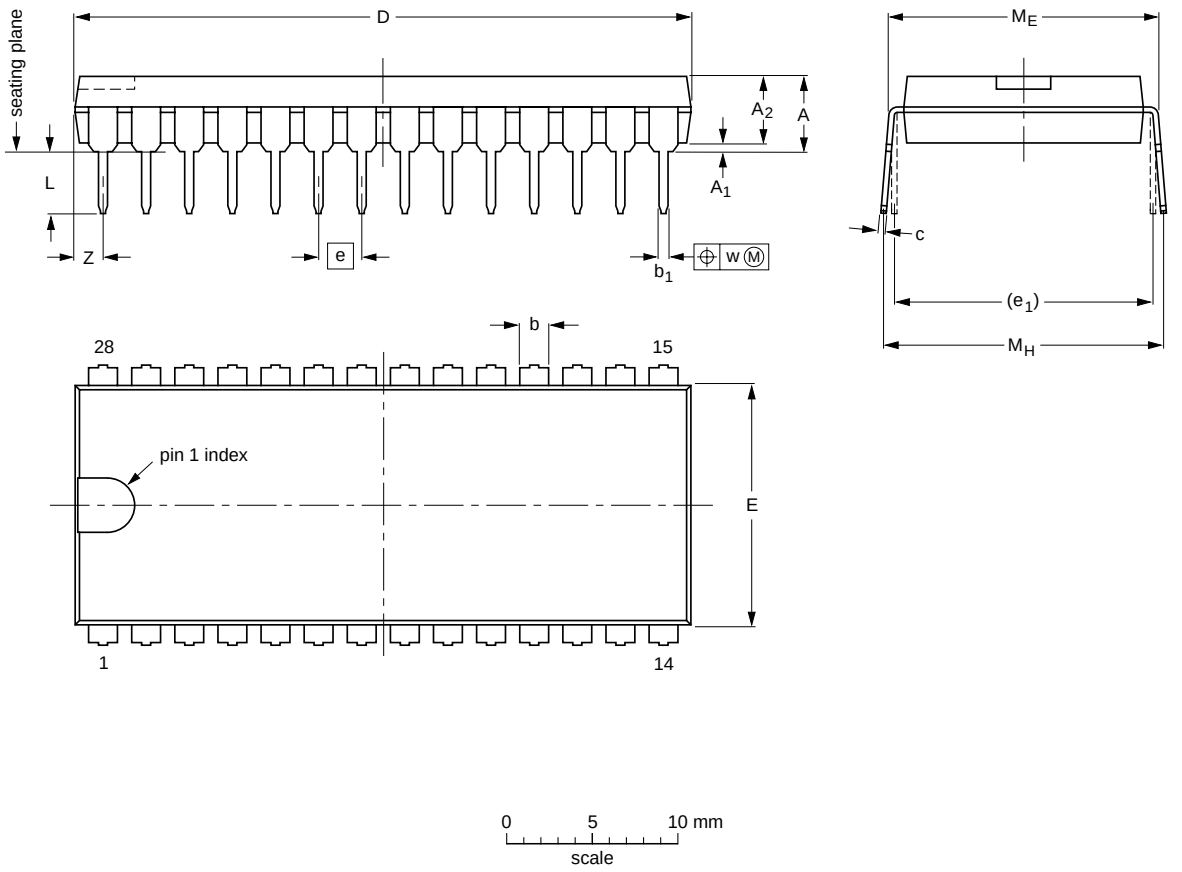
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

Fig 29. Package outline SOT261-2 (PLCC28)

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	36 35	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.2	0.02	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT117-1	051G05	MO-015	SC-510-28			~~99-12-27~~ 03-02-13

Fig 32. Package outline SOT117-1 (DIP28)

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