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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f363aedfa-u0

Table 1.3 Specifications for the 80-Pin Package (1/2)

Item	Function	Description
CPU	Central processing unit	M16C/60 Series core (multiplier: 16 bit × 16 bit → 32 bit, multiply and accumulate instruction: 16 bit × 16 bit + 32 bit → 32 bit) • Number of basic instructions: 91 • Minimum instruction execution time: 50.0 ns (f(BCLK) = 20 MHz, VCC1 = 2.7 to 5.5 V) 100.0 ns (f(BCLK) = 10 MHz, VCC1 = 2.1 to below 2.7 V) 200.0 ns (f(BCLK) = 5 MHz, VCC1 = 1.8 V) • Operating mode: Single-chip
Memory	ROM, RAM, data flash	See Table 1.5 “Product List”.
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
Clock	Clock generator	• 4 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ±10%) • Oscillation stop detection: Main clock oscillation stop/restart detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 Sub clock frequency divider circuit: Divide ratio selectable from 1 and 2 • Power saving features: Wait mode, stop mode • Real-time clock
External Bus Expansion	Bus memory expansion	None
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 68 (selectable pull-up resistors) • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 14 ($\overline{NMI}$, $\overline{INT}$ × 5, key input × 8) • Interrupt priority levels: 7
Watchdog Timer		15-bit timer × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)

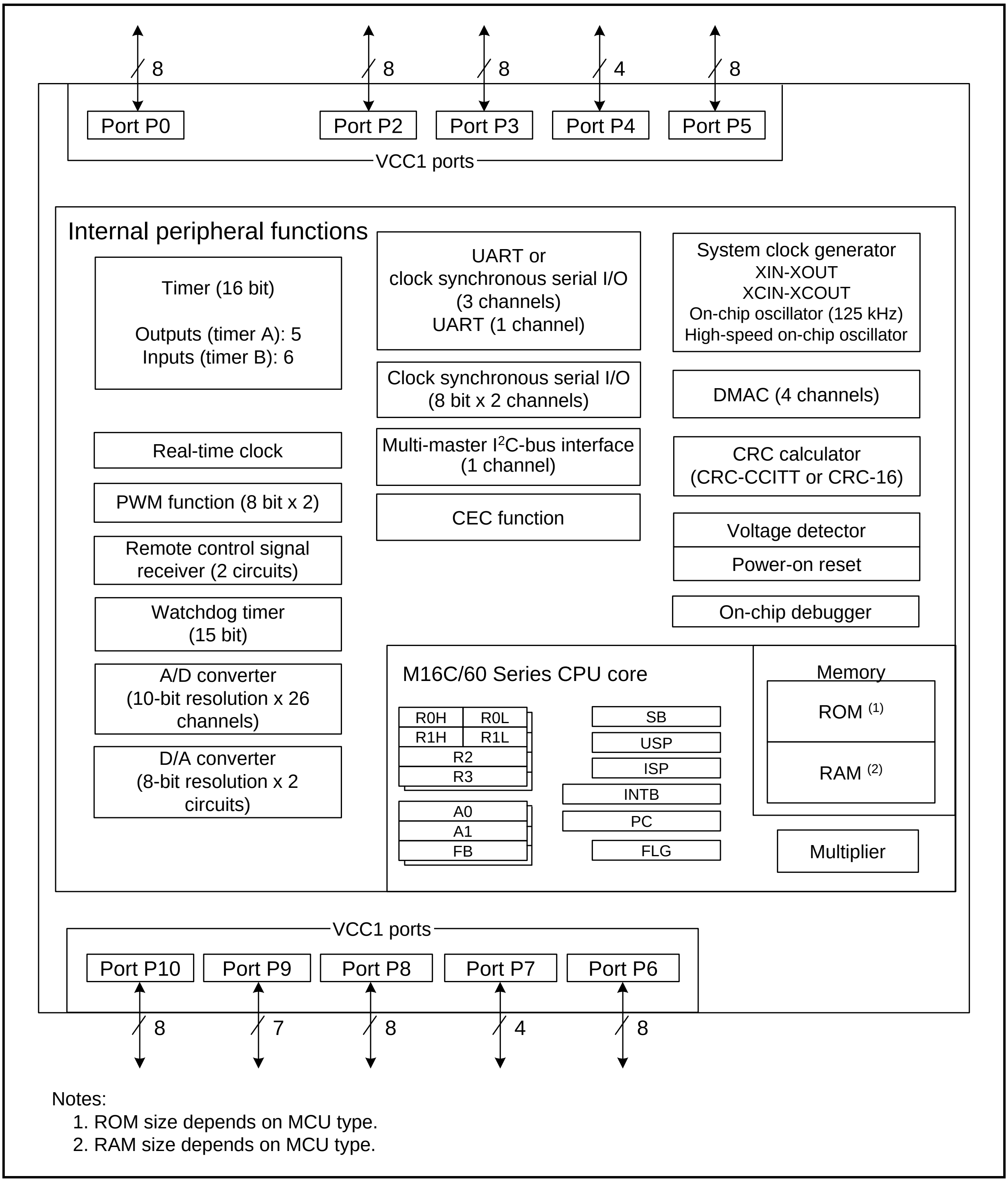
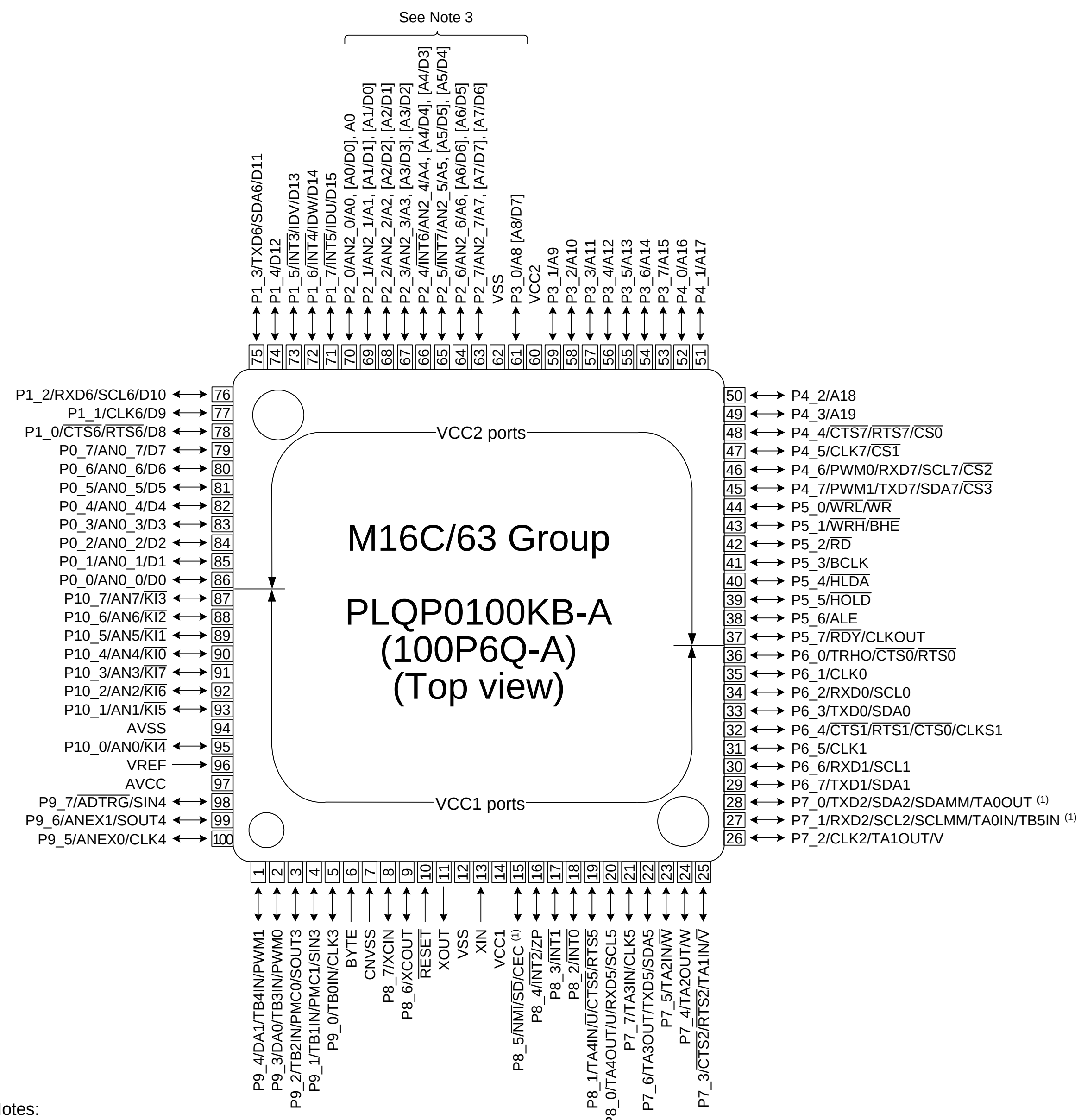


Figure 1.5 Block Diagram for the 80-Pin Package



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

Figure 1.7 Pin Assignment for the 100-Pin Package

Table 1.8 Pin Names for the 80-Pin Package (1/2)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function			
			Interrupt	Timer	Serial interface	A/D converter, D/A converter
1		P9_5			CLK4	ANEX0
2		P9_4		TB4IN/PWM1		DA1
3		P9_3		TB3IN/PWM0		DA0
4		P9_2		TB2IN/PMC0	SOUT3	
5		P9_0		TB0IN	CLK3	
6	CNVSS					
7	XCIN	P8_7				
8	XCOUT	P8_6				
9	$\overline{\text{RESET}}$					
10	XOUT					
11	VSS					
12	XIN					
13	VCC1					
14		P8_5	$\overline{\text{NMI}}$		CEC	
15		P8_4	$\overline{\text{INT2}}$	ZP		
16		P8_3	$\overline{\text{INT1}}$			
17		P8_2	$\overline{\text{INT0}}$			
18		P8_1		TA4IN	$\overline{\text{CTS5}}/\overline{\text{RTS5}}$	
19		P8_0		TA4OUT	RXD5/SCL5	
20		P7_7		TA3IN	CLK5	
21		P7_6		TA3OUT	TXD5/SDA5	
22		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM	
23		P7_0		TA0OUT	TXD2/SDA2/SDAMM	
24		P6_7			TXD1/SDA1	
25		P6_6			RXD1/SCL1	
26		P6_5			CLK1	
27		P6_4			$\overline{\text{CTS1}}/\overline{\text{RTS1}}/\overline{\text{CTS0}}$/ CLKS1	
28		P6_3			TXD0/SDA0	
29		P6_2			RXD0/SCL0	
30		P6_1			CLK0	
31		P6_0		TRHO	$\overline{\text{CTS0}}/\overline{\text{RTS0}}$	
32	CLKOUT	P5_7				
33		P5_6				
34		P5_5				
35		P5_4				
36		P5_3				
37		P5_2				
38		P5_1				
39		P5_0				
40		P4_3				

Table 1.11 Pin Functions for the 100-Pin Package (2/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Main clock input	XIN	I	VCC1	I/O for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. (1) Input an external clock to XIN pin and leave XOUT pin open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. (1) Input an external clock to XCIN pin and leave XCOUT pin open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	Outputs a clock with the same frequency as fC, f1, f8, or f32.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input for the $\overline{\text{INT}}$ interrupt.
	$\overline{\text{INT3}}$ to $\overline{\text{INT7}}$	I	VCC2	
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input for the $\overline{\text{NMI}}$ interrupt.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	VCC1	Input for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O for timers A0 to A4 (TA0OUT is N-channel open drain output).
	TA0IN to TA4IN	I	VCC1	Input for timers A0 to A4.
	ZP	I	VCC1	Input for Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	Input for timers B0 to B5.
Three-phase motor control timer	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	Output for the three-phase motor control timer.
	$\overline{\text{SD}}$	I	VCC1	Forced cutoff input.
	IDU, IDV, IDW	I	VCC2	Input for the position data.
Real-time clock output	TRHO	O	VCC1	Output for the real-time clock.
PWM output	PWM0, PWM1	O	VCC1, VCC2	PWM output.
Remote control signal receiver input	PMC0, PMC1	I	VCC1	Input for the remote control signal receiver.
Serial interface UART0 to UART2, UART5 to UART7	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$, $\overline{\text{CTS5}}$	I	VCC1	Input pins to control data transmission.
	$\overline{\text{CTS6}}$, $\overline{\text{CTS7}}$	I	VCC2	
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$, $\overline{\text{RTS5}}$	O	VCC1	Output pins to control data reception.
	$\overline{\text{RTS6}}$, $\overline{\text{RTS7}}$	O	VCC2	
	CLK0 to CLK2, CLK5	I/O	VCC1	Transmit/receive clock I/O.
	CLK6, CLK7	I/O	VCC2	
	RXD0 to RXD2, RXD5	I	VCC1	Serial data input.
	RXD6, RXD7	I	VCC2	
	TXD0 to TXD2, TXD5	O	VCC1	Serial data output. (2)
	TXD6, TXD7	O	VCC2	
	CLKS1	O	VCC1	Output for the transmit/receive clock multiple-pin output function.

Notes:
1. Contact the manufacturer of crystal/ceramic resonator regarding the oscillation characteristics.
2. TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi, SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins (i = 0, 1, 5 to 7).

Table 1.13 Pin Functions for the 80-Pin Package (1/2)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VSS	I	-	Apply 1.8 to 5.5 V to the VCC1 pin and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{RESET}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor.
Main clock input	XIN	I	VCC1	I/O pins for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. (1) Input an external clock to XIN pin and leave XOUT pin open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. (1) Input an external clock to XCIN pin and leave XCOUT pin open.
Sub clock output	XCOUT	O	VCC1	
Clock output	CLKOUT	O	VCC1	Outputs a clock with the same frequency as fC, f1, f8, or f32.
$\overline{INT}$ interrupt input	$\overline{INT0}$ to $\overline{INT2}$	I	VCC1	Input for the $\overline{INT}$ interrupt.
	$\overline{INT6}$, $\overline{INT7}$	I	VCC1	
$\overline{NMI}$ interrupt input	$\overline{NMI}$	I	VCC1	Input for the $\overline{NMI}$ interrupt.
Key input interrupt input	$\overline{KI0}$ to $\overline{KI7}$	I	VCC1	Input for the key input interrupt.
Timer A	TA0OUT, TA3OUT, TA4OUT	I/O	VCC1	I/O for timers A0, A3, and A4 (TA0OUT is N-channel open drain output).
	TA0IN, TA3IN, TA4IN	I	VCC1	Input for timers A0, A3, and A4.
	ZP	I	VCC1	Input for Z-phase.
Timer B	TB0IN, TB2IN to TB5IN	I	VCC1	Input for timers B0, and B2 to B5.
Real-time clock output	TRHO	O	VCC1	Output for the real-time clock.
PWM output	PWM0, PWM1	O	VCC1	PWM output.
Remote control signal receiver input	PMC0	I	VCC1	Input for the remote control signal receiver.

Note:
1. Contact the manufacturer of crystal/ceramic resonator regarding oscillation characteristics.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	Reset Value
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register CEC1 Interrupt Control Register	U5BCNIC CEC1IC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register CEC2 Interrupt Control Register	S5TIC CEC2IC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART6 Bus Collision Detection Interrupt Control Register Real-Time Clock Periodic Interrupt Control Register	U6BCNIC RTCTIC	XXXX X000b
006Fh	UART6 Transmit Interrupt Control Register Real-Time Clock Alarm Interrupt Control Register	S6TIC RTCCIC	XXXX X000b
0070h	UART6 Receive Interrupt Control Register	S6RIC	XXXX X000b
0071h	UART7 Bus Collision Detection Interrupt Control Register Remote Control Signal Receiver 0 Interrupt Control Register	U7BCNIC PMC0IC	XXXX X000b
0072h	UART7 Transmit Interrupt Control Register Remote Control Signal Receiver 1 Interrupt Control Register	S7TIC PMC1IC	XXXX X000b
0073h	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh	I2C-bus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
007Dh			
007Eh			
007Fh			
0080h to 017Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART7 Special Mode Register 4	U7SMR4	00h
02A5h	UART7 Special Mode Register 3	U7SMR3	000X 0X0Xb
02A6h	UART7 Special Mode Register 2	U7SMR2	X000 0000b
02A7h	UART7 Special Mode Register	U7SMR	X000 0000b
02A8h	UART7 Transmit/Receive Mode Register	U7MR	00h
02A9h	UART7 Bit Rate Register	U7BRG	XXh
02AAh	UART7 Transmit Buffer Register	U7TB	XXh
02ABh			XXh
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	0000 1000b
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	0000 0010b
02AEh	UART7 Receive Buffer Register	U7RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h to 02FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

5.1.5 Flash Memory Electrical Characteristics

Table 5.9 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				10 (1)	MHz
f(SLOW_R)	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC(32.768)	35	kHz
-	Data flash read	3.0 V < V_{CC1} ≤ 5.5 V			20 (2)	MHz

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is 1.8 ≤ V_{CC1} ≤ 3.0 V, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

Table 5.10 Flash Memory (Program ROM 1, 2) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = 0°C to 60°C (option: -40°C to 85°C), unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	1,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		150	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		70	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f(BCLK)}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f(BCLK)}$	µs
-	Program, erase voltage		2.7		5.5	V
-	Read voltage	T_{opr}= -20°C to 85°C/-40°C to 85°C	2.7		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles:
The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

Table 5.11 Flash Memory (Data Flash) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C/-40 to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	10,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		300	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		140	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f(BCLK)}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f(BCLK)}$	µs
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		–20/–40		85	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:

1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

5.1.7 Oscillator Electrical Characteristics

Table 5.17 40 MHz On-Chip Oscillator Electrical Characteristics

V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO40M}	40 MHz on-chip oscillator frequency	Average frequency in a 10 ms period 2.7 V ≤ V_{CC1} < 5.5 V	36	40	44	MHz
		Average frequency in a 10 ms period 1.8 V ≤ V_{CC1} < 2.7 V	30	40	50	MHz
tsu(f_{OCO40M})	Wait time until 40 MHz on-chip oscillator stabilizes				2	ms

Table 5.18 125 kHz On-Chip Oscillator Electrical Characteristics

V_{CC1} = 1.8 to 5.5 V, T_{opr} = −20°C to 85°C/−40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO-S}	125 kHz on-chip oscillator frequency	Average frequency in a 10 ms period	100	125	150	kHz
tsu(f_{OCO-S})	Wait time until 125 kHz on-chip oscillator stabilizes				20	µs

5.2 Electrical Characteristics ($V_{CC1} = V_{CC2} = 5$ V)

5.2.1 Electrical Characteristics

$V_{CC1} = V_{CC2} = 5$ V

Table 5.19 Electrical Characteristics (1) [(1)]

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20$°C to 85°C/–40°C to 85°C, $f_{(BCLK)} = 20$ MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OH} = -5$ mA	$V_{CC1} - 2.0$		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OH} = -5$ mA	$V_{CC2} - 2.0$		V_{CC2}	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OH} = -200$ µA	$V_{CC1} - 0.3$		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OH} = -200$ µA	$V_{CC2} - 0.3$		V_{CC2}	
V_{OH}	High output voltage XOUT	HIGHPOWER	$I_{OH} = -1$ mA	$V_{CC1} - 2.0$		V_{CC1}	V
		LOWPOWER	$I_{OH} = -0.5$ mA	$V_{CC1} - 2.0$		V_{CC1}	
	High output voltage XCOUT		With no load applied		1.5		V
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OL} = 5$ mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OL} = 5$ mA			2.0	
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	$I_{OL} = 200$ µA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$I_{OL} = 200$ µA			0.45	
V_{OL}	Low output voltage XOUT	HIGHPOWER	$I_{OL} = 1$ mA			2.0	V
		LOWPOWER	$I_{OL} = 0.5$ mA			2.0	
	Low output voltage XCOUT		With no load applied		0		V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V, 3 V, or 1.8 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5$ V

Timing Requirements
($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

Table 5.28 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

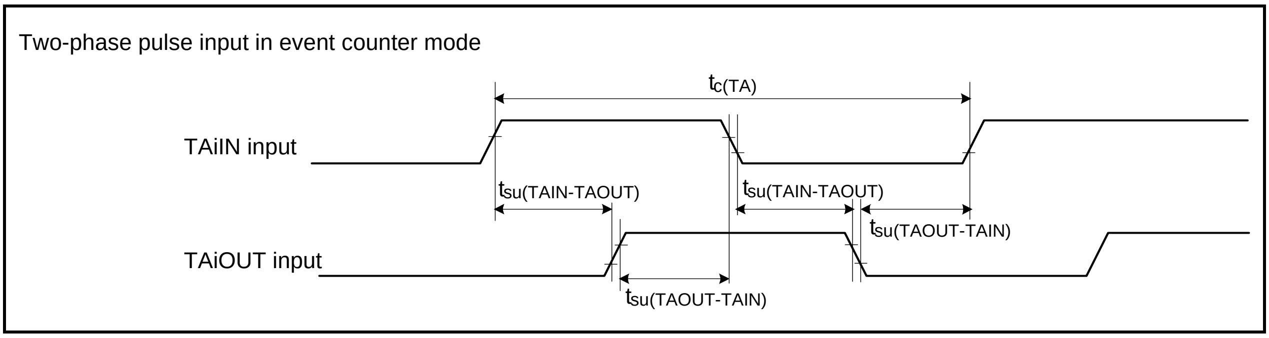


Figure 5.9 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

$V_{CC1} = V_{CC2} = 5$ V

5.2.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.1 In No Wait State Setting

Table 5.36 Memory Expansion Mode and Microprocessor Mode (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.15		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

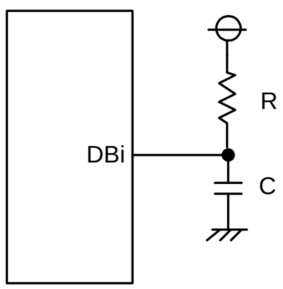
1. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$ $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

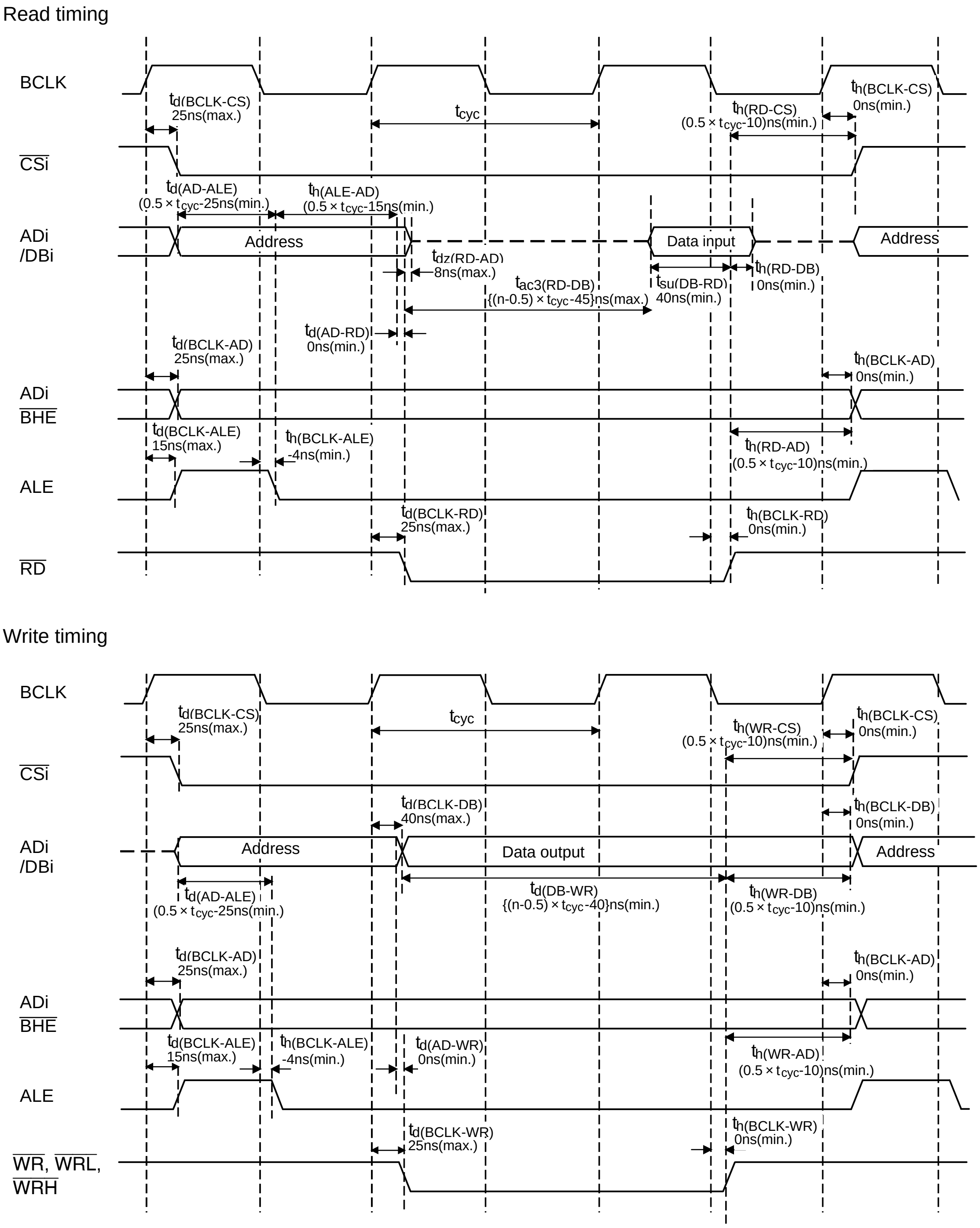
   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
   $t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
   $= 6.7$ ns.



Memory Expansion Mode and Microprocessor Mode
(in 2 or 3 waits setting, and when accessing external area and using multiplexed bus)

$V_{CC1} = V_{CC2} = 5V$



Measuring conditions

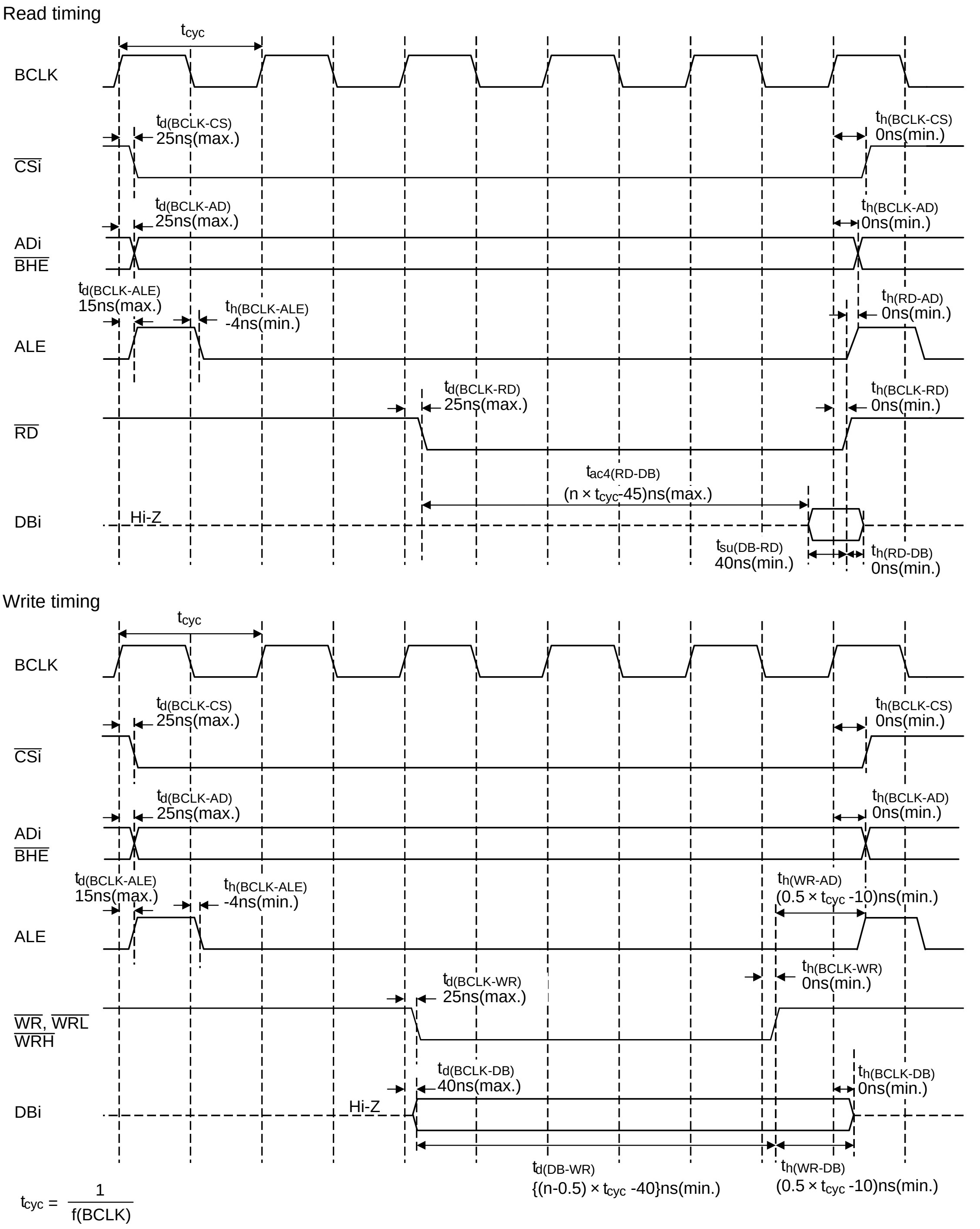
- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

n: 2 (when 2 waits)
3 (when 3 waits)

Figure 5.18 Timing Diagram

Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 φ + 3 φ, 2 φ + 4 φ, 3φ + 4 φ, and 4 φ + 5 φ, and when accessing external area)

$V_{CC1} = V_{CC2} = 5V$



$t_{cyc} = \frac{1}{f(BCLK)}$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

n: 3 (when 2 φ + 3 φ)
4 (when 2 φ + 4 φ or 3 φ + 4 φ)
5 (when 4 φ + 5 φ)

Figure 5.19 Timing Diagram

$V_{CC1} = V_{CC2} = 3$ V

Timing Requirements
($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.3 Timer A Input

Table 5.45 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

Table 5.46 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

Table 5.47 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

Table 5.48 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

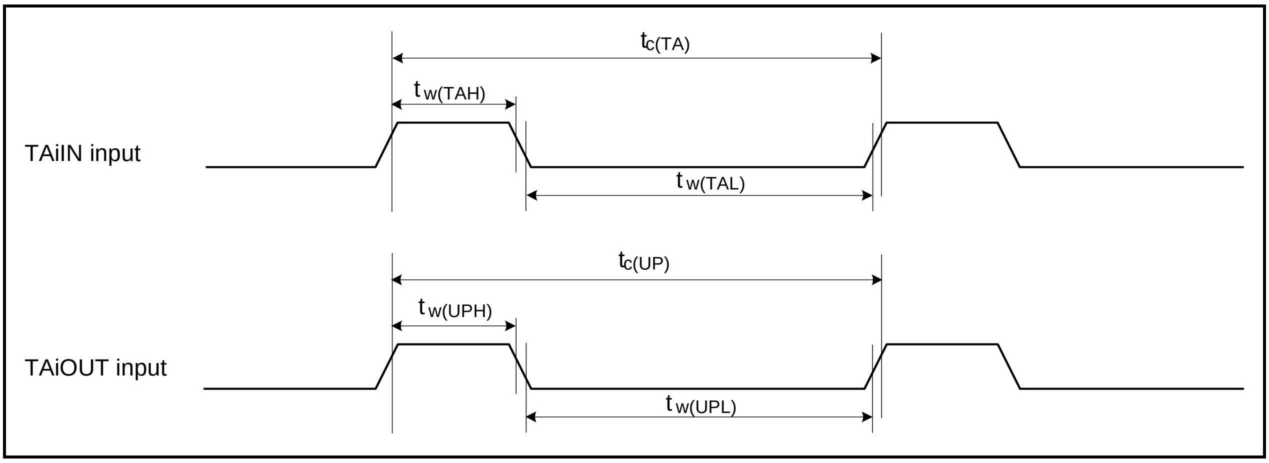


Figure 5.23 Timer A Input

$V_{CC1} = V_{CC2} = 3$ V

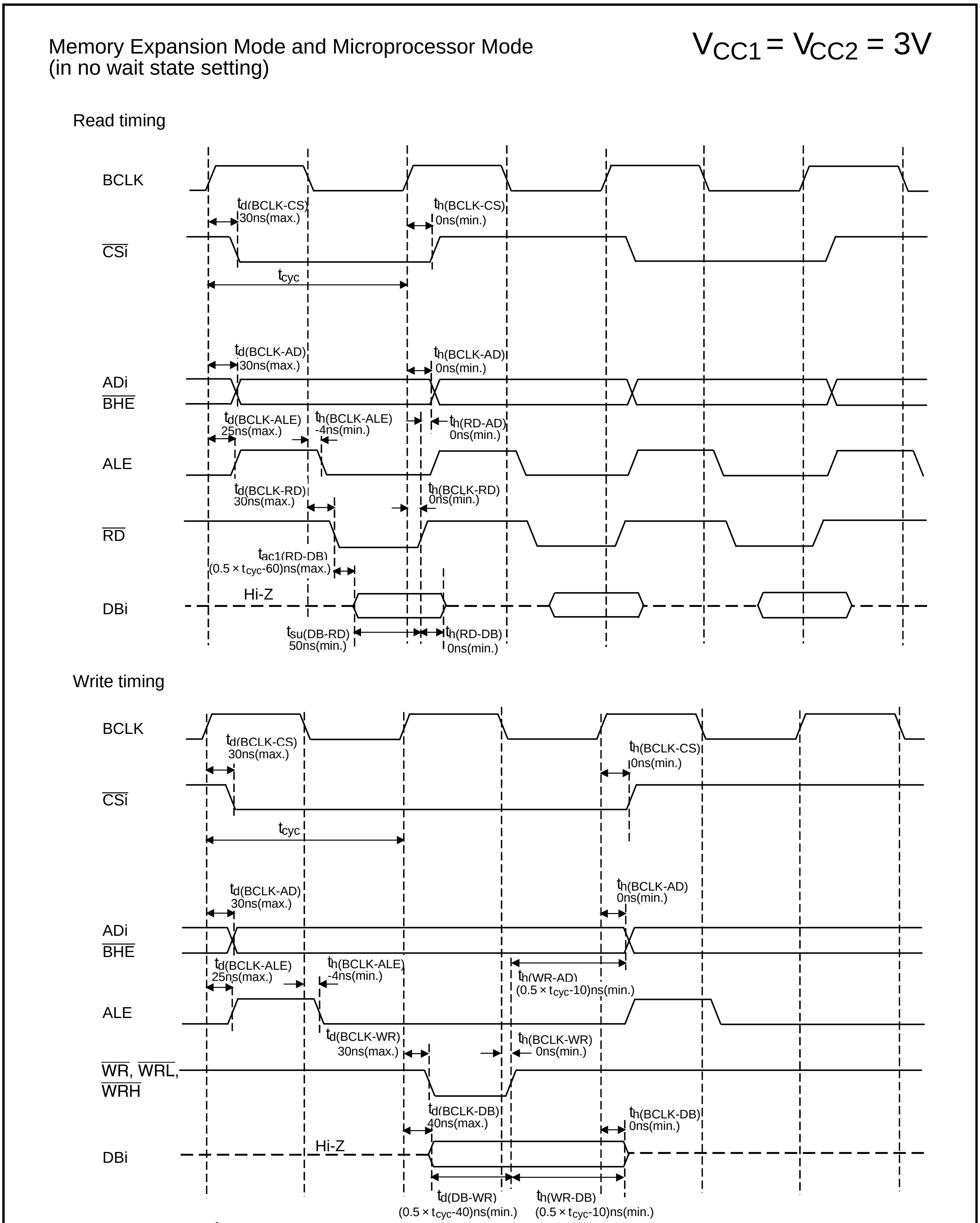
Timing Requirements
($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

Table 5.56 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{ac4(RD-DB)}$	Data input access time (for setting with 2 φ + 3 φ or more)		(Note 4)	ns
$t_{su(DB-RD)}$	Data input setup time	50		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	85		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns

Notes:
1. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 60[ns]$$
2. Calculated according to the BCLK frequency as follows:
$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns]$$
n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
3. Calculated according to the BCLK frequency as follows:
$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns]$$
n is 2 for 2 waits setting, 3 for 3 waits setting.
4. Calculated according to the BCLK frequency as follows:
$$\frac{n \times 10^9}{f_{(BCLK)}} - 60[ns]$$
n is 3 for 2 φ + 3 φ, 4 for 2 φ + 4 φ, 4 for 3 φ + 4 φ, 5 for 4 φ + 5 φ,.



$t_{cyc} = \frac{1}{f_{(BCLK)}}$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

Figure 5.31 Timing Diagram

$V_{CC1} = V_{CC2} = 3$ V

Switching Characteristics

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.2 In 1 to 3 Waits Setting and When Accessing External Area

Table 5.58 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.30		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.