Renesas Electronics America Inc - R5F363AENFA#U0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f363aenfa-u0

1.2 Specifications

The M16C/63 Group includes 100-pin and 80-pin packages. Table 1.1 to Table 1.4 list specifications.

Table 1.1 Specifications for the 100-Pin Package (1/2)

Item	Function	Description
CPU	Central processing unit	M16C/60 Series core (multiplier: 16 bit × 16 bit → 32 bit, multiply and accumulate instruction: 16 bit × 16 bit + 32 bit → 32 bit) • Number of basic instructions: 91 • Minimum instruction execution time: 50.0 ns (f(BCLK) = 20 MHz, VCC1 = VCC2 = 2.7 to 5.5 V) 100.0 ns (f(BCLK) = 10 MHz, VCC1 = VCC2 = 2.1 to below 2.7 V) 200.0 ns (f(BCLK) = 5 MHz, VCC1 = VCC2 = 1.8 V) • Operating modes: Single-chip, memory expansion, and microprocessor
Memory	ROM, RAM, data flash	See Table 1.5 “Product List”.
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
Clock	Clock generator	• 4 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ±10%) • Oscillation stop detection: Main clock oscillation stop/restart detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 Sub clock frequency divider circuit: Divide ratio selectable from 1 and 2 • Power saving features: Wait mode, stop mode • Real-time clock
External Bus Expansion	Bus memory expansion	• Address space: 1 MB • External bus interface: 0 to 8 waits inserted, 4 chip select outputs, memory area expansion function (expandable to 4 MB), 3 V and 5 V interfaces • Bus format: Separate bus or multiplexed bus selectable, data bus width selectable (8 or 16 bits), number of address buses selectable (12, 16, or 20)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 85 (selectable pull-up resistors) • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 17 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 8, key input × 8) • Interrupt priority levels: 7
Watchdog Timer		15-bit timer × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)

Table 1.3 Specifications for the 80-Pin Package (1/2)

Item	Function	Description
CPU	Central processing unit	M16C/60 Series core (multiplier: 16 bit × 16 bit → 32 bit, multiply and accumulate instruction: 16 bit × 16 bit + 32 bit → 32 bit) • Number of basic instructions: 91 • Minimum instruction execution time: 50.0 ns (f(BCLK) = 20 MHz, VCC1 = 2.7 to 5.5 V) 100.0 ns (f(BCLK) = 10 MHz, VCC1 = 2.1 to below 2.7 V) 200.0 ns (f(BCLK) = 5 MHz, VCC1 = 1.8 V) • Operating mode: Single-chip
Memory	ROM, RAM, data flash	See Table 1.5 “Product List”.
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
Clock	Clock generator	• 4 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ±10%) • Oscillation stop detection: Main clock oscillation stop/restart detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 Sub clock frequency divider circuit: Divide ratio selectable from 1 and 2 • Power saving features: Wait mode, stop mode • Real-time clock
External Bus Expansion	Bus memory expansion	None
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 68 (selectable pull-up resistors) • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 14 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 5, key input × 8) • Interrupt priority levels: 7
Watchdog Timer		15-bit timer × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)

Table 1.4 Specifications for the 80-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode × 5 Event counter mode, one-shot timer mode, pulse width modulation (PWM) mode × 3 Event counter two-phase pulse signal processing (two-phase encoder input) × 2 Programmable output mode × 1
	Timer B	16-bit timer × 6 Timer mode × 6 Event counter mode, pulse period measurement mode, pulse width measurement mode × 5
	Three-phase motor control timer functions	None
	Real-time clock	• Count: seconds, minutes, hours, days of the week, months, years • Periodic interrupt: 0.25 s, 0.5 s • Automatic correction function
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5	Clock synchronous/asynchronous × 3 channels I^2C-bus, IEBus, special mode 2 Clock asynchronous × 1 channel I^2C-bus, IEBus, SIM
	SI/O3, SI/O4	Clock synchronization only × 2 channels (SI/O3 is used for transmission only)
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 2.15 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		5 MHz/VCC1 = 1.8 to 5.5 V 10 MHz/VCC1 = 2.1 to 5.5 V 20 MHz/VCC1 = 2.7 to 5.5 V
Current Consumption		Described in Electrical Characteristics
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		80-pin LQFP: PLQP0080KB-A (Previous package code: 80P6Q-A)

Notes:
1. See Table 1.5 “Product List” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

1.3 Product List

Table 1.5 lists product information. Figure 1.1 shows the Part No., with Memory Size and Package, and Figure 1.2 and Figure 1.3 shows the Marking Diagram (Top View).

Table 1.5 Product List As of November, 2012

Part No.	ROM Capacity			RAM Capacity	Package Code	Remarks
	Program ROM 1	Program ROM 2	Data flash			
R5F363A6NFA	128 KB	16 KB	4 KB × 2 blocks	12 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F363A6NFB					PLQP0100KB-A	
R5F363A6NLG					PTLG0100KA-A	
R5F363B6NFE					PLQP0080KB-A	
R5F363A6DFA					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F363A6DFB					PLQP0100KB-A	
R5F363B6DFE					PLQP0080KB-A	
R5F363AENFA	256 KB	16 KB	4 KB × 2 blocks	20 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F363AENFB					PLQP0100KB-A	
R5F363AENLG					PTLG0100KA-A	
R5F363BENFE					PLQP0080KB-A	
R5F363AEDFA					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F363AEDFB					PLQP0100KB-A	
R5F363BEDFE					PLQP0080KB-A	
R5F363AKNFA	384 KB	16 KB	4 KB × 2 blocks	31 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F363AKNFB					PLQP0100KB-A	
R5F363AKNLG					PTLG0100KA-A	
R5F363AKDFA					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F363AKDFB					PLQP0100KB-A	
R5F363AMNFA	512 KB	16 KB	4 KB × 2 blocks	31 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F363AMNFB					PLQP0100KB-A	
R5F363AMNLG					PTLG0100KA-A	
R5F363AMDFA					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F363AMDFB					PLQP0100KB-A	

(D): Under development
(P): Planning

Previous package codes are as follows:
PRQP0100JD-B: 100P6F-A
PLQP0100KB-A: 100P6Q-A
PTLG0100KA-A: 100F0M
PLQP0080KB-A: 80P6Q-A

Table 1.6 Pin Names for the 100-Pin Package (1/2)

Pin No.			Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB	LG			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	99	B2		P9_6			SOUT4	ANEX1	
2	100	A2		P9_5			CLK4	ANEX0	
3	1	A1		P9_4		TB4IN/PWM1		DA1	
4	2	E4		P9_3		TB3IN/PWM0		DA0	
5	3	B1		P9_2		TB2IN/PMC0	SOUT3		
6	4	D3		P9_1		TB1IN/PMC1	SIN3		
7	5	C2		P9_0		TB0IN	CLK3		
8	6	C1	BYTE						
9	7	D2	CNVSS						
10	8	D1	XCIN	P8_7					
11	9	E3	XCOUT	P8_6					
12	10	E2	$\overline{\text{RESET}}$						
13	11	E1	XOUT						
14	12	F3	VSS						
15	13	F2	XIN						
16	14	F1	VCC1						
17	15	G2		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$	CEC		
18	16	F5		P8_4	$\overline{\text{INT2}}$	ZP			
19	17	G3		P8_3	$\overline{\text{INT1}}$				
20	18	G1		P8_2	$\overline{\text{INT0}}$				
21	19	F4		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$		
22	20	H1		P8_0		TA4OUT/U	RXD5/SCL5		
23	21	H2		P7_7		TA3IN	CLK5		
24	22	G4		P7_6		TA3OUT	TXD5/SDA5		
25	23	H3		P7_5		TA2IN/$\overline{\text{W}}$			
26	24	J1		P7_4		TA2OUT/W			
27	25	J2		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$		
28	26	K1		P7_2		TA1OUT/V	CLK2		
29	27	K2		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
30	28	J3		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
31	29	H4		P6_7			TXD1/SDA1		
32	30	K3		P6_6			RXD1/SCL1		
33	31	G5		P6_5			CLK1		
34	32	J4		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/ CLKS1		
35	33	K4		P6_3			TXD0/SDA0		
36	34	H5		P6_2			RXD0/SCL0		
37	35	J5		P6_1			CLK0		
38	36	K5		P6_0		TRHO	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
39	37	G6	CLKOUT	P5_7					$\overline{\text{RDY}}$
40	38	H6		P5_6					ALE
41	39	J6		P5_5					$\overline{\text{HOLD}}$
42	40	K6		P5_4					$\overline{\text{HLDA}}$
43	41	H7		P5_3					BCLK
44	42	J7		P5_2					$\overline{\text{RD}}$
45	43	K7		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
46	44	K8		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
47	45	G7		P4_7		PWM1	TXD7/SDA7		$\overline{\text{CS3}}$
48	46	J8		P4_6		PWM0	RXD7/SCL7		$\overline{\text{CS2}}$
49	47	H8		P4_5			CLK7		$\overline{\text{CS1}}$
50	48	G8		P4_4			$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$		$\overline{\text{CS0}}$

Table 1.8 Pin Names for the 80-Pin Package (1/2)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function			
			Interrupt	Timer	Serial interface	A/D converter, D/A converter
1		P9_5			CLK4	ANEX0
2		P9_4		TB4IN/PWM1		DA1
3		P9_3		TB3IN/PWM0		DA0
4		P9_2		TB2IN/PMC0	SOUT3	
5		P9_0		TB0IN	CLK3	
6	CNVSS					
7	XCIN	P8_7				
8	XCOUT	P8_6				
9	$\overline{\text{RESET}}$					
10	XOUT					
11	VSS					
12	XIN					
13	VCC1					
14		P8_5	$\overline{\text{NMI}}$		CEC	
15		P8_4	$\overline{\text{INT2}}$	ZP		
16		P8_3	$\overline{\text{INT1}}$			
17		P8_2	$\overline{\text{INT0}}$			
18		P8_1		TA4IN	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	
19		P8_0		TA4OUT	RXD5/SCL5	
20		P7_7		TA3IN	CLK5	
21		P7_6		TA3OUT	TXD5/SDA5	
22		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM	
23		P7_0		TA0OUT	TXD2/SDA2/SDAMM	
24		P6_7			TXD1/SDA1	
25		P6_6			RXD1/SCL1	
26		P6_5			CLK1	
27		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/ CLKS1	
28		P6_3			TXD0/SDA0	
29		P6_2			RXD0/SCL0	
30		P6_1			CLK0	
31		P6_0		TRHO	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	
32	CLKOUT	P5_7				
33		P5_6				
34		P5_5				
35		P5_4				
36		P5_3				
37		P5_2				
38		P5_1				
39		P5_0				
40		P4_3				

2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.
Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.
The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.
If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

2.8.10 Reserved Areas

Only set these bits to 0. The read value is undefined.

Table 5.4 Recommended Operating Conditions (3/4)

V_{CC1} = V_{CC2} = 1.8 to 5.5 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
$I_{OL(sum)}$	Low peak output current (100-pin package)	V_{CC1}, V_{CC2} ≥ 2.7 V	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			80.0	mA
			Sum of $I_{OL(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_5			80.0	mA
		V_{CC1}, V_{CC2} < 2.7 V	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
			Sum of $I_{OL(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_5			10.0	mA
	Low peak output current (80-pin package)	V_{CC1}, V_{CC2} ≥ 2.7 V	Sum of all ports			80.0	mA
		V_{CC1}, V_{CC2} < 2.7 V	Sum of all ports			10.0	mA
$I_{OL(peak)}$	Low peak output current	V_{CC1}, V_{CC2} ≥ 2.7	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
		V_{CC1}, V_{CC2} < 2.7 V	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			1.0	mA
$I_{OL(avg)}$	Low average output current (1)	V_{CC1}, V_{CC2} ≥ 2.7 V	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			5.0	mA
		V_{CC1}, V_{CC2} < 2.7 V	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			0.5	mA
$f_{(XIN)}$	Main clock input oscillation frequency		2.7 V ≤ V_{CC1} ≤ 5.5 V	1		20	MHz
			1.8 V ≤ V_{CC1} < 2.7 V	1		10	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency				32.768		kHz
$f_{(BCLK)}$	CPU operation clock		2.7 V ≤ V_{CC1} ≤ 5.5 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 20 MHz			20	MHz
			2.1 V ≤ V_{CC1} < 2.7 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 10 MHz			10	MHz
			1.8 V ≤ V_{CC1} < 2.1 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 10 MHz			(Note 2)	MHz

Notes:
1. The average output current is the mean value within 100 ms.
2. Calculated by the following equation according to V_{CC1}: $16.67 \times V_{CC1} - 25$ [MHz]

   See Figure 5.1 “Relation between $f_{(BCLK)}$ and V_{CC1}”

Table 5.16 Power Supply Circuit Timing Characteristics

The measurement condition is V_{CC1} = 1.8 to 5.5 V and T_{opr} = 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply stability time when power is on (1)				5	ms
$t_{d(R-S)}$	STOP release time				150	µs
$t_{d(W-S)}$	Low power mode wait mode release time				150	µs

Note:
1. Waiting time until the internal power supply generator stabilizes when power is on.

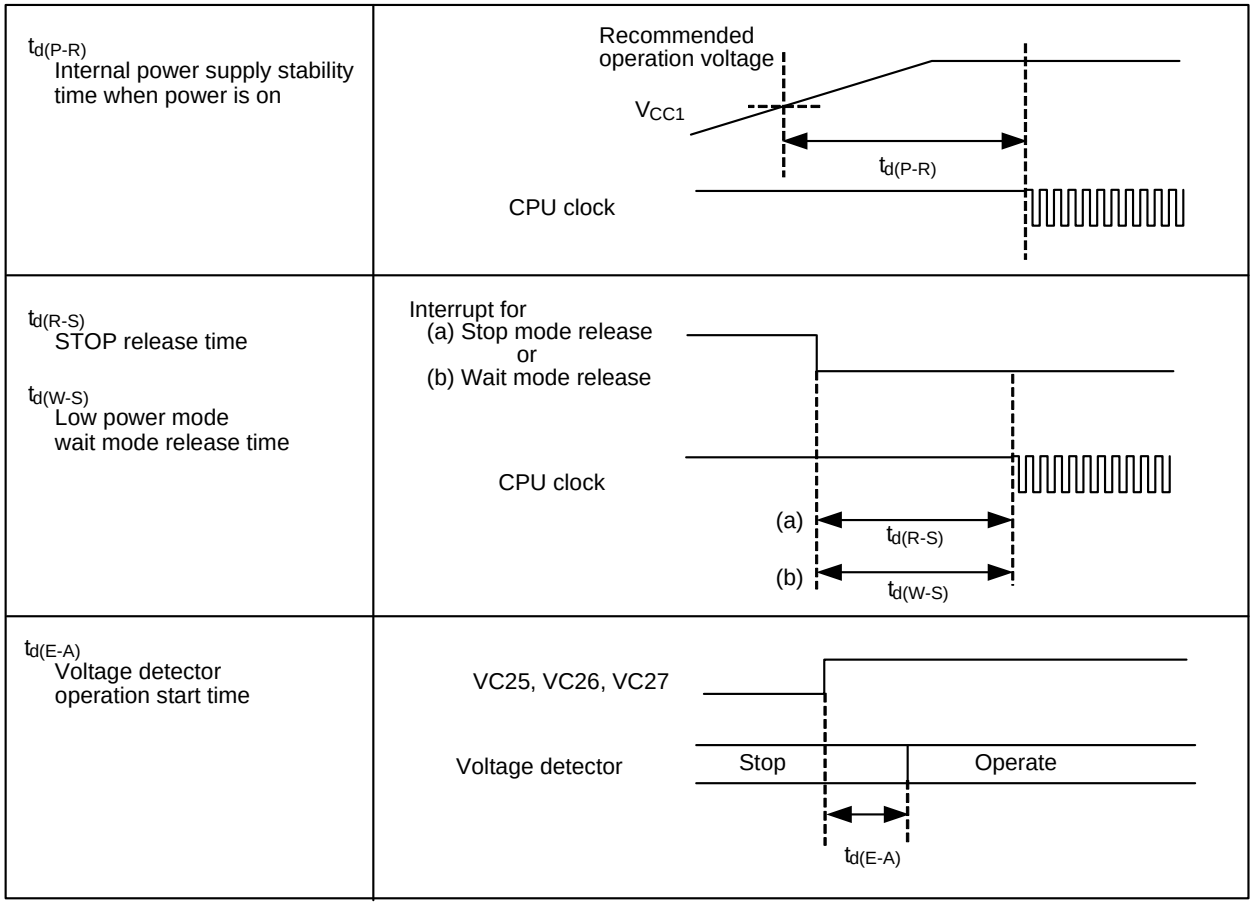


Figure 5.5 Power Supply Circuit Timing Diagram

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.5 Serial Interface

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high pulse width	100		ns
$t_{w(CKL)}$	CLKi input low pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

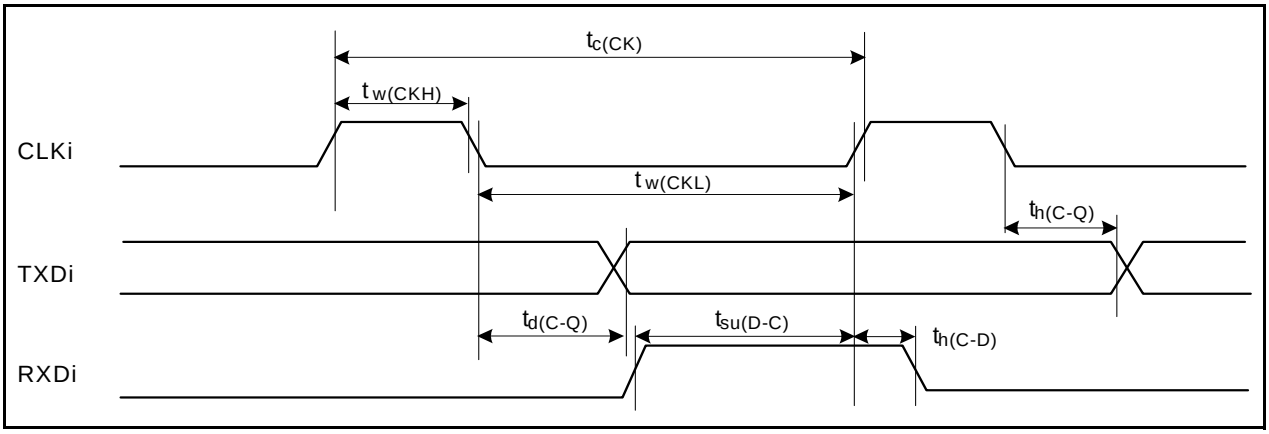


Figure 5.11 Serial Interface

5.2.2.6 External Interrupt $\overline{INTi}$ Input

Table 5.33 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	250		ns

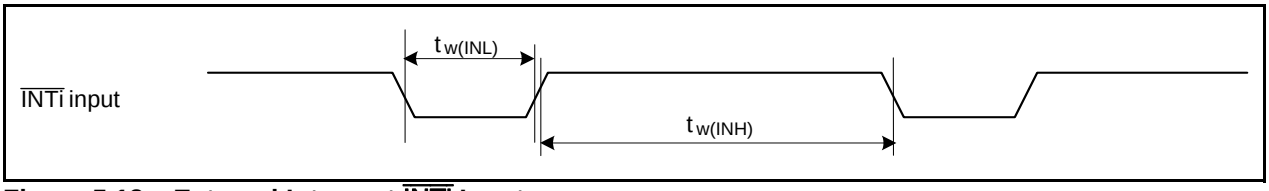
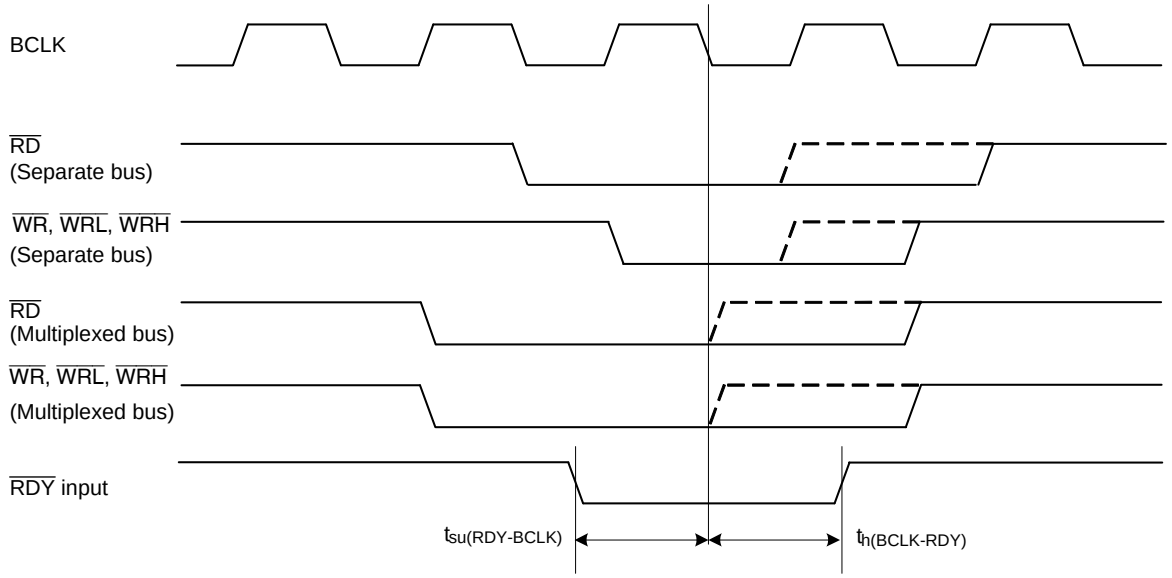


Figure 5.12 External Interrupt $\overline{INTi}$ Input

Memory Expansion Mode and Microprocessor Mode

$V_{CC1} = V_{CC2} = 5\ V$

(Effective in wait state setting**)**



Measuring conditions

- $V_{CC1} = V_{CC2} = 5\ V$
- Input timing voltage: $V_{IL} = 1.0\ V$, $V_{IH} = 4.0\ V$
- Output timing voltage: $V_{OL} = 2.5\ V$, $V_{OH} = 2.5\ V$

Figure 5.14 Timing Diagram

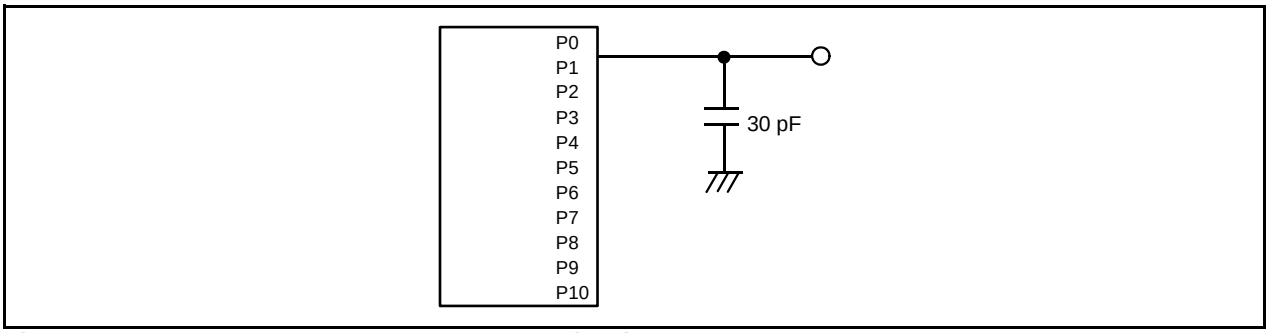


Figure 5.15 Ports P0 to P10 Measurement Circuit

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.4 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area

Table 5.39 Memory Expansion Mode and Microprocessor Mode (in Wait State Setting 2 φ + 3 φ, 2 φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.15		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

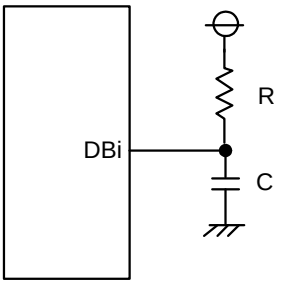
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

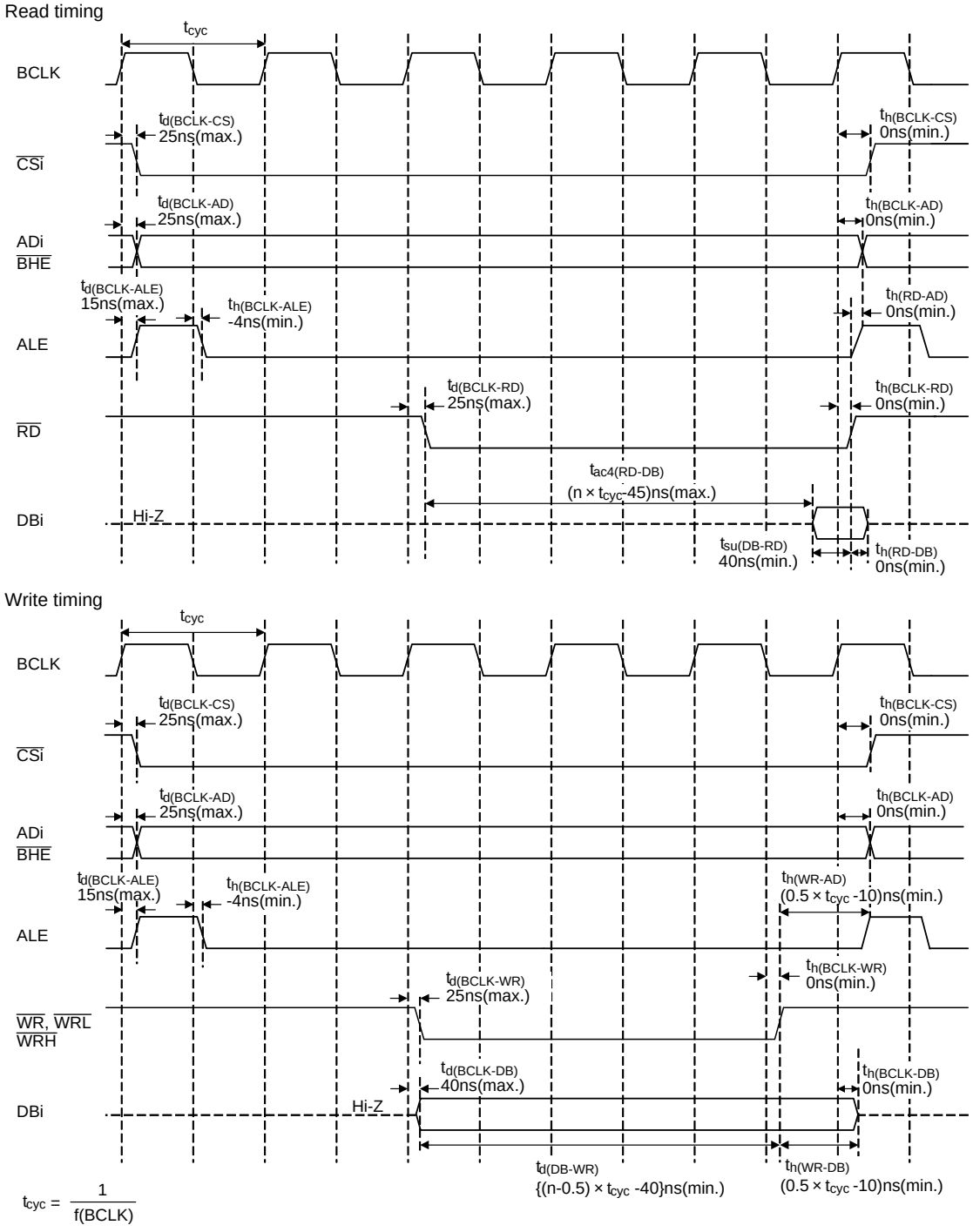
$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 5V$



$t_{cyc} = \frac{1}{f(BCLK)}$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage: V_{OL} = 0.4 V, V_{OH} = 2.4 V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

Figure 5.19 Timing Diagram

5.3 Electrical Characteristics (V_{CC1} = V_{CC2} = 3 V)

5.3.1 Electrical Characteristics

V_{CC1} = V_{CC2} = 3 V

Table 5.41 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 2.7 to 3.3 V, V_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C, $f_{(BCLK)}$ = 20 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –1 mA	V_{CC1} – 0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –1 mA	V_{CC2} – 0.5		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGHPOWER	I_{OH} = –0.1 mA	V_{CC1} – 0.5		V_{CC1}	V
			LOWPOWER	I_{OH} = –50 µA	V_{CC1} – 0.5		V_{CC1}	
	High output voltage XCOUT			With no load applied		1.5		V
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 1 mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 1 mA			0.5	
		CEC		I_{OL} = 1 mA		0	0.5	V
V_{OL}	Low output voltage XOUT		HIGHPOWER	I_{OL} = 0.1 mA			0.5	V
			LOWPOWER	I_{OL} = 50 µA			0.5	
	Low output voltage XCOUT			With no load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$ to $\overline{CTS7}$, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI7}$, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{SD}$, PMC0, PMC1, SCLMM, SDAMM, ZP, IDU, IDV, IDW			0.2		1.0	V
		CEC			0.2	0.5	1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 3 V			4.0	µA
–	Leakage current in powered-off state		CEC	V_{CC1} = 0 V			1.8	µA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 0 V			–4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		V_I = 0 V	50	100	500	kΩ
R_{fXIN}	Feedback resistance XIN					0.8		MΩ
R_{fXCIN}	Feedback resistance XCIN					8		MΩ
V_{RAM}	RAM retention voltage			In stop mode	1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V, 3 V, or 1.8 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 3\ V$

5.3.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.43 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

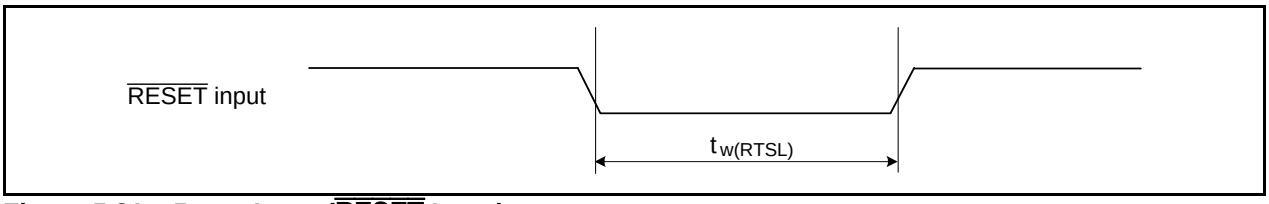


Figure 5.21 Reset Input ($\overline{\text{RESET}}$ Input)

5.3.2.2 External Clock Input

Table 5.44 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 2.7$ to 3.0 V.

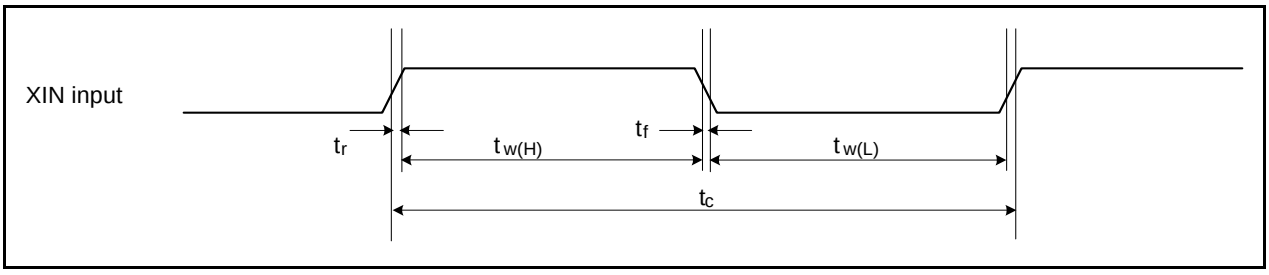
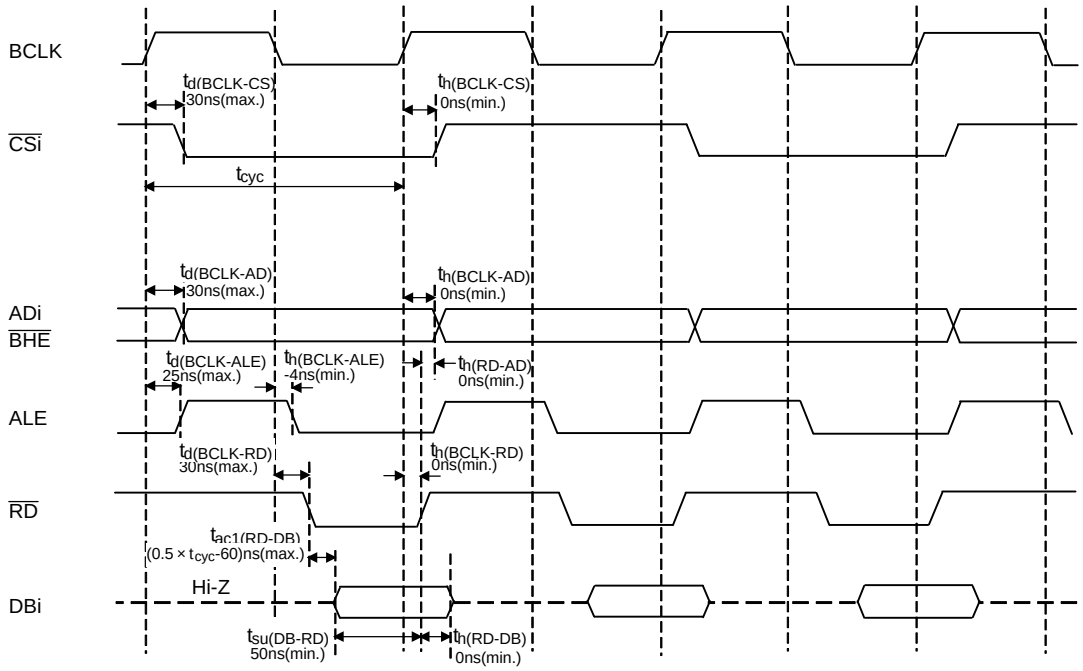


Figure 5.22 External Clock Input (XIN Input)

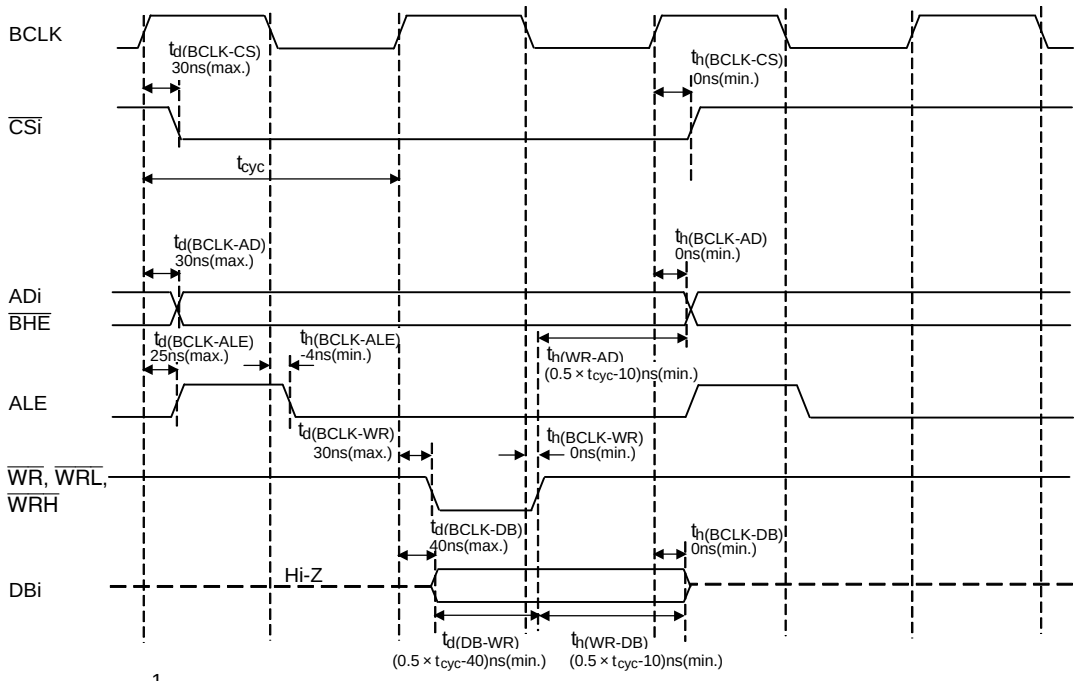
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$V_{CC1} = V_{CC2} = 3V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

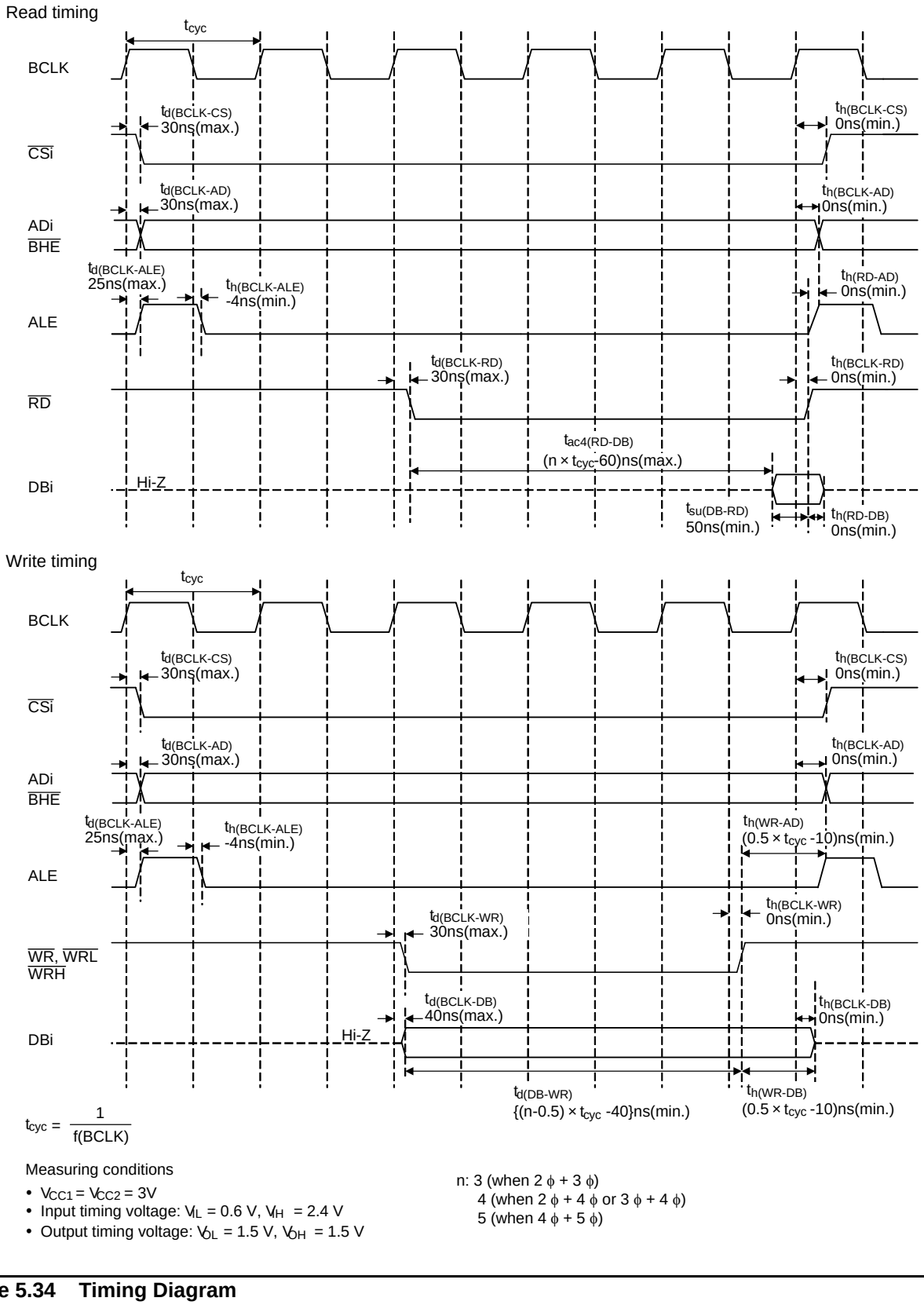
Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

Figure 5.31 Timing Diagram

Memory Expansion Mode, Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$



$t_{cyc} = \frac{1}{f(BCLK)}$

Measuring conditions

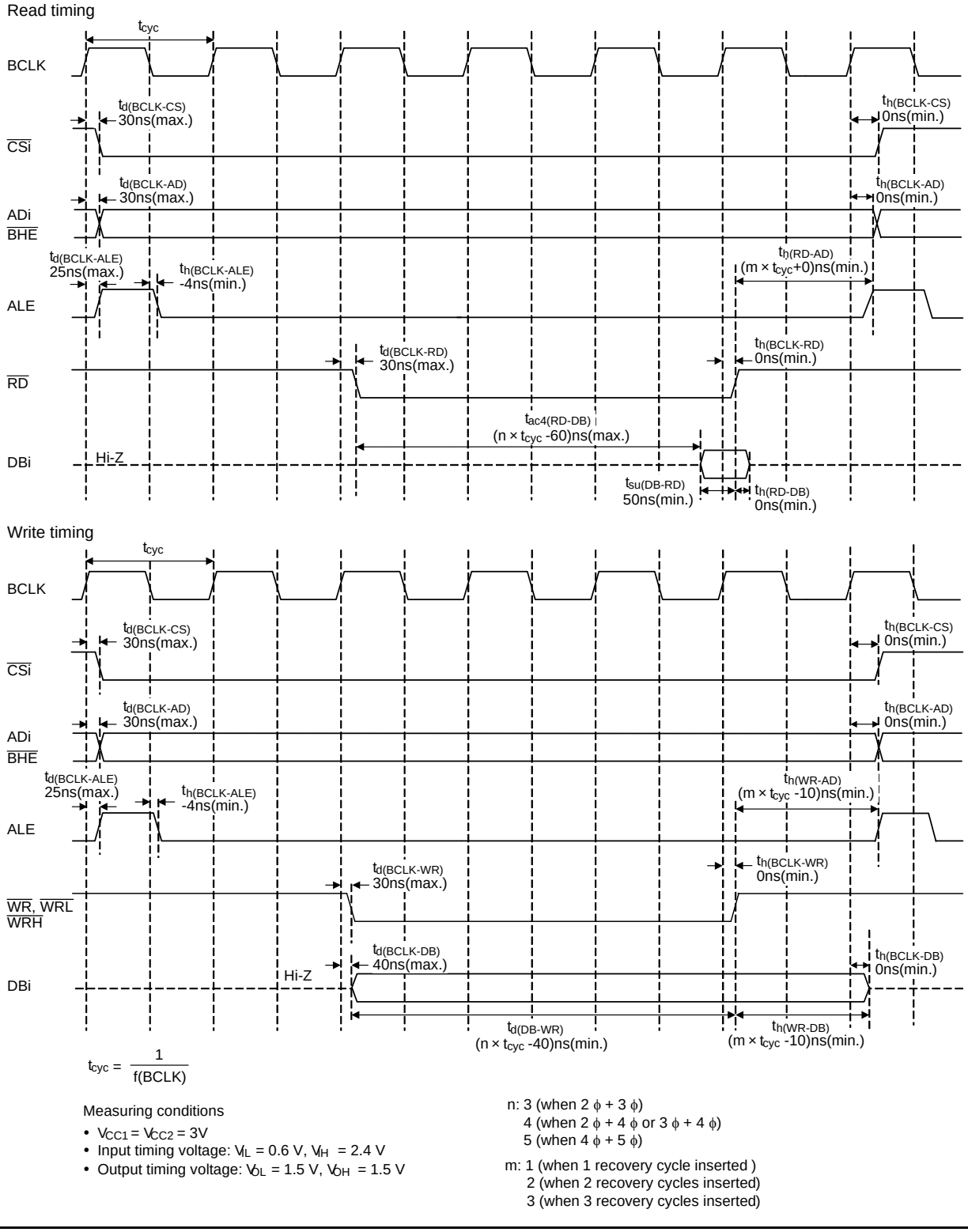
- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

Figure 5.34 Timing Diagram

Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and
when inserting 1 to 3 recovery cycles inserted and accessing external area)

$V_{CC1} = V_{CC2} = 3V$



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

m: 1 (when 1 recovery cycle inserted)
2 (when 2 recovery cycles inserted)
3 (when 3 recovery cycles inserted)

Figure 5.35 Timing Diagram

5.4 Electrical Characteristics (V_{CC1} = V_{CC2} = 1.8 V)

5.4.1 Electrical Characteristics

V_{CC1} = V_{CC2} = 1.8 V

Table 5.62 Electrical Characteristics (1) (1)

1.8 V ≤ V_{CC1} = V_{CC2} < 2.7 V, V_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C, $f_{(BCLK)}$ = 5 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –1 mA	V_{CC1} – 0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –1 mA	V_{CC2} – 0.5		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGHPOWER	I_{OH} = –0.1 mA	V_{CC1} – 0.5		V_{CC1}	V
			LOWPOWER	I_{OH} = –50 µA	V_{CC1} – 0.5		V_{CC1}	
	High output voltage XCOUT			With no load applied		1.5		V
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 1 mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 1 mA			0.5	
V_{OL}	Low output voltage XOUT		HIGHPOWER	I_{OL} = 0.1 mA			0.5	V
			LOWPOWER	I_{OL} = 50 µA			0.5	
	Low output voltage XCOUT			With no load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$ to $\overline{CTS7}$, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI7}$, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{SD}$, PMC0, PMC1, SCLMM, SDAMM, CEC		V_{CC1} = V_{CC2} = 1.8 V	0.02		0.1	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		V_{CC1} = V_{CC2} = 1.8 V	0.05		0.15	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 1.8 V			2.0	µA

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V, 3 V, or 1.8 V standard depending on the voltage.