Renesas Electronics America Inc - R5F363AKDFA#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f363akdfa-u0

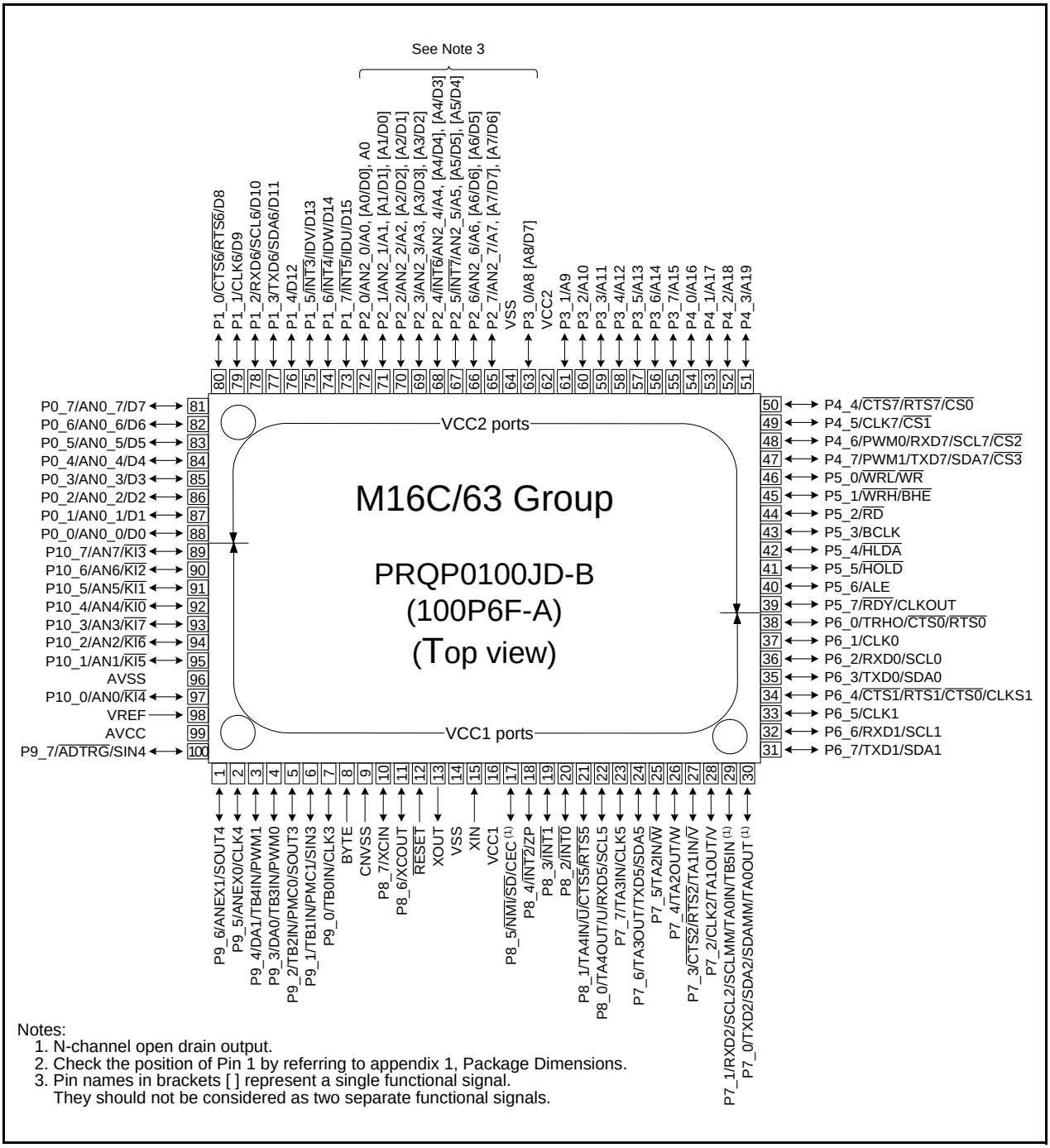
Table 1.4 Specifications for the 80-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode × 5 Event counter mode, one-shot timer mode, pulse width modulation (PWM) mode × 3 Event counter two-phase pulse signal processing (two-phase encoder input) × 2 Programmable output mode × 1
	Timer B	16-bit timer × 6 Timer mode × 6 Event counter mode, pulse period measurement mode, pulse width measurement mode × 5
	Three-phase motor control timer functions	None
	Real-time clock	• Count: seconds, minutes, hours, days of the week, months, years • Periodic interrupt: 0.25 s, 0.5 s • Automatic correction function
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5	Clock synchronous/asynchronous × 3 channels I^2C-bus, IEBus, special mode 2 Clock asynchronous × 1 channel I^2C-bus, IEBus, SIM
	SI/O3, SI/O4	Clock synchronization only × 2 channels (SI/O3 is used for transmission only)
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 2.15 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		5 MHz/VCC1 = 1.8 to 5.5 V 10 MHz/VCC1 = 2.1 to 5.5 V 20 MHz/VCC1 = 2.7 to 5.5 V
Current Consumption		Described in Electrical Characteristics
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		80-pin LQFP: PLQP0080KB-A (Previous package code: 80P6Q-A)

Notes:
1. See Table 1.5 “Product List” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

1.5 Pin Assignments

Figure 1.6 to Figure 1.9 show pin assignments. Table 1.6 to Table 1.9 list pin names.



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

Figure 1.6 Pin Assignment for the 100-Pin Package

Table 1.7 Pin Names for the 100-Pin Package (2/2)

Pin No.			Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB	LG			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
51	49	K9		P4_3					A19
52	50	K10		P4_2					A18
53	51	J10		P4_1					A17
54	52	J9		P4_0					A16
55	53	H9		P3_7					A15
56	54	H10		P3_6					A14
57	55	F6		P3_5					A13
58	56	F7		P3_4					A12
59	57	G9		P3_3					A11
60	58	G10		P3_2					A10
61	59	F8		P3_1					A9
62	60	F9	VCC2						
63	61	F10		P3_0					A8, [A8/D7]
64	62	E8	VSS						
65	63	E9		P2_7				AN2_7	A7, [A7/D7], [A7/D6]
66	64	E10		P2_6				AN2_6	A6, [A6/D6], [A6/D5]
67	65	E7		P2_5	$\overline{INT7}$			AN2_5	A5, [A5/D5], [A5/D4]
68	66	D7		P2_4	$\overline{INT6}$			AN2_4	A4, [A4/D4], [A4/D3]
69	67	D8		P2_3				AN2_3	A3, [A3/D3], [A3/D2]
70	68	D10		P2_2				AN2_2	A2, [A2/D2], [A2/D1]
71	69	D9		P2_1				AN2_1	A1, [A1/D1], [A1/D0]
72	70	C10		P2_0				AN2_0	A0, [A0/D0], A0
73	71	C9		P1_7	$\overline{INT5}$	IDU			D15
74	72	E6		P1_6	$\overline{INT4}$	IDW			D14
75	73	B9		P1_5	$\overline{INT3}$	IDV			D13
76	74	B10		P1_4					D12
77	75	A10		P1_3			TXD6/SDA6		D11
78	76	A9		P1_2			RXD6/SCL6		D10
79	77	C8		P1_1			CLK6		D9
80	78	C7		P1_0			$\overline{CTS6}/\overline{RTS6}$		D8
81	79	A8		P0_7				AN0_7	D7
82	80	B8		P0_6				AN0_6	D6
83	81	D6		P0_5				AN0_5	D5
84	82	B7		P0_4				AN0_4	D4
85	83	A7		P0_3				AN0_3	D3
86	84	B6		P0_2				AN0_2	D2
87	85	C6		P0_1				AN0_1	D1
88	86	E5		P0_0				AN0_0	D0
89	87	D5		P10_7	$\overline{KI3}$			AN7	
90	88	A6		P10_6	$\overline{KI2}$			AN6	
91	89	B5		P10_5	$\overline{KI1}$			AN5	
92	90	A5		P10_4	$\overline{KI0}$			AN4	
93	91	C5		P10_3	$\overline{KI7}$			AN3	
94	92	B4		P10_2	$\overline{KI6}$			AN2	
95	93	A4		P10_1	$\overline{KI5}$			AN1	
96	94	C4	AVSS						
97	95	D4		P10_0	$\overline{KI4}$			AN0	
98	96	A3	VREF						
99	97	B3	AVCC						
100	98	C3		P9_7			SIN4	$\overline{ADTRG}$	

1.6 Pin Functions

Table 1.10 Pin Functions for the 100-Pin Package (1/3)

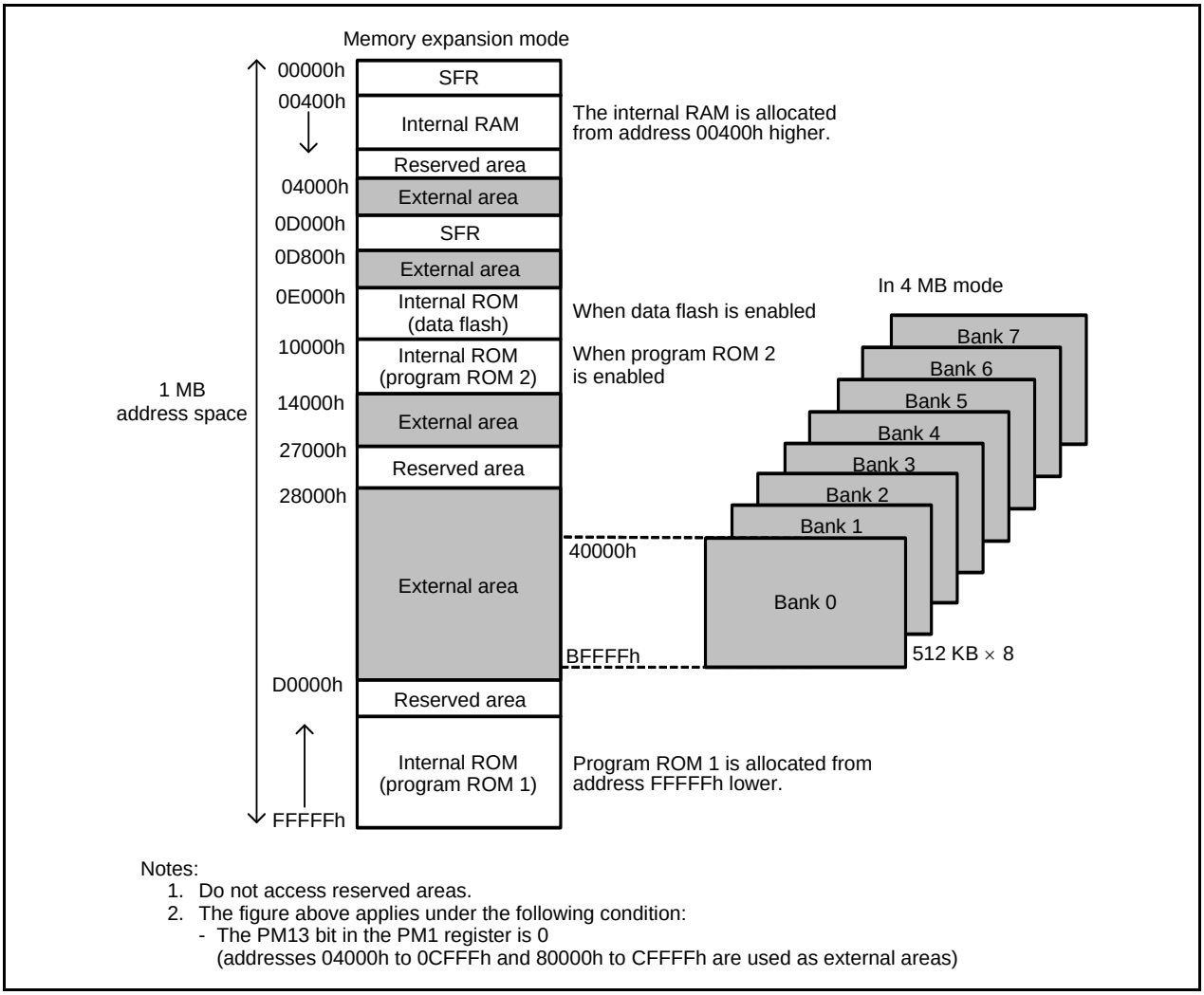
Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 1.8 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2) and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low, and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ selected Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ when using an 8-bit external data bus.
	ALE	O	VCC2	Outputs an ALE signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	$\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up).
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

3. Address Space

3.1 Address Space

The M16C/63 Group has a 1 MB address space from 00000h to FFFFFh. Address space is expandable to 4 MB with the memory area expansion function. Addresses 40000h to BFFFFh can be used as external areas from bank 0 to bank 7. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following condition:
   - The PM13 bit in the PM1 register is 0
     (addresses 04000h to 0CFFFh and 80000h to CFFFFh are used as external areas)

Figure 3.1 Address Space

3.2 Memory Map

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank areas within SFRs are reserved. Do not access these areas.

Internal RAM is allocated from address 00400h and higher, with 10 KB of internal RAM allocated from 00400h to 02BFFh. Internal RAM is used not only for data storage, but also for the stack area when subroutines are called or when an interrupt request is accepted.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is allocated from 0E000h to 0FFFFh. This data flash area is mostly used for data storage, but can also store programs.

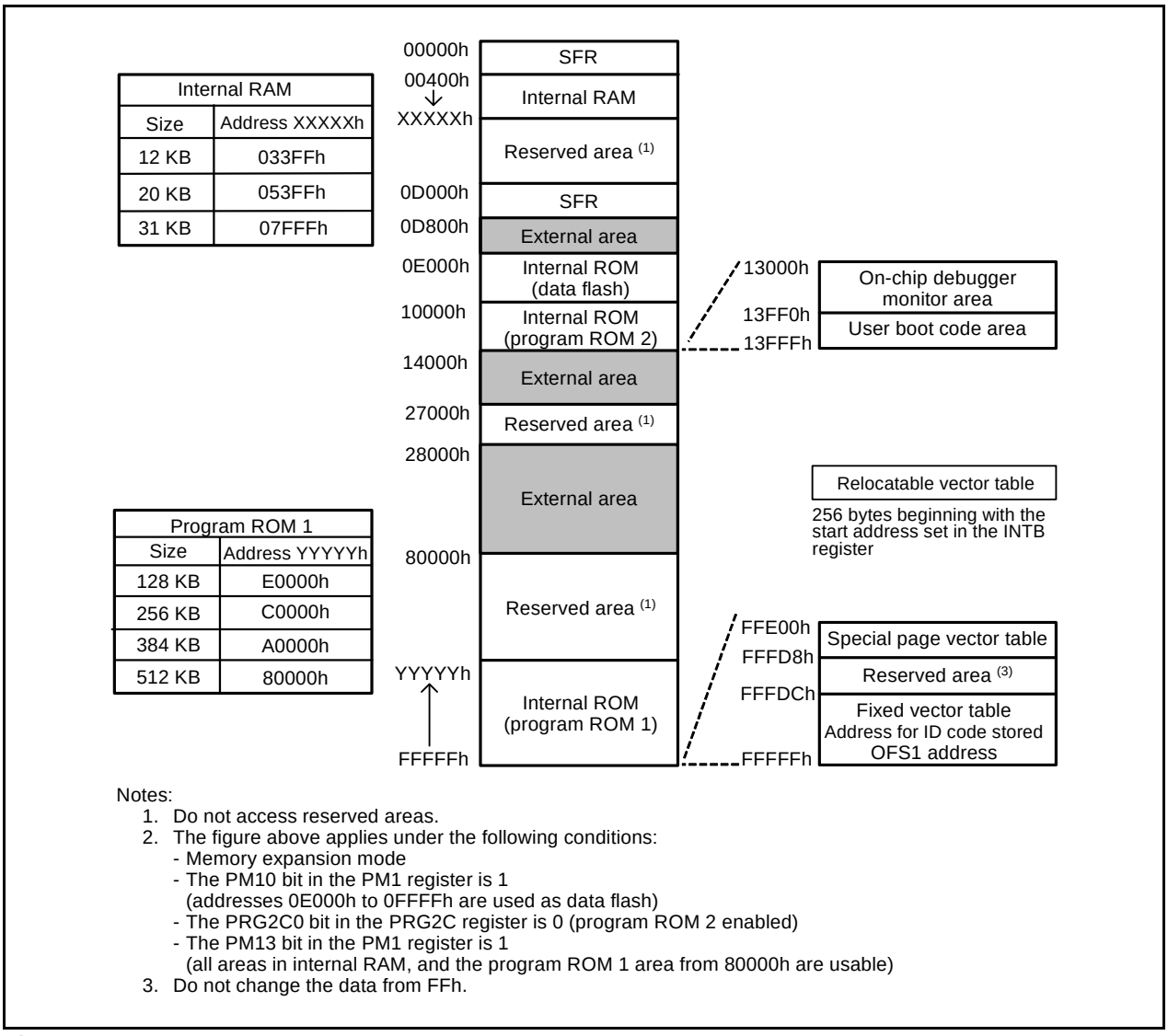
Program ROM 2 is allocated from 10000h to 13FFFh. Program ROM 1 is allocated from FFFFFh and lower, with the 64 KB program ROM 1 area allocated from address F0000h to FFFFFh.

The special page vectors are allocated from FFE00h to FFFD7h. They are used for the JMPS and JSRS instructions. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts is allocated from FFFDCh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

Figure 3.2 shows the Memory Map.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following conditions:
   - Memory expansion mode
   - The PM10 bit in the PM1 register is 1
     (addresses 0E000h to 0FFFFh are used as data flash)
   - The PRG2C0 bit in the PRG2C register is 0 (program ROM 2 enabled)
   - The PM13 bit in the PM1 register is 1
     (all areas in internal RAM, and the program ROM 1 area from 80000h are usable)
3. Do not change the data from FFh.

Figure 3.2 Memory Map

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.20 Read-Modify-Write Instructions

Function	Mnemonic
Transfer	MOV*Dir*
Bit processing	BCLR, BM*Cnd*, BNOT, BSET, BTSTC, and BTSTS
Shifting	ROLC, RORC, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

5.1.6 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 5.12 Voltage Detector 0 Electrical Characteristics

The measurement condition is V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)	When V_{CC1} is falling.	1.80	1.90	2.10	V
	Voltage detection level Vdet0_2 (1)	When V_{CC1} is falling.	2.70	2.85	3.00	V
-	Voltage detector 0 response time (3)	When V_{CC1} falls from 5 V to (Vdet0_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC25 = 1, V_{CC1} = 5.0 V		1.5		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (2)				100	µs

Notes:
1. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
3. Time from when passing the V_{det0} until when a voltage monitor 0 reset is generated.

Table 5.13 Voltage Detector 1 Electrical Characteristics

The measurement condition is V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	When V_{CC1} is falling.	1.90	2.20	2.50	V
	Voltage detection level Vdet1_6 (1)	When V_{CC1} is falling.	2.80	3.10	3.40	V
	Voltage detection level Vdet1_B (1)	When V_{CC1} is falling.	3.55	3.85	4.15	V
	Voltage detection level Vdet1_F (1)	When V_{CC1} is falling.	4.15	4.45	4.75	V
-	Hysteresis width at the rising of V_{CC1} in voltage detector 1	When selecting Vdet1_0		0.10		V
		When selecting Vdet1_6 to Vdet1_F		0.15		V
-	Voltage detector 1 response time (3)	When V_{CC1} falls from 5 V to (Vdet1_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC26 = 1, V_{CC1} = 5.0 V		1.7		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (2)				100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC26 bit in the VCR2 register to 0.
3. Time from when passing the V_{det1} until when a voltage monitor 1 reset is generated.

5.1.7 Oscillator Electrical Characteristics

Table 5.17 40 MHz On-Chip Oscillator Electrical Characteristics

V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO40M}	40 MHz on-chip oscillator frequency	Average frequency in a 10 ms period 2.7 V ≤ V_{CC1} < 5.5 V	36	40	44	MHz
		Average frequency in a 10 ms period 1.8 V ≤ V_{CC1} < 2.7 V	30	40	50	MHz
tsu(f_{OCO40M})	Wait time until 40 MHz on-chip oscillator stabilizes				2	ms

Table 5.18 125 kHz On-Chip Oscillator Electrical Characteristics

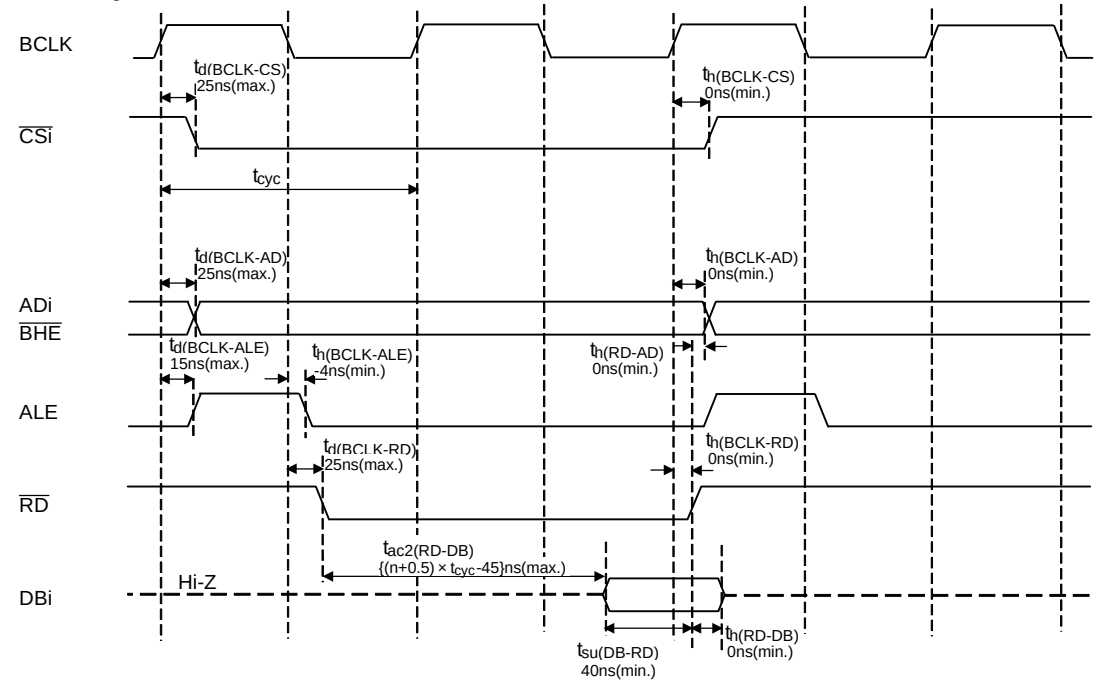
V_{CC1} = 1.8 to 5.5 V, T_{opr} = –20°C to 85°C/–40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO-S}	125 kHz on-chip oscillator frequency	Average frequency in a 10 ms period	100	125	150	kHz
tsu(f_{OCO-S})	Wait time until 125 kHz on-chip oscillator stabilizes				20	µs

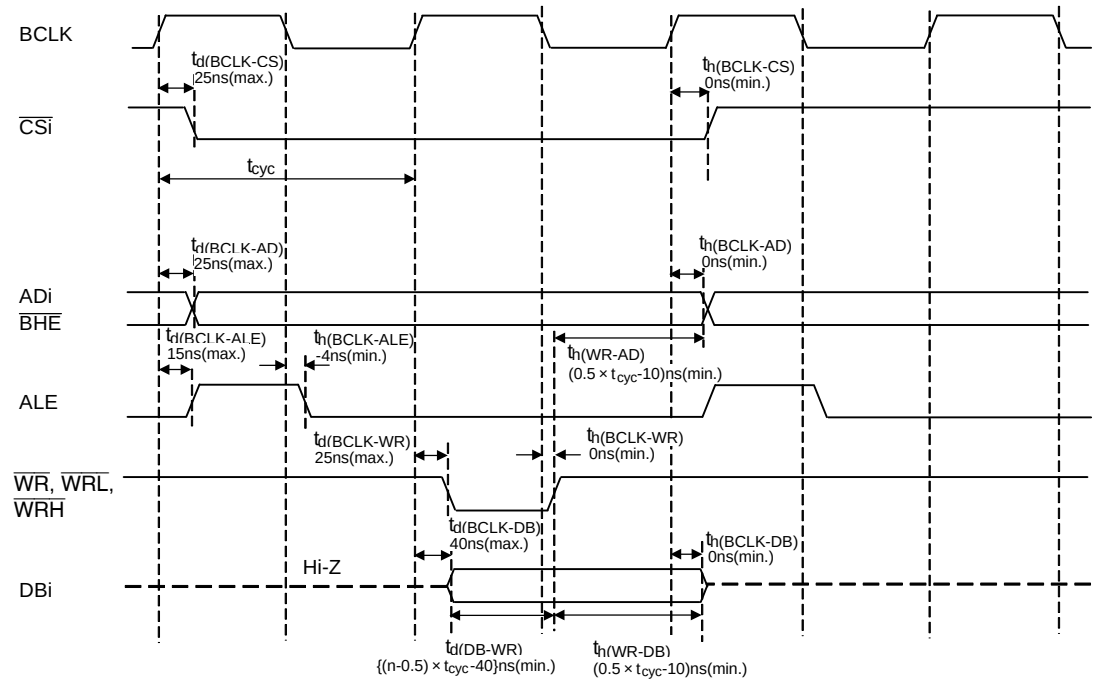
Memory Expansion Mode and Microprocessor Mode
(in 1 to 3 waits setting and when accessing external area)

$V_{CC1} = V_{CC2} = 5V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

n: 1 (when 1 wait)
2 (when 2 waits)
3 (when 3 waits)

Figure 5.17 Timing Diagram

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.4 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area

Table 5.39 Memory Expansion Mode and Microprocessor Mode (in Wait State Setting 2 φ + 3 φ, 2 φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.15		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

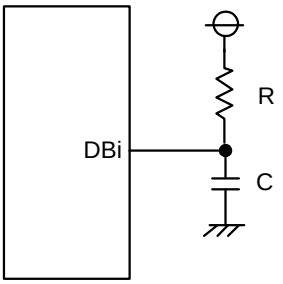
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

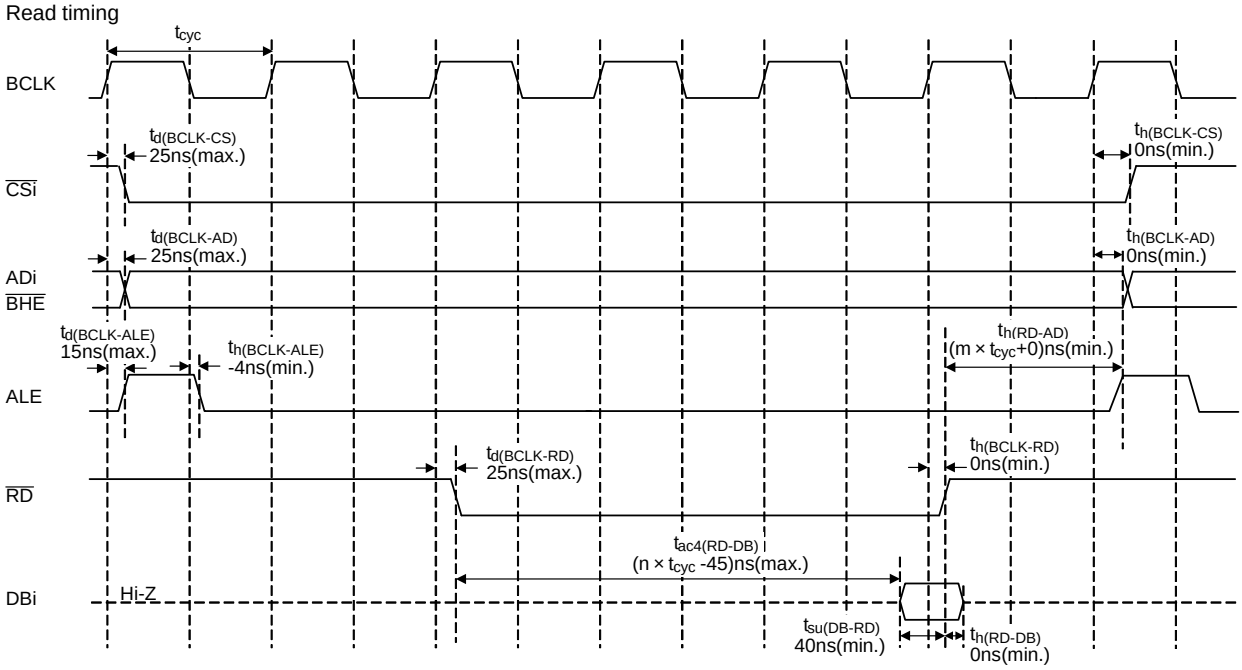
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



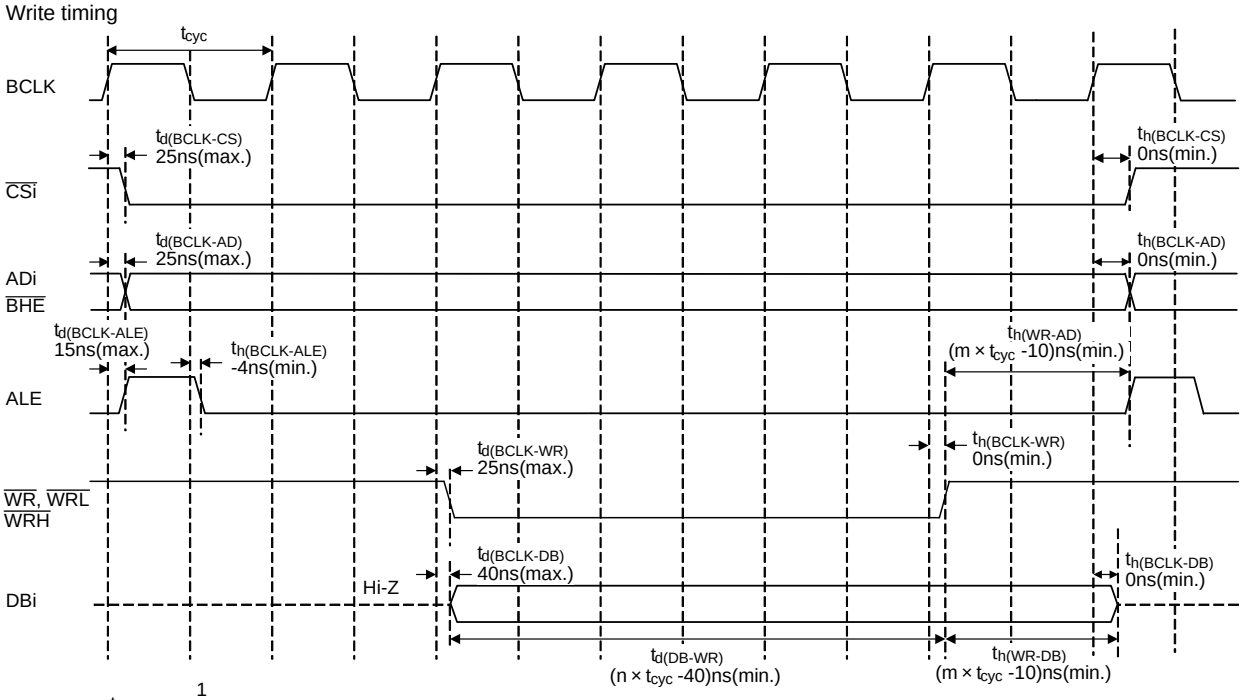
Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and
when inserting 1 to 3 recovery cycles and accessing external area)

$V_{CC1} = V_{CC2} = 5V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage: V_{OL} = 0.4 V, V_{OH} = 2.4 V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

m: 1 (when 1 recovery cycle inserted)
2 (when 2 recovery cycles inserted)
3 (when 3 recovery cycles inserted)

Figure 5.20 Timing Diagram

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.3 Timer A Input

Table 5.45 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

Table 5.46 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

Table 5.47 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

Table 5.48 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

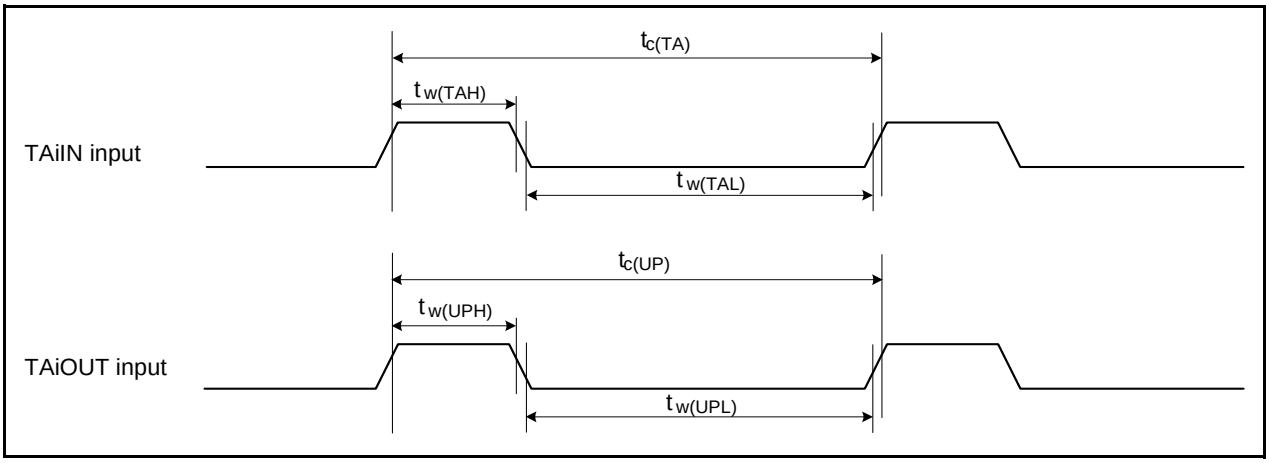


Figure 5.23 Timer A Input

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

Table 5.49 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

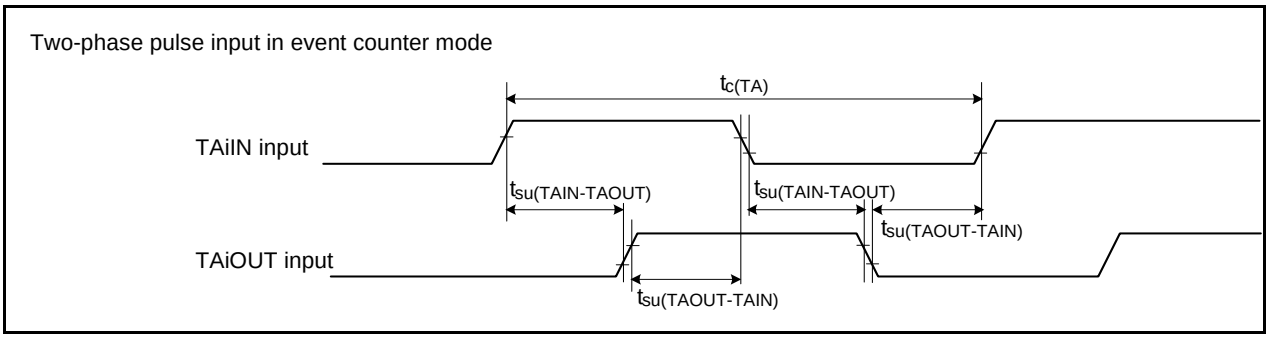


Figure 5.24 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3\ V$, $V_{SS} = 0\ V$, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.59 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.30		50	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			50	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			40	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			40	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			50	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of address		0		ns
$t_{dz(RD-AD)}$	Address output floating start time			8	ns

Notes:

1. Calculated according to the BCLK frequency as follows: $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$
2. Calculated according to the BCLK frequency as follows:
   $\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 50[ns]$ n is 2 for 2 waits setting, 3 for 3 waits setting.
3. Calculated according to the BCLK frequency as follows: $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$
4. Calculated according to the BCLK frequency as follows: $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$
5. When using multiplexed bus, set $f_{(BCLK)}$ 12.5 MHz or less.

$V_{CC1} = V_{CC2} = 1.8$ V

Timing Requirements

($V_{CC1} = V_{CC2} = 1.8$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.4.2.4 Timer B Input

Table 5.72 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	120		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	120		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	240		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	240		ns

Table 5.73 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	1000		ns
$t_{w(TBH)}$	TBiIN input high pulse width	500		ns
$t_{w(TBL)}$	TBiIN input low pulse width	500		ns

Table 5.74 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	1000		ns
$t_{w(TBH)}$	TBiIN input high pulse width	500		ns
$t^{w(TBL)}$	TBiIN input low pulse width	500		ns

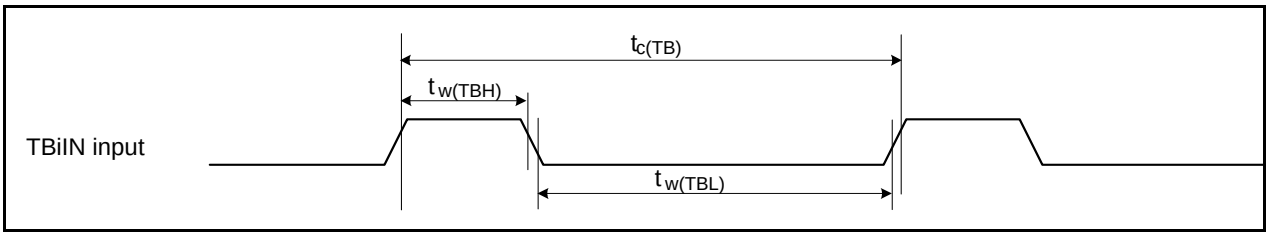


Figure 5.40 Timer B Input

REVISION HISTORY	M16C/63 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Feb 07, 2011	71 to 78, 92 to 99	Table 5.35 to Table 5.40 and Table 5.56 to Table 5.61 Memory Expansion Mode and Microprocessor Mode: Deleted the following: • $\overline{\text{HOLD}}$ input setup time • $\overline{\text{HOLD}}$ input hold time • $\overline{\text{HLDA}}$ output delay time
		72, 93	Figure 5.14 and Figure 5.29 Timing Diagram: Deleted lower figure (Common to wait state and no wait state settings).
		83, 104	Figure 5.20 and Figure 5.35 Timing Diagram: Changed the width of th(RD-AD).
		84	Table 5.41 Electrical Characteristics (1): • Added rows for the CEC value to V_{OL}, V_{T+}-V_{T-}, and Leakage current in powered-off state. • Added “ZP, IDU, IDV, IDW” to the V_{T+} - V_{T-} row.
		85	Table 5.42 Electrical Characteristics (2): Changed “VCC1 = 5.0 V” to "VCC1 = 3.0 V" in the During flash memory program and During flash memory erase rows.
		92	Table 5.56 Memory Expansion Mode and Microprocessor Mode: Changed $\overline{\text{RDY}}$ input setup time from 40.
		105	Table 5.62 Electrical Characteristics (1): • Changed the Measuring Condition over the table. • Added “ZP, IDU, IDV, IDW” to the Parameter column and the value to the Measuring Condition in the V_{T+} - V_{T-} row. • Changed the Measuring Condition in the I_{IH} row.
		106, 107	Table 5.63 Electrical Characteristics (2) and Table 5.64 Electrical Characteristics (3): Changed the Measuring Condition over the table.
		108	Table 5.66 External Clock Input (XIN Input): Changed the condition in note 1.
2.20	Nov 01, 2012	**Overview**	
		2	Table 1.1 Specifications for the 100-Pin Package (1/2): Added the condition for 100.0 ns and changed the condition for 200 ns in the Minimum instruction execution time in the Description column of the CPU.
		3	Table 1.2 Specifications for the 100-Pin Package (2/2): Added “10 MHz/VCC1 = 2.1 to 5.5 V, VCC2 = 2.1 V to VCC1” to the Description column of the Operation Frequency/Supply Voltage.
		4	Table 1.3 Specifications for the 80-Pin Package (1/2): Added the condition for 100.0 ns and changed the condition for 200 ns in the Minimum instruction execution time in the Description column of the CPU.
		5	Table 1.4 Specifications for the 80-Pin Package (2/2): Added “10 MHz/VCC1 = 2.1 to 5.5 V” to the Description column of the Operation Frequency/Supply Voltage.
		Electrical Characteristics	
		52	Table 5.4 Recommended Operating Conditions (3/4) • Changed the Parameter “2.7 V ≤ V_{CC1} < 5.5 V” to “2.7 V ≤ V_{CC1} < 5.5 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 20 MHz” in $f_{(BCLK)}$. • Added the line for “2.1 V ≤ V_{CC1} < 2.7 V, 1 MHz ≤ f(XIN) ≤ 10 MHz” in $f_{(BCLK)}$. • Changed the Parameter “1.8 V ≤ V_{CC1} < 2.7 V” to “1.8 V ≤ V_{CC1} < 2.1 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 10 MHz” in $f_{(BCLK)}$.
		53	Figure 5.1 Relation between $f_{(BCLK)}$ and V_{CC1}: Modified the range of 2.1 V ≤ V_{CC1} < 2.7 V.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.