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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

| Product Status | Not For New Designs |
|----------------------------|---|
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | EBI/EMI, I ² C, SIO, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 31K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-QFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f363akdfa-u0 |

Email: info@E-XFL.COM

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| Item | Function | Description |
|---------------------|---|--|
| | Timer A | 16-bit timer x 5 Timer mode x 5 Event counter mode, one-shot timer mode, pulse width modulation (PWM) mode x 3 Event counter two-phase pulse signal processing (two-phase encoder input) x 2 Programmable output mode x 1 |
| | Timer B | 16-bit timer × 6 Timer mode × 6 Event counter mode, pulse period measurement mode, pulse width measurement mode × 5 |
| Timers | Three-phase motor control timer functions | None |
| | Real-time clock | Count: seconds, minutes, hours, days of the week, months, years Periodic interrupt: 0.25 s, 0.5 s Automatic correction function |
| | PWM function | 8 bits × 2 |
| | Remote control signal receiver | 2 circuits 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) 6-byte receive buffer (1 circuit only) Operating frequency of 32 kHz |
| Serial Interface | UART0 to UART2, UART5 | Clock synchronous/asynchronous × 3 channels I ² C-bus, IEBus, special mode 2 Clock asynchronous × 1 channel I ² C-bus, IEBus, SIM |
| | SI/O3, SI/O4 | Clock synchronization only × 2 channels (SI/O3 is used for transmission only) |
| Multi-master | ¹² C-bus Interface | 1 channel |
| CEC Functior | ns (2) | CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz |
| A/D Converte | r | 10-bit resolution x 26 channels, including sample and hold function Conversion time: 2.15 μs |
| D/A Converte | r | 8-bit resolution x 2 circuits |
| CRC Calculat | tor | CRC-CCITT (X ¹⁶ + X ¹² + X ⁵ + 1), CRC-16 (X ¹⁶ + X ¹⁵ + X ² + 1) compliant |
| Flash Memory | | Program and erase power supply voltage: 2.7 to 5.5 V Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) Program security: ROM code protect, ID code check |
| Debug Functi | ons | On-chip debug, on-board flash rewrite, address match interrupt × 4 |
| Operation Fre | equency/Supply Voltage | 5 MHz/VCC1 = 1.8 to 5.5 V 10 MHz/VCC1 = 2.1 to 5.5 V 20 MHz/VCC1 = 2.7 to 5.5 V |
| Current Cons | umption | Described in Electrical Characteristics |
| Operating Ter | mperature | -20°C to 85°C, -40°C to 85°C ⁽¹⁾ |
| Package | | 80-pin LQFP: PLQP0080KB-A (Previous package code: 80P6Q-A) |

Table 1.4Specifications for the 80-Pin Package (2/2)

Notes:

1. See Table 1.5 "Product List" for the operating temperature.

 The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

1.5 Pin Assignments

Figure 1.6 to Figure 1.9 show pin assignments. Table 1.6 to Table 1.9 list pin names.



Figure 1.6 Pin Assignment for the 100-Pin Package

| FA FB LG Control Pin Pot Interrupt Timer Serial interface AUD converter, D/A converter, Bus Control Pin 51 40 49 P4_3 A19 52 50 K10 P4_1 A18 53 51 J10 P4_1 A17 54 52 J9 P4_0 A18 55 53 H9 P3_7 A14 56 54 H10 P3_6 A13 58 56 F P3_3 A14 59 57 G9 P3_3 A13 60 56 G10 P3_2 A11 61 59 F2 P3_0 A10 61 61 F10 P3_0 A10 62 60 F9 VCC2 AN2_7 A7, [A7/D7], [A7/D6],[A5/D6] 64 | F | Pin No |). | | | | I/O Pin f | or Peripheral Fund | ction | |
|--|-----|----------|------------|----------------|-------|--------------------|-----------|--------------------|---------------------------------|----------------------|
| 151 49 K9 P4.2 A19 25 50 K10 P4.2 A18 53 51 J10 P4.1 A17 54 52 J9 P4.0 A16 55 53 H9 P3.7 A16 56 53 H9 P3.7 A15 56 56 H9 P3.7 A14 57 56 F6 P3.5 A14 59 57 G9 P3.3 A12 58 56 F7 P3.4 A12 60 58 G10 P3.2 A11 61 59 76 G9 P3.3 A12 63 61 F10 P3.0 A12 A10 64 62 E8 VSS A11 A3 A8 65 63 E9 P2.7 AN2.7 A7.(A7.D7.[A7.D6] 66 64 E10 P2.6 AN2.4 A4.[A4D4].(A4D3] 68 67 D8 P2.3 A | FA | FB | LG | Control Pin | Port | Interrupt | Timer | Serial interface | A/D converter, D/A converter | Bus Control Pin |
| 12 50 K10 P4.2 A18 13 51 J10 P4.1 A17 14 52 J9 P4.0 A16 155 53 H9 P3.7 A16 156 54 H10 P3.6 A11 157 55 F6 P3.5 A11 168 56 F7 P3.4 A12 159 57 G9 P3.3 A11 160 58 G10 P3.2 A11 161 59 F8 P3.1 A10 161 F8 P3.1 A10 A12 163 F10 P3.0 A11 A10 164 62 E8 VSS A14 166 63 E9 P2.7 AN2.4 At, [A/D7], [A7/D6] 166 64 E10 P2.6 AN2.4 At, [A/D7], [A7/D6] 167 65 E7 P2.2 AN2.4 At, [A/D1], [A1/D1] 168 60 D7 P2.4 INT6 | 51 | 49 | K9 | | P4_3 | | | | | A19 |
| 53 51 J10 P4.0 A17 54 52 J9 P4.0 A16 55 53 H9 P3.7 A16 56 54 H10 P3.6 A13 56 55 F6 P3.5 A13 58 56 F7 P3.4 A12 59 57 69 P3.2 A11 60 58 G10 P3.2 A10 61 59 F7 OB P3.1 A12 62 60 F9 VCC A10 A12 63 61 F10 P3.0 A8. A82 64 62 E8 VSS A12.6 A6. [A6/D5]. [A7/D6] 66 64 E10 P2.6 AN2.4 A4. [A4/D4]. [A4/D3]. [A3/D7] 70 68 D10 P2.3 A3. [A3/D3]. [A3/D2] A3. [A3/D3]. [A3/D2]. [A2/D2]. [A2/D1]. [A1/D0] 71 68 D10 P2.2 A3. [A3/D3]. [A3/D2]. [A2/D2]. [A2/D1]. [A1/D0] 71 72 76 A9 | 52 | 50 | K10 | | P4_2 | | | | | A18 |
| 64 52 J9 P4.0 A16 55 53 H9 P3.7 A15 56 54 H10 P3.6 A14 57 55 F6 P3.5 A13 58 56 F7 P3.4 A12 59 57 G9 P3.3 A11 60 58 G10 P3.2 A11 61 59 F8 P3.1 A11 63 61 F10 P3.2 A11 64 62 E8 VSS A8 66 63 E9 P2.7 AN2.6 A6, [A&D6], [A&D5] 66 64 E10 P2.6 AN2.2 A5, [A&D6], [A&D5] 68 66 D7 P2.4 INT6 AN2.4 A4, [AD4], [A/D3] 68 66 D7 P2.2 INT7 AN2.2 A5, [A/D6], [A/D3] 70 68 D10 P2.2 INT6 AN2.4 A4, [A/D4], [A/D3] 71 69 P1.7 INT5 IDU < | 53 | 51 | J10 | | P4_1 | | | | | A17 |
| 55 63 H9 P3,7 A15 56 54 H10 P3,6 A14 57 55 F6 P3,3 A13 58 56 F7 P3,4 A13 58 57 69 P3,3 A11 60 58 G10 P3,2 A10 61 59 7 69 P3,1 A10 61 59 F6 P3,1 A10 A11 60 58 G10 P3,2 A10 A10 61 59 F6 P3,0 A11 A10 63 61 F10 P3,0 A12 A17 65 63 E9 YZ A12,7 A7, [A7/D7, [A7/D6] 66 64 E10 P2,6 INT7 A12,2 A5, [A5/D5], [A5/D4] 68 67 D8 P2,3 A14, [A4/D4], [A4/D3] A3, [A3/D3], [A3/D2] 70 68 D10 P2,0 A12, [A2/D1], [A1/D3], [A1/D3] A12, [A2/D2], [A2/D2], [A2/D2], [A2/D2], [A2/D2], [A2/D2], [A2/D2], [A2/D2], [A2 | 54 | 52 | J9 | | P4_0 | | | | | A16 |
| 66 54 H10 P3.6 A14 57 55 F6 P3.5 A13 58 56 F7 P3.4 A13 58 57 G3 P3.3 A11 58 56 F7 P3.4 A11 59 57 G3 P3.3 A11 60 58 G10 P3.2 A11 61 59 F8 P3.1 A9 52 60 F9 VC2 A9 63 61 F10 P3.0 A8 64 62 E8 VSS AN2.7 A7. [A7D7], [A7D6] 66 64 E10 P2.6 AN2.7 A7. [A2D3], [A2D3] 66 64 E10 P2.4 INT6 AN2.4 A4. [A4D4], [A4D3], [A3D2] 70 68 D10 P2.2 INT6 AN2.1 A1. [A1D1], [A1D0] 71 169 P1.7 INT5 IDU D15 D14 73 71 C3 IC3 IC4 IC4. [A2 | 55 | 53 | H9 | | P3_7 | | | | | A15 |
| F7 $F6$ $F7$ $P3.5$ A13 $F7$ $P3.4$ A13 A13 $F7$ $P3.3$ A12 $F7$ $P3.3$ A11 $F7$ $P3.3$ A11 $F8$ $P3.1$ A10 $F1$ $P3.0$ A13 $F8$ $P2.1$ A17 $F1$ $P3.0$ A12 $F1$ $P2.5$ $A12.7$ $F1$ $P2.4$ $A17.670.76.76.76.76.76.76.76.76.76.76.76.76.76.$ | 56 | 54 | H10 | | P3_6 | | | | | A14 |
| 58 56 F7 P3.4 A12 59 57 69 P3.3 A11 60 58 610 P3.2 A10 61 59 F8 P3.1 A9 62 60 F9 VCC A9 63 61 F10 P3.0 A8, [AB/D7] 64 62 E8 VSS A8, [AB/D7] 65 63 E9 P2.7 AN2.7 A7, [A7/D7], [A7/D6] 66 64 E10 P2.6 AN2.6 A6, [A6/D6], [A6/D5] 67 D5 T7 P2.4 INT6 AN2.4 A4, [A4/D4], [A4/D3] 68 66 D7 P2.4 INT6 AN2.3 A3, [A3/D2] 70 68 D10 P2.2 AN2.1 A1, [A1/D1], [A1/D0], [A2/D2], [A2/D1] 71 72 70 C10 P2.0 AN2.1 A1, [A1/D1], [A1, [A1/D1], [A1/D1], [A1, [A1/D1], [A1/D1], [A1, [A1 | 57 | 55 | F6 | | P3_5 | | | | | A13 |
| 59 57 G9 P3.3 A11 60 58 G10 P3.2 A10 61 59 F8 P3.1 A10 62 60 F9 VCC2 A39 64 62 E8 VSS A8, [A&D7] 64 62 E8 VSS AN2.6 A6, [A&D7], [A7/D6], [A7/D6] 66 64 E10 P2.5 INT7 AN2.5 A5, [A5/D3], [A5/D4] 68 F10 P2.5 INT7 AN2.5 A5, [A5/D4], [A/D3], [A3/D2] 68 66 D7 P2.4 INT6 AN2.2 A3, [A3/D3], [A3/D2], [A3/D2], [A2/D1] 70 68 D10 P2.2 AN2.2 A2, [A2/D2], [A2/D1] 71 69 P2.0 AN2.2 A3, [A3/D3], [A3/D2], [A2/D1] 71 69 P1.5 INT3 IDU D14 75 73 B9 P1.5 INT3 IDV D14 76 74 B10 P1.4 D12 D14 D12 77 540 P1.2 </td <td>58</td> <td>56</td> <td>F7</td> <td></td> <td>P3_4</td> <td></td> <td></td> <td></td> <td></td> <td>A12</td> | 58 | 56 | F7 | | P3_4 | | | | | A12 |
| 60 58 G10 P3_2 A10 61 59 F8 P3_1 A9 62 60 F9 VCC2 A8, [A8/D7] 63 61 F10 P3_0 A8, [A8/D7] 64 62 E8 VSS A8, [A8/D7] 65 63 E9 P2_7 AN2_7 A7, [A7/D7], [A7/D6] 66 64 E10 P2_6 AN2_6 A6, [A6/D6], [A6/D5] 67 D8 P2_3 AN2_4 A4, [A4/D4], [A4/D3] 68 67 D8 P2_3 AN2_2 A2, [A2/D2], [A2/D1] 70 68 D10 P2_2 AN2_1 A1, [A1/D1], [A1/D0] 71 69 D9 P2_1 AN2_1 A1, [A1/D1], [A1/D0] 71 69 D9 P2_1 AN2_1 A1, [A1/D1], [A1/D0] 73 71 C9 P1_7 INT5 IDU D14 75 73 B9 P1_5 INT3 IDV D13 76 74 P1_6 INT4 IDW <td< td=""><td>59</td><td>57</td><td>G9</td><td></td><td>P3_3</td><td></td><td></td><td></td><td></td><td>A11</td></td<> | 59 | 57 | G9 | | P3_3 | | | | | A11 |
| 61 59 F8 P3_1 A9 62 60 F9 VCC2 A8, [A8/D7] A8, [A8/D7] 64 62 E8 VSS A8, [A8/D7] A8, [A8/D7] 64 62 E8 VSS AN2_7 A7, [A7/D7], [A7/D6], [A6/D6] 66 64 E10 P2_6 AN2_6 A6, [A6/D6], [A6/D5], [A5/D4] 66 64 E10 P2_6 AN2_4 A4, [A4/D4], [A4/D3], [A3/D2], [A2/D1] 68 66 D7 P2_4 INT6 AN2_4 A4, [A4/D4], [A4/D3], [A3/D2], [A2/D1] 70 68 D10 P2_2 AN2_2 AN2_2 A2, [A2/D2], [A2/D1], [A1/D1], [A1/D1] | 60 | 58 | G10 | | P3_2 | | | | | A10 |
| 62 60 $F9$ VCC2 P3.0 A8. [A8/D7] 63 61 $F10$ P3.0 A8. [A8/D7] A8. [A8/D7] 64 62 63 $E9$ P2.7 AN2.7 A7. [A7/D7]. [A7/D6] 66 63 $E9$ P2.7 AN2.6 A6. [A6/D6]. [A6/D5] 66 67 $E7$ P2.5 INT7 AN2.5 A5. [A5/D6]. [A5/D4] 66 66 $D7$ P2.4 INT6 AN2.4 A4. [A4/D4]. [A4/D3] 68 66 $D7$ P2.4 INT6 AN2.2 A3. [A3/D3]. [A3/D2] 70 68 $D10$ P2.2 AN2.2 A2. [A2/D2]. [A2/D1] 71 69 $P9$ $P2.1$ AN2.0 A0. [A0/D0]. A0 73 71 $C9$ $P1.7$ INT5 IDU D15 74 72 $E6$ $P1.6$ INT4 IDW D13 77 75 <a10< td=""> $P1.3$ TXD6/SDA6</a10<> | 61 | 59 | F8 | | P3_1 | | | | | A9 |
| 63 61 F10 P3_0 A8, [A8/D7] 64 62 E8 VSS A8, [A8/D7] 65 63 E9 P2_7 AN2_6 A6, [A6/D6], [A6/D5] 66 64 E10 P2_6 AN2_5 A6, [A6/D6], [A6/D5] 67 65 E7 P2_5 INT7 AN2_5 A5, [A5/D5], [A5/D4] 68 60 D7 P2_4 INT6 AN2_4 A4, [A4/D4], [A4/D3] 69 67 D8 P2_3 AN2_4 A4, [A4/D4], [A4/D3] 70 68 D10 P2_2 AN2_1 A1, [A1/D1], [A1/D0] 71 C9 P1_7 INT5 IDU D14 73 71 C9 P1_6 INT4 IDW D14 76 74 B10 P1_4 IDW D14 D12 77 75 A10 P1_3 TXD6/SDA6 D11 D12 77 75 A10 P1_3 CX66 D9 D12 77 76 A9 P1_1 CLK6 | 62 | 60 | F9 | VCC2 | | | | | | |
| 64 62 E8 VSS P2_7 AN2_7 A7, [A7/D7], [A7/D6] 66 64 E10 P2_6 AN2_6 AA2_6 A6, [A6/D6], [A6/D5] 67 65 E7 P2_5 INT7 AN2_5 A5, [A6/D6], [A6/D5] 68 66 D7 P2_4 INT6 AN2_3 A3, [A3/D2], [A3/D2] 70 68 D10 P2_2 AN2_1 A1, [A1/D1], [A1/D1] 70 68 D10 P2_2 AN2_1 A1, [A1/D1], [A1/D0] 71 69 D9 P2_1 AN2_0 A0, [A0/D0], A0 73 71 C9 P1_7 INT5 IDU D15 74 72 E6 P1_6 INT4 IDW D14 76 74 B10 P1_4 D12 TXD6/SDA6 D11 77 75 A10 P1_3 TXD6/SDA6 D11 D12 77 75 A10 P1_3 TXD6/SDA6 D11 <td< td=""><td>63</td><td>61</td><td>F10</td><td></td><td>P3_0</td><td></td><td></td><td></td><td></td><td>A8, [A8/D7]</td></td<> | 63 | 61 | F10 | | P3_0 | | | | | A8, [A8/D7] |
| 66 63 E9 P2_7 AN2_7 A7, [A7/07], [A7/06] 66 64 E10 P2_6 AN2_6 A6, [A6/05], [A6/05] 67 65 E7 P2_5 INT7 AN2_5 A5, [A5/05], [A5/04] 68 66 D7 P2_4 INT6 AN2_4 A4, [A4/04], [A4/03] 68 67 D8 P2_3 AN2_4 A4, [A4/04], [A4/03] 70 68 D10 P2_2 AN2_2 A2, [A2/02], [A2/01] 71 69 D9 P2_1 AN2_1 A1, [A1/01], [A1/00] 72 70 C10 P2_0 AN2_1 A1, [A1/01], [A1/00] 73 71 C3 P1_7 INT5 IDU D14 75 73 B9 P1_5 INT3 IDV D14 75 A10 P1_4 IDV D12 D17 77 C8 P1_1 CLK6 D9 D10 77 C8 P1_1 <t< td=""><td>64</td><td>62</td><td>E8</td><td>VSS</td><td></td><td></td><td></td><td></td><td></td><td></td></t<> | 64 | 62 | E8 | VSS | | | | | | |
| 66 64 E10 P2_6 AN2_6 A6, [A6/D6], [A6/D5], [A5/D4] 67 65 E7 P2_5 INT7 AN2_5 A5, [A5/D5], [A5/D4] 68 66 D7 P2_4 INT6 AN2_4 A4, [A4/D4], [A4/D3] 68 67 D8 P2_2 AN2_3 A3, [A3/D3], [A3/D2] 70 68 D10 P2_2 AN2_1 A1, [A1/D1], [A1/D0] 71 69 D9 P2_1 AN2_0 A0, [A0/D0], A0 71 C9 P1_7 INT5 IDU D15 74 72 E6 P1_6 INT4 IDW D14 75 73 B9 P1_5 INT3 IDV D13 76 74 B10 P1_3 TXD6/SDA6 D10 D12 77 75 A10 P1_3 CT P1_0 D16 D9 80 78 C7 P1_0 CTS6/RTS6 D8 D8 8 | 65 | 63 | E9 | | P2_7 | | | | AN2_7 | A7, [A7/D7], [A7/D6] |
| 67 65 E7 P2_5 INT7 AN2_5 A5, [A5/D5], [A5/D4] 68 60 D7 P2_4 INT6 AN2_4 A4, [A4/D4], [A4/D3] 69 67 D8 P2_3 AN2_3 A3, [A3/D3], [A3/D2] 70 68 D10 P2_2 AN2_2 A2, [A2/D2], [A2/D1] 71 69 P9 P2_1 AN2_1 A1, [A1/D1], [A1/D0] 71 C10 P2_0 AN2_1 A1, [A1/D1], [A1/D0] D15 74 72 E6 P1_6 INT4 IDW D14 D14 75 73 B9 P1_5 INT3 IDV D13 D14 76 74 B10 P1_4 D12 D12 D12 D12 77 75 A10 P1_2 RXD6/SCL6 D10 D12 D17 77 75 A10 P1_2 CLK6 D9 B8 D6 D2.5 AN0_5 D5 84 </td <td>66</td> <td>64</td> <td>E10</td> <td></td> <td>P2_6</td> <td></td> <td></td> <td></td> <td>AN2_6</td> <td>A6, [A6/D6], [A6/D5]</td> | 66 | 64 | E10 | | P2_6 | | | | AN2_6 | A6, [A6/D6], [A6/D5] |
| 68 66 D7 P2_4 INT6 AN2_4 A4, [A4/D4], [A4/D3] 69 67 D8 P2_3 AN2_3 A3, [A3/D3], [A3/D2] 70 68 D10 P2_2 AN2_2 A2, [A2/D2], [A2/D1] 71 69 D9 P2_1 AN2_2 A2, [A2/D2], [A2/D1] 72 70 C10 P2_0 AN2_2 A2, [A2/D1], [A1/D0] 72 70 C10 P2_0 AN2_0 A0, [A0/D0], A0 73 71 C3 P1_7 INT5 IDU D14 75 73 B9 P1_5 INT3 IDV D13 76 74 B10 P1_4 D14 D12 D17 77 75 A10 P1_3 TXD6/SDA6 D10 D12 77 76 A9 P1_1 CLK6 D9 D3 81 79 A8 P0_7 AN0_5 D5 84 82 B7 < | 67 | 65 | E7 | | P2_5 | INT7 | | | AN2_5 | A5, [A5/D5], [A5/D4] |
| 69 67 D8 P_2_3 AN2_3 A3_[A3/D3], [A3/D2] 70 68 D10 $P2_2$ AN2_1 A1, [A1/D1], [A1/D0] 71 69 D9 $P2_1$ AN2_1 A1, [A1/D1], [A1/D0] 72 70 C10 $P2_0$ AN2_0 A0, [A0/D0], A0 73 71 C9 $P1_7$ INT5 IDU D15 74 72 E6 P1_6 INT4 IDW D14 75 73 B9 $P1_5$ INT3 IDV D13 76 74 B10 P1_4 D12 D12 77 75 A10 P1_3 TXD6/SDA6 D11 78 76 A9 P1_2 RXD6/SCL6 D10 79 77 C8 P1_1 CLK6 D9 80 78 C7 P1_0 CTS6/RTS6 D8 81 79 A8 P0_5 AN0_5 D5 | 68 | 66 | D7 | | P2 4 | INT6 | | | AN2 4 | A4. [A4/D4]. [A4/D3] |
| TO 68 D10 $P2_2$ AN2_2 A2, [A2/D2], [A2/D1] 71 69 D9 P2_1 AN2_1 A1, [A1/D1], [A1/D0] 72 70 C10 P2_0 AN2_0 A0, [A0/D0], A0 73 71 C9 P1_7 INT5 IDU D15 74 72 E6 P1_6 INT4 IDW D14 75 73 B9 P1_5 INT3 IDV D13 76 74 B10 P1_4 D12 D12 77 75 A10 P1_4 D12 D12 77 75 A10 P1_2 RXD6/SCL6 D10 78 76 A9 P1_2 RXD6/SCL6 D10 78 76 A9 P1_2 RXD6/SCL6 D10 78 78 B6 P0_7 D7 AN0_5 D5 84 82 B7 P0_6 AN0_5 D5 <t< td=""><td>69</td><td>67</td><td>D8</td><td></td><td>P2 3</td><td></td><td></td><td></td><td></td><td>A3. [A3/D3]. [A3/D2]</td></t<> | 69 | 67 | D8 | | P2 3 | | | | | A3. [A3/D3]. [A3/D2] |
| 1 <td>70</td> <td>68</td> <td>D10</td> <td></td> <td>P2 2</td> <td></td> <td></td> <td></td> <td>AN2 2</td> <td>A2, [A2/D2], [A2/D1]</td> | 70 | 68 | D10 | | P2 2 | | | | AN2 2 | A2, [A2/D2], [A2/D1] |
| 72 70 C10 $P_{2.0}$ AN2_0 AN2_0 AN_A(A)/D0, AU 73 71 C9 P1_7 INT5 IDU D15 74 72 E6 P1_6 INT4 IDW D14 75 73 B9 P1_5 INT3 IDV D13 76 74 B10 P1_3 TXD6/SDA6 D11 77 75 A10 P1_3 TXD6/SDA6 D11 78 76 A9 P1_2 RXD6/SCL6 D10 77 75 A10 P1_3 CKK6 D9 80 78 C7 P1_0 CTS6/RTS6 D8 81 79 A8 P0_7 AN0_4 D4 82 80 B8 P0_6 AN0_4 D4 83 81 D6 P0_2 AN0_4 D4 85 83 A7 P0_3 AN0_1 D1 86 84 <td>71</td> <td>69</td> <td>D9</td> <td></td> <td>P2 1</td> <td></td> <td></td> <td></td> <td>AN2 1</td> <td>A1. [A1/D1]. [A1/D0]</td> | 71 | 69 | D9 | | P2 1 | | | | AN2 1 | A1. [A1/D1]. [A1/D0] |
| 73 71 C9 P1_7 INT5 IDU D15 74 72 E6 P1_6 INT4 IDW D14 75 73 B9 P1_5 INT3 IDV D13 76 74 B10 P1_4 D12 D13 76 74 B10 P1_2 RXD6/SCL6 D11 78 76 A9 P1_2 RXD6/SCL6 D10 79 77 C8 P1_1 CLK6 D9 80 78 C7 P1_0 CTS6/RTS6 D8 81 79 A8 P0_7 AN0_7 D7 82 80 B8 P0_6 AN0_7 D7 82 80 B7 P0_4 AN0_3 D3 84 86 P0_2 AN0_2 D2 87 85 C6 P0_1 AN0_1 D1 88 86 E5 P0_0 AN0_2 D2 87 85 C6 P10_7 Ki3 AN7 | 72 | 70 | C10 | | P2 0 | | | | AN2 0 | A0. [A0/D0]. A0 |
| 74 72 $E6$ $P1_{-6}$ $INT4$ IDW $D14$ 75 73 $B9$ $P1_{-5}$ $INT3$ IDV $D13$ 76 74 $B10$ $P1_{-4}$ $D12$ $D13$ 76 74 $B10$ $P1_{-4}$ $D12$ $D12$ 77 75 $A10$ $P1_{-3}$ $TXD6/SDA6$ $D11$ 78 76 $A9$ $P1_{-2}$ $RXD6/SCL6$ $D10$ 79 77 $C8$ $P1_{-1}$ $CLK6$ $D9$ 80 78 $C7$ $P1_{-0}$ $CTS6/RTS6$ $D8$ 81 79 $A8$ $P0_{-7}$ $AN0_{-7}$ $D7$ 82 80 $B8$ $P0_{-6}$ $AN0_{-5}$ $D5$ 84 28 7 $P0_{-4}$ $AN0_{-6}$ $D6$ 83 81 $D6$ $P0_{-5}$ $AN0_{-5}$ $D5$ 84 86 $P0_{-2}$ $AN0_{-3}$ $D3$ $AN0_{-1}$ $D1$ 87 <td>73</td> <td>71</td> <td>C9</td> <td></td> <td>P1 7</td> <td>INT5</td> <td>IDU</td> <td></td> <td></td> <td>D15</td> | 73 | 71 | C9 | | P1 7 | INT5 | IDU | | | D15 |
| 17 12 12 11 11 11 11 11 11 11 11 11 75 73 89 P1_4 013 013 013 76 74 810 P1_4 013 013 013 77 75 A10 P1_3 TXD6/SDA6 011 78 76 A9 P1_2 RXD6/SCL6 010 79 77 C8 P1_1 CLK6 09 80 78 C7 P1_0 CTS6/RTS6 08 81 79 A8 P0_7 AN0_7 07 82 80 88 P0_6 AN0_7 07 83 81 D6 P0_5 AN0_4 04 84 82 B7 P0_3 AN0_2 02 87 85 C6 P0_1 AN0_1 01 88 86 E5 P0_0 AN0_0 00 89 87 D5 P10_7 K13 AN7 90 | 74 | 72 | F6 | | P1 6 | | | | | D14 |
| 173 173 173 174 174 175 175 171 174 175 175 171 174 175 174 174 175 174 174 175 175 176 174 174 175 175 175 175 175 175 175 175 175 175 175 175 177 175 176 174 175 175 175 175 175 175 175 175 175 175 175 175 175 177 175 | 75 | 72 | BO | | D1 5 | | | | | D12 |
| 176 174 10 P1_4 TXD6/SDA6 D12 777 75 A10 P1_3 TXD6/SDA6 D11 78 76 A9 P1_2 RXD6/SCL6 D10 79 77 C8 P1_1 CLK6 D9 80 78 C7 P1_0 CTS6/RTS6 D8 81 79 A8 P0_7 AN0_7 D7 82 80 B8 P0_6 AN0_6 D6 83 81 D6 P0_5 AN0_6 D5 84 82 B7 P0_4 AN0_3 D3 86 84 B6 P0_2 AN0_2 D2 87 85 C6 P0_1 AN0_0 D0 88 86 E5 P0_0 AN0_2 D2 87 D5 P10_7 K13 AN7 D0 90 88 A6 P10_10_KI3 AN5 99 91 89 B5 P10_15 K11 AN5 92 | 75 | 73 | D3 | | D1 4 | 1113 | | | | D13 |
| 17 73 $A10$ $P1_{-2}$ $RXD6/SCL6$ D11 78 76 $A9$ $P1_{-2}$ $RXD6/SCL6$ D10 79 77 $C8$ $P1_{-1}$ $CLK6$ D9 80 78 $C7$ $P1_{-0}$ $\overline{CTS6/RTS6}$ D8 81 79 $A8$ $P0_{-7}$ $AN0_{-7}$ D7 82 80 $B8$ $P0_{-6}$ $AN0_{-7}$ D7 82 80 $B8$ $P0_{-6}$ $AN0_{-7}$ D7 82 87 $P0_{-4}$ $AN0_{-5}$ D5 84 82 $B7$ $P0_{-4}$ $AN0_{-3}$ D3 86 84 $B6$ $P0_{-2}$ $AN0_{-3}$ D3 87 85 $C6$ $P0_{-1}$ $AN0_{-3}$ D3 88 86 $E5$ $P0_{-0}$ $AN0_{-0}$ D0 89 87 $D5$ $P10_{-7}$ $\overline{K13}$ $AN7$ 90 91 89 85 $P10_{-5}$ < | 70 | 74 | D10 A10 | | F1_4 | | | | | D12 |
| 79 77 68 $P1_{-1}$ $CLK6$ D9 80 78 $C7$ $P1_{-0}$ $CLK6$ D9 80 78 $C7$ $P1_{-0}$ $CLK6$ D9 80 78 $C7$ $P1_{-0}$ $CTS6/RTS6$ D8 81 79 $A8$ $P0_{-7}$ $AN0_{-7}$ D7 82 80 88 $P0_{-6}$ $AN0_{-6}$ D6 83 81 $D6$ $P0_{-5}$ $AN0_{-6}$ D6 83 87 $P0_{-4}$ $AN0_{-3}$ D3 84 86 $P0_{-2}$ $AN0_{-2}$ D2 87 85 $C6$ $P0_{-1}$ $AN0_{-2}$ D2 87 85 $C6$ $P0_{-1}$ $AN0_{-1}$ D1 88 86 $E5$ $P0_{-0}$ $AN0_{-1}$ D1 89 87 $D5$ $P10_{-7}$ $\overline{K13}$ $AN7$ $O0$ 90 88 $A6$ $P10_{-6}$ $\overline{K12}$ $AN6$ <td>70</td> <td>75</td> <td></td> <td></td> <td>FI_3</td> <td></td> <td></td> <td>TAD0/SDA0</td> <td></td> <td></td> | 70 | 75 | | | FI_3 | | | TAD0/SDA0 | | |
| 17 CGS $P1_{-1}$ $CCRS$ $D9$ 80 78 $C7$ $P1_{-0}$ $\overline{CTS6}/\overline{RTS6}$ $D8$ 81 79 A8 $P0_{-7}$ $AN0_{-7}$ $D7$ 82 80 B8 $P0_{-6}$ $AN0_{-6}$ $D6$ 83 81 D6 $P0_{-5}$ $AN0_{-5}$ $D5$ 84 82 B7 $P0_{-4}$ $AN0_{-3}$ $D3$ 86 84 B6 $P0_{-2}$ $AN0_{-3}$ $D3$ 86 84 B6 $P0_{-2}$ $AN0_{-1}$ $D1$ 87 85 C6 $P0_{-1}$ $AN0_{-1}$ $D1$ 88 86 E5 $P0_{-0}$ $AN0_{-1}$ $D1$ 88 86 P10_7 $\overline{K13}$ $AN7$ 90 90 88 A6 P10_6 $\overline{K12}$ $AN6$ 91 91 89 B5 P10_4 $\overline{K10}$ $AN4$ 93 91 C5 $P10_{-3}$ $\overline{K17}$ $AN3$ 94 | 70 | 70 | A9 C9 | | P1_2 | | | | | |
| 80 78 $C7$ $C180/F186$ $D6$ 81 79 $A8$ $P0_{-7}$ $AN0_{-7}$ $D7$ 82 80 $B8$ $P0_{-6}$ $AN0_{-6}$ $D6$ 83 81 $D6$ $P0_{-5}$ $AN0_{-5}$ $D5$ 84 82 $B7$ $P0_{-4}$ $AN0_{-3}$ $D3$ 86 84 $B6$ $P0_{-2}$ $AN0_{-2}$ $D2$ 87 85 $C6$ $P0_{-1}$ $AN0_{-1}$ $D1$ 88 86 $E5$ $P0_{-0}$ $AN0_{-1}$ $D1$ 88 86 $E5$ $P0_{-0}$ $AN0_{-1}$ $D1$ 88 86 $P10_{-7}$ $\overline{K13}$ $AN7$ $O0$ 90 88 $A6$ $P10_{-6}$ $\overline{K12}$ $AN6$ $O0$ 91 89 $B5$ $P10_{-5}$ $\overline{K11}$ $AN5$ $O0$ 92 90 $A5$ $P10_{-1}$ $\overline{K17}$ $AN3$ $O0$ 94 92 <td>79</td> <td>70</td> <td>00</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>D9</td> | 79 | 70 | 00 | | | | | | | D9 |
| 81 79 A8 P0_7 AN0_7 D7 82 80 B8 P0_6 AN0_6 D6 83 81 D6 P0_5 AN0_6 D6 83 81 D6 P0_5 AN0_5 D5 84 82 B7 P0_4 AN0_3 D3 86 84 B6 P0_2 AN0_2 D2 87 85 C6 P0_1 AN0_1 D1 88 86 E5 P0_0 AN0_2 D2 89 87 D5 P10_7 KI3 AN7 90 88 A6 P10_6 KI2 AN6 91 89 B5 P10_5 KI1 AN5 92 90 A5 P10_4 KI0 AN4 93 91 C5 P10_3 KI7 AN3 94 92 B4 P10_2 KI6 AN2 95 93 A4 P10_1 KI5 AN1 96 94 <t< td=""><td>00</td><td>70</td><td>07</td><td></td><td></td><td></td><td></td><td>C156/R156</td><td></td><td>Do D7</td></t<> | 00 | 70 | 07 | | | | | C156/R156 | | Do D7 |
| 82 80 $P0_{-0}$ $AN0_{-0}$ $D0$ 83 81 $D6$ $P0_{-5}$ $AN0_{-5}$ $D5$ 84 82 $B7$ $P0_{-4}$ $AN0_{-4}$ $D4$ 85 83 $A7$ $P0_{-3}$ $AN0_{-3}$ $D3$ 86 84 $B6$ $P0_{-2}$ $AN0_{-1}$ $D1$ 87 85 $C6$ $P0_{-1}$ $AN0_{-1}$ $D1$ 88 86 $E5$ $P0_{-0}$ $AN0_{-1}$ $D1$ 88 86 $P10_{-7}$ $\overline{K13}$ $AN7$ $O0$ 90 88 $A6$ $P10_{-7}$ $\overline{K13}$ $AN7$ 90 88 $A6$ $P10_{-5}$ $\overline{K17}$ $AN6$ 91 89 $B5$ $P10_{-5}$ $\overline{K17}$ $AN4$ 93 91 $C5$ $P10_{-3}$ $\overline{K17}$ $AN3$ 94 92 $B4$ $P10_{-2}$ $\overline{K16}$ $AN1$ 96 94 $P10_{-0}$ $\overline{K14}$ | 81 | 79 | A8 D0 | | P0_7 | | | | ANU_7 | D7 |
| 83 81 D6 P0_3 ANU_5 D5 84 82 B7 P0_4 ANU_4 D4 85 83 A7 P0_3 ANU_3 D3 86 84 B6 P0_2 ANU_2 D2 87 85 C6 P0_1 ANU_2 D2 87 85 C6 P0_1 ANU_1 D1 88 86 E5 P0_0 ANU_0 D0 89 87 D5 P10_7 Ki3 ANT 00 90 88 A6 P10_6 Ki2 AN6 00 00 91 89 B5 P10_5 Ki1 ANS 00 00 92 90 A5 P10_4 Ki0 AN4 00 00 93 91 C5 P10_3 Ki7 AN3 00 00 94 92 B4 P10_2 Ki6 AN1 00 00 96 94 C4 AVSS AVI AN0 <td>02</td> <td>00</td> <td></td> <td></td> <td>P0_0</td> <td></td> <td></td> <td></td> <td></td> <td>D6</td> | 02 | 00 | | | P0_0 | | | | | D6 |
| 84 62 $B7$ $P0_{-4}$ $AN0_{-4}$ $D4$ 85 83 $A7$ $P0_{-3}$ $AN0_{-3}$ $D3$ 86 84 $B6$ $P0_{-2}$ $AN0_{-3}$ $D2$ 87 85 $C6$ $P0_{-1}$ $AN0_{-1}$ $D1$ 88 86 $E5$ $P0_{-0}$ $AN0_{-0}$ $D0$ 89 87 $D5$ $P10_{-7}$ $\overline{K13}$ $AN7$ 90 88 $A6$ $P10_{-6}$ $\overline{K12}$ $AN6$ 91 89 $B5$ $P10_{-5}$ $\overline{K11}$ $AN5$ 92 90 $A5$ $P10_{-4}$ $\overline{K10}$ $AN4$ 93 91 $C5$ $P10_{-3}$ $\overline{K17}$ $AN3$ 94 92 $B4$ $P10_{-2}$ $\overline{K16}$ $AN1$ $AN2$ 95 93 $A4$ $P10_{-1}$ $\overline{K15}$ $AN1$ $AN0$ 96 $A3$ $VREF$ $AN0$ $AN0$ $AN0$ $AN0$ 99 <td>83</td> <td>81</td> <td></td> <td></td> <td>P0_5</td> <td></td> <td></td> <td></td> <td></td> <td>D5</td> | 83 | 81 | | | P0_5 | | | | | D5 |
| 83 83 $A7$ $P0_{-3}$ $AN0_{-3}$ $D3$ 86 84 $B6$ $P0_{-2}$ $AN0_{-3}$ $D2$ 87 85 $C6$ $P0_{-1}$ $AN0_{-1}$ $D1$ 88 86 $E5$ $P0_{-0}$ $AN0_{-0}$ $D0$ 89 87 $D5$ $P10_{-7}$ $\overline{Kl3}$ $AN7$ 90 88 $A6$ $P10_{-6}$ $\overline{Kl2}$ $AN6$ 91 89 $B5$ $P10_{-5}$ $\overline{Kl1}$ $AN5$ 92 90 $A5$ $P10_{-4}$ $\overline{Kl0}$ $AN4$ 93 91 $C5$ $P10_{-3}$ $\overline{Kl7}$ $AN3$ 94 92 $B4$ $P10_{-2}$ $\overline{Kl6}$ $AN2$ 95 93 $A4$ $P10_{-1}$ $\overline{Kl5}$ $AN1$ 96 $A3$ $VREF$ $AN0$ $AN0$ 99 97 $B3$ $AVCC$ $AN0$ 99 97 $B3$ $AVCC$ $ADTEG$ <td>04</td> <td>02</td> <td></td> <td></td> <td>P0_4</td> <td></td> <td></td> <td></td> <td>AN0_4</td> <td>D4</td> | 04 | 02 | | | P0_4 | | | | AN0_4 | D4 |
| 30 64 B0 PO_2 D2 87 85 C6 PO_1 ANO_1 D1 88 86 E5 PO_0 ANO_0 D0 89 87 D5 P10_7 KI3 AN7 90 88 A6 P10_6 KI2 AN6 91 89 B5 P10_5 KI1 AN5 92 90 A5 P10_4 KI0 AN4 93 91 C5 P10_3 KI7 AN3 94 92 B4 P10_2 KI6 AN1 95 93 A4 P10_1 KI5 AN1 96 94 C4 AVS AN0 AN0 98 96 A3 VREF Image: C3 Image: C3 Image: C3 90 98 C3 P9.7 SIN4 ADTEG | 00 | 03 | A/ DC | | FU_3 | | | | AN0_3 | D3 |
| 87 83 C6 P0_1 ANO_1 D1 88 86 E5 P0_0 ANO_0 D0 89 87 D5 P10_7 Ki3 AN7 90 88 A6 P10_6 Ki2 AN6 91 89 B5 P10_5 Ki1 AN5 92 90 A5 P10_4 Ki0 AN4 93 91 C5 P10_3 Ki7 AN3 94 92 B4 P10_1 Ki6 AN1 95 93 A4 P10_1 Ki5 AN1 96 94 C4 AVSS AN0 AN0 98 96 A3 VREF AN0 AN0 99 97 B3 AVCC ANC ADTEG | 00 | 04 05 | | | FU_2 | | | | AN0_2 | D2 |
| 88 87 D5 P10_7 KI3 AN7 90 88 A6 P10_6 KI2 AN6 91 89 B5 P10_5 KI1 AN5 92 90 A5 P10_4 KI0 AN4 93 91 C5 P10_3 KI7 AN3 94 92 B4 P10_2 KI6 AN1 95 93 A4 P10_1 KI5 AN1 96 94 C4 AVSS AN0 AN0 97 95 D4 P10_0 KI4 AN0 98 96 A3 VREF AN0 AN0 99 97 B3 AVCC AVC AN0 100 98 C3 P97 SIN4 ADTEG | 07 | 00 | 5 | | | | | | | |
| 03 07 D3 P10_7 KI3 AN7 90 88 A6 P10_6 KI2 AN6 91 89 B5 P10_5 KI1 AN5 92 90 A5 P10_4 KI0 AN4 93 91 C5 P10_3 KI7 AN3 94 92 B4 P10_2 KI6 AN2 95 93 A4 P10_1 KI5 AN1 96 94 C4 AVSS AN0 AN0 97 95 D4 P10_0 KI4 AN0 98 96 A3 VREF AN0 AN0 99 97 B3 AVCC AVC AN0 100 98 C3 P97 SIN4 ADTEG | 00 | 00 | | | P10_0 | IZIO | | | | |
| 90 88 A0 P10_6 Kl2 AN6 91 89 B5 P10_5 Kl1 AN5 92 90 A5 P10_4 Kl0 AN4 93 91 C5 P10_3 Kl7 AN3 94 92 B4 P10_2 Kl6 AN2 95 93 A4 P10_1 Kl5 AN1 96 94 C4 AVSS AN0 AN0 97 95 D4 P10_0 Kl4 AN0 AN0 98 96 A3 VREF AN0 AN0 99 97 B3 AVCC AVCE AN0 100 98 C3 P97 SIN4 ADTEG | 09 | 0/ | 05 | | | KI3 100 | | | | |
| 91 89 B5 P10_5 KI1 AN5 92 90 A5 P10_4 Ki0 AN4 93 91 C5 P10_3 Ki7 AN3 94 92 B4 P10_2 Ki6 AN2 95 93 A4 P10_1 Ki5 AN1 96 94 C4 AVSS AN0 AN0 97 95 D4 P10_0 Ki4 AN0 98 96 A3 VREF AN0 AN0 99 97 B3 AVCC AVC AN0 100 98 C3 P97 SIN4 ADTEG | 90 | 88 | A6 | | P10_6 | KI2 | | | ANG | |
| 92 90 A5 P10_4 Ki0 AN4 93 91 C5 P10_3 Ki7 AN3 94 92 B4 P10_2 Ki6 AN2 95 93 A4 P10_1 Ki5 AN1 96 94 C4 AVSS AN0 AN0 97 95 D4 P10_0 Ki4 AN0 98 96 A3 VREF AN0 AN0 99 97 B3 AVCC AVCE ADTEG | 91 | 89 | B5 | | P10_5 | KI1 | | | AN5 | |
| 93 91 C5 P10_3 KI7 AN3 94 92 B4 P10_2 KI6 AN2 95 93 A4 P10_1 KI5 AN1 96 94 C4 AVSS AN0 97 95 D4 P10_0 KI4 AN0 98 96 A3 VREF VREF AN0 99 97 B3 AVCC AVCC AVC 100 98 C3 P9 7 SIN4 ADTEG | 92 | 90 | A5 | | P10_4 | KI0 | | | AN4 | |
| 94 92 B4 P10_2 KI6 AN2 95 93 A4 P10_1 KI5 AN1 96 94 C4 AVSS AN1 97 95 D4 P10_0 KI4 AN0 98 96 A3 VREF VREF AN0 99 97 B3 AVCC AVCC AVCC 100 98 C3 P9 7 SIN4 ADTEG | 93 | 91 | C5 | | P10_3 | KI7 | | | AN3 | |
| 95 93 A4 P10_1 KI5 AN1 96 94 C4 AVSS 97 95 D4 P10_0 KI4 AN0 98 96 A3 VREF 99 97 B3 AVCC 100 98 C3 P9 7 SIN4 ADTRG | 94 | 92 | B4 | | P10_2 | KI6 | | | AN2 | |
| 96 94 C4 AVSS AVSS 97 95 D4 P10_0 KI4 AN0 98 96 A3 VREF Image: Comparison of the second seco | 95 | 93 | A4 | | P10 1 | KI5 | | | AN1 | |
| 97 95 D4 P10_0 KI4 AN0 98 96 A3 VREF 99 97 B3 AVCC 100 98 C3 P9 7 SIN4 ADTEG | 96 | 94 | C4 | AVSS | | | | | | |
| 98 96 A3 VREF 99 97 B3 AVCC 90 97 SIN4 ADTRG 90 97 | 97 | 95 | D4 | | P10_0 | KI <u>A</u> | | | AN0 | |
| 99 97 B3 AVCC 100 98 C3 P9 7 SIN4 ADTRG | 98 | 96 | A3 | VRFF | | | | | | |
| 100 98 C3 P9 7 SIN4 ADTRG | 99 | 97 | B3 | AVCC | | | | | | |
| | 100 | 98 | C3 | | P9 7 | | | SIN4 | | |

 Table 1.7
 Pin Names for the 100-Pin Package (2/2)



1.6 Pin Functions

| Signal Name | Pin Name | I/O | Power Supply | Description |
|--------------------------------------|--|-----|--------------|--|
| Power supply input | VCC1, VCC2, VSS | Ι | - | Apply 1.8 to 5.5 V to pins VCC1 and VCC2 (VCC1 \ge VCC2) and 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | I | VCC1 | This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS. |
| Reset input | RESET | | VCC1 | Driving this pin low resets the MCU. |
| CNVSS | CNVSS | I | VCC1 | Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1. |
| External data bus width select input | BYTE | I | VCC1 | Input pin to select the data bus of the external area. The data bus is 16 bits when it is low, and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode. |
| | D0 to D7 | I/O | VCC2 | Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus. |
| | D8 to D15 | I/O | VCC2 | Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus. |
| | A0 to A19 | 0 | VCC2 | Outputs address bits A0 to A19. |
| | A0/D0 to A7/D7 | I/O | VCC2 | Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus. |
| | A1/D0 to A8/D7 | I/O | VCC2 | Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus. |
| | $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ | 0 | VCC2 | Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area. |
| Bus control pins | WRL/WR WRH/BHE RD | Ο | VCC2 | Outputs WRL, WRH, (WR, BHE), and RD signals. WRL and WRH can be switched with BHE and WR. WRL, WRH, and RD selected If the external data bus is 16 bits, data is written to an even address in an external area when WRL is driven low. Data is written to an odd address when WRH is driven low. Data is read when RD is driven low. WR, BHE, and RD selected Data is written to an external area when WR is driven low. Data is written to an external area when RD is driven low. WR, BHE, and RD selected Data is written to an external area when RD is driven low. An odd address is accessed when BHE is driven low. Select WR, BHE, and RD when using an 8-bit external data bus. |
| | ALE | 0 | VCC2 | Outputs an ALE signal to latch the address. |
| | HOLD | Ι | VCC2 | $\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up). |
| | HLDA | 0 | VCC2 | In a hold state, HLDA outputs a low-level signal. |
| | RDY | I | VCC2 | The MCU bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is driven low. |

Table 1.10Pin Functions for the 100-Pin Package (1/3)

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

3. Address Space

3.1 Address Space

The M16C/63 Group has a 1 MB address space from 00000h to FFFFFh. Address space is expandable to 4 MB with the memory area expansion function. Addresses 40000h to BFFFFh can be used as external areas from bank 0 to bank 7. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.



Figure 3.1 Address Space



3.2 Memory Map

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank areas within SFRs are reserved. Do not access these areas.

Internal RAM is allocated from address 00400h and higher, with 10 KB of internal RAM allocated from 00400h to 02BFFh. Internal RAM is used not only for data storage, but also for the stack area when subroutines are called or when an interrupt request is accepted.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is allocated from 0E000h to 0FFFFh. This data flash area is mostly used for data storage, but can also store programs.

Program ROM 2 is allocated from 10000h to 13FFFh. Program ROM 1 is allocated from FFFFFh and lower, with the 64 KB program ROM 1 area allocated from address F0000h to FFFFFh.

The special page vectors are allocated from FFE00h to FFFD7h. They are used for the JMPS and JSRS instructions. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts is allocated from FFFDCh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

Figure 3.2 shows the Memory Map.



Figure 3.2 Memory Map



| Address | Register | Symbol | Reset Value |
|---------|------------------------------------|--------|-----------------------------|
| 0210h | | - | 00h |
| 0211h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0212h | | | X0h |
| 0213h | | | |
| 0210h | | | 00b |
| 0214h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0215h | | RIMADI | X0h |
| 021011 | | | 2011 |
| 02171 | | | 0.01- |
| 0218h | | DIADO | 00h |
| 0219h | Address Match Interrupt Register 2 | RMAD2 | UUh |
| 021Ah | | | XUh |
| 021Bh | | | |
| 021Ch | | | 00h |
| 021Dh | Address Match Interrupt Register 3 | RMAD3 | 00h |
| 021Eh | | | X0h |
| 021Fh | | | |
| | | | 0000 0001b |
| 0220h | Elash Memory Control Register 0 | EMBO | (Other than user boot mode) |
| 022011 | | TIMIXO | 0010 0001b |
| | | | (User boot mode) |
| 0221h | Flash Memory Control Register 1 | FMR1 | 00X0 XX0Xb |
| 0222h | Flash Memory Control Register 2 | FMR2 | XXXX 0000b |
| 0223h | Flash Memory Control Register 3 | FMR3 | XXXX 0000b |
| 0224h | | | |
| 0225h | | | |
| 0226h | | | |
| 0227h | | | |
| 0228h | | | |
| 0229h | | | |
| 022Ah | | | |
| 022Bh | | | |
| 022Ch | | | |
| 0220h | | | |
| 022Eh | | | |
| 022EH | | | |
| 0221 h | Elach Mamany Control Pagistar 6 | EMD6 | XX0X XX00b |
| 023011 | | FININO | ~~~~~~~~ |
| 023111 | | | |
| 0232h | | | |
| 0233h | | | |
| 0234h | | | |
| 0235h | | | |
| 0236h | | | |
| 0237h | | | |
| 0238h | | | |
| 0239h | | | |
| 023Ah | | | |
| 023Bh | | | |
| 023Ch | | | |
| 023Dh | | | |
| 023Eh | | T | |
| 023Fh | | | |

Table 4.8SFR Information (8) (1)

X: Undefined

Note: 1. The blank areas are reserved. No access is allowed.



| Address | Register | Symbol | Reset Value |
|---------|-----------------------------|--------|--------------|
| 03F0h | Port P8 Register | P8 | XXh |
| 03F1h | Port P9 Register | P9 | XXh |
| 03F2h | Port P8 Direction Register | PD8 | 00h |
| 03F3h | Port P9 Direction Register | PD9 | 00h |
| 03F4h | Port P10 Register | P10 | XXh |
| 03F5h | | | |
| 03F6h | Port P10 Direction Register | PD10 | 00h |
| 03F7h | | | |
| 03F8h | | | |
| 03F9h | | | |
| 03FAh | | | |
| 03FBh | | | |
| 03FCh | | | |
| 03FDh | | | |
| 03FEh | | | |
| 03FFh | | | |
| | • | • | X: Undefined |

Table 4.17SFR Information (17) (1)

Note:

1. The blank areas are reserved. No access is allowed.



| Function | Mnemonic |
|----------------------|--|
| Transfer | MOV <i>Dir</i> |
| Bit processing | BCLR, BMCnd, BNOT, BSET, BTSTC, and BTSTS |
| Shifting | ROLC, RORC, ROT, SHA, and SHL |
| Arithmetic operation | ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB |
| Decimal operation | DADC, DADD, DSBB, and DSUB |
| Logical operation | AND, NOT, OR, and XOR |
| Jump | ADJNZ, SBJNZ |

Table 4.20 Read-Modify-Write Instructions



5.1.6 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 5.12 Voltage Detector 0 Electrical Characteristics

The measurement condition is V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | | Lloit | | |
|---------------------|---|--|------|-------|------|-------|
| Symbol | i arameter | Condition | Min. | Тур. | Max. | Offic |
| V _{det0} | Voltage detection level Vdet0_0 ⁽¹⁾ | When V _{CC1} is falling. | 1.80 | 1.90 | 2.10 | V |
| | Voltage detection level Vdet0_2 ⁽¹⁾ | When V _{CC1} is falling. | 2.70 | 2.85 | 3.00 | V |
| - | Voltage detector 0 response time ⁽³⁾ | When V _{CC1} falls from 5 V to (Vdet0_0 - 0.1) V | | | 200 | μS |
| - | Voltage detector self power consumption | VC25 = 1, V _{CC1} = 5.0 V | | 1.5 | | μΑ |
| t _{d(E-A)} | Waiting time until voltage detector operation starts ⁽²⁾ | | | | 100 | μS |

Notes:

1. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.

- 2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
- 3. Time from when passing the V_{det0} until when a voltage monitor 0 reset is generated.

Table 5.13 Voltage Detector 1 Electrical Characteristics

The measurement condition is V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

| Symbol | Peremeter | Condition | : | Linit | | |
|---------------------|---|--|------|-------|------|------|
| Symbol | Falameter | Condition | Min. | Тур. | Max. | Unit |
| V _{det1} | Voltage detection level Vdet1_0 ⁽¹⁾ | When V _{CC1} is falling. | 1.90 | 2.20 | 2.50 | V |
| | Voltage detection level Vdet1_6 ⁽¹⁾ | When V _{CC1} is falling. | 2.80 | 3.10 | 3.40 | V |
| | Voltage detection level Vdet1_B (1) | When V _{CC1} is falling. | 3.55 | 3.85 | 4.15 | V |
| | Voltage detection level Vdet1_F (1) | When V _{CC1} is falling. | 4.15 | 4.45 | 4.75 | V |
| - | Hysteresis width at the rising of V_{CC1} in voltage | When selecting Vdet1_0 | | 0.10 | | V |
| | detector 1 | When selecting Vdet1_6 to Vdet1_F | | 0.15 | | V |
| - | Voltage detector 1 response time ⁽³⁾ | When V _{CC1} falls from 5 V to (Vdet1_0 - 0.1) V | | | 200 | μs |
| - | Voltage detector self power consumption | VC26 = 1, V _{CC1} = 5.0 V | | 1.7 | | μΑ |
| t _{d(E-A)} | Waiting time until voltage detector operation starts ⁽²⁾ | | | | 100 | μs |

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.

2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC26 bit in the VCR2 register to 0.

3. Time from when passing the V_{det1} until when a voltage monitor 1 reset is generated.



5.1.7 Oscillator Electrical Characteristics

Table 5.17 40 MHz On-Chip Oscillator Electrical Characteristics

 V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | ę | Linit | | |
|---------------------------|---|---|------|-------|------|------|
| Symbol | | Condition | Min. | Тур. | Max. | Unit |
| f _{OCO40M} | 40 MHz on-chip oscillator frequency | Average frequency in a 10 ms period 2.7 V \leq V _{CC1} < 5.5 V | 36 | 40 | 44 | MHz |
| | | Average frequency in a 10 ms period 1.8 V \leq V _{CC1} < 2.7 V | 30 | 40 | 50 | MHz |
| tsu(f _{OCO40M}) | Wait time until 40 MHz on-chip oscillator stabilizes | | | | 2 | ms |

Table 5.18 125 kHz On-Chip Oscillator Electrical Characteristics

 V_{CC1} = 1.8 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | 5 | Unit | | | |
|--------------------------|--|-------------------------------------|-----|------|------|-------|--|
| Cymbol | T diameter | Min. Typ | | Тур. | Max. | Offic | |
| foco-s | 125 kHz on-chip oscillator frequency | Average frequency in a 10 ms period | 100 | 125 | 150 | kHz | |
| tsu(f _{OCO-S}) | Wait time until 125 kHz on-chip oscillator stabilizes | | | | 20 | μs | |







 $V_{CC1} = V_{CC2} = 5 V$

Switching Characteristics

 $(V_{CC1} = V_{CC2} = 5 \text{ V}, V_{SS} = 0 \text{ V}, \text{ at } T_{opr} = -20^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}/-40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C} \text{ unless otherwise specified})$

5.2.4.4 In Wait State Setting $2\phi + 3\phi$, $2\phi + 4\phi$, $3\phi + 4\phi$, and $4\phi + 5\phi$, and When Accessing External Area

Table 5.39Memory Expansion Mode and Microprocessor Mode (in Wait State Setting 2 ϕ + 3 ϕ , 2 ϕ + 4 ϕ , 3 ϕ + 4 ϕ , and 4 ϕ + 5 ϕ , and When Accessing External Area)

| Symbol | Parameter | Measuring | Stan | Linit | | |
|---------------------------|--|--------------------|----------|-------|------|--|
| Symbol | Falailletei | Condition Min. Max | | Max. | Onic | |
| t _{d(BCLK-AD)} | Address output delay time | | | 25 | ns | |
| t _{h(BCLK-AD}) | Address output hold time (in relation to BCLK) | | 0 | | ns | |
| t _{h(RD-AD}) | Address output hold time (in relation to RD) | | 0 | | ns | |
| t _{h(WR-AD)} | Address output hold time (in relation to WR) | | (Note 2) | | ns | |
| t _{d(BCLK-CS)} | Chip select output delay time | | | 25 | ns | |
| t _{h(BCLK-CS)} | Chip select output hold time (in relation to BCLK) | | 0 | | ns | |
| t _{d(BCLK-ALE)} | ALE signal output delay time | | | 15 | ns | |
| t _{h(BCLK-ALE}) | ALE signal output hold time | See | -4 | | ns | |
| t _{d(BCLK-RD)} | RD signal output delay time | Figure 5.15 | | 25 | ns | |
| t _{h(BCLK-RD)} | RD signal output hold time | | 0 | | ns | |
| t _{d(BCLK-WR)} | WR signal output delay time | | | 25 | ns | |
| t _{h(BCLK-WR)} | WR signal output hold time | | 0 | | ns | |
| t _{d(BCLK-DB)} | Data output delay time (in relation to BCLK) | | | 40 | ns | |
| t _{h(BCLK-DB)} | Data output hold time (in relation to BCLK) ⁽³⁾ | | 0 | | ns | |
| t _{d(DB-WR)} | Data output delay time (in relation to WR) | | (Note 1) | | ns | |
| t _{h(WR-DB)} | Data output hold time (in relation to WR) $^{(3)}$ | | (Note 2) | | ns | |

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)\times10^9}{f_{(BCLK)}} - 40[ns] \qquad \text{n is 3 for } 2\phi + 3\phi, 4 \text{ for } 2\phi + 4\phi, 4 \text{ for } 3\phi + 4\phi, \text{ and 5 for } 4\phi + 5\phi.$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus. Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value. Hold time of data bus is expressed in $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$ by a circuit of the right figure. For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 k Ω , hold time of output low level is t = -30 pF x 1 k $\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$ = 6.7 ns.







Figure 5.20 Timing Diagram



 $V_{CC1} = V_{CC2} = 3 V$

Timing Requirements

 $(V_{CC1} = V_{CC2} = 3 \text{ V}, V_{SS} = 0 \text{ V}, \text{ at } T_{opr} = -20^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}/-40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C} \text{ unless otherwise specified})$

5.3.2.3 Timer A Input

Table 5.45 Timer A Input (Counter Input in Event Counter Mode)

| Symbol | Parameter | Standard Min. M | dard | Unit |
|---------------------|------------------------------|--------------------|------|------|
| | i arameter | | Max. | |
| t _{c(TA)} | TAilN input cycle time | 150 | | ns |
| t _{w(TAH)} | TAilN input high pulse width | 60 | | ns |
| t _{w(TAL)} | TAilN input low pulse width | 60 | | ns |

Table 5.46 Timer A Input (Gating Input in Timer Mode)

| Symbol | Parameter | Standard Min. Max. | Unit | |
|---------------------|------------------------------|-----------------------|------|----|
| | | | | |
| t _{c(TA)} | TAIIN input cycle time | 600 | | ns |
| t _{w(TAH)} | TAiIN input high pulse width | 300 | | ns |
| t _{w(TAL)} | TAilN input low pulse width | 300 | | ns |

Table 5.47 Timer A Input (External Trigger Input in One-Shot Timer Mode)

| Symbol | Parameter | Standard | | Unit |
|---------------------|------------------------------|-----------|--|------|
| | i alameter | Min. Max. | | |
| t _{c(TA)} | TAiIN input cycle time | 300 | | ns |
| t _{w(TAH)} | TAiIN input high pulse width | 150 | | ns |
| t _{w(TAL)} | TAiIN input low pulse width | 150 | | ns |

Table 5.48Timer A Input (External Trigger Input in Pulse Width Modulation Mode and
Programmable Output Mode)

| Symbol | Parameter | Stan | dard | Linit |
|---------------------|---------------------------------|-----------|------|-------|
| | | Min. Max. | | Offic |
| t _{w(TAH)} | TAilN input high pulse width | 150 | | ns |
| t _{w(TAL)} | TAilN input low pulse width 150 | | | ns |



Figure 5.23 Timer A Input



$V_{CC1} = V_{CC2} = 3 V$

Timing Requirements

 $(V_{CC1} = V_{CC2} = 3 \text{ V}, V_{SS} = 0 \text{ V}, \text{ at } T_{opr} = -20^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}/-40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C} \text{ unless otherwise specified})$

| Table 5.49 Timer A Input (Two-Phase Pulse Input in Event Count | ter Mode) |
|--|-----------|
|--|-----------|

| Symbol | Parameter | Standard | | Unit |
|-----------------------------|-------------------------|-----------|------|------|
| | i didineter | Min. Max. | Max. | Onit |
| t _{c(TA)} | TAilN input cycle time | 2 | | μS |
| t _{su(TAIN-TAOUT)} | TAiOUT input setup time | 500 | | ns |
| t _{su(TAOUT-TAIN)} | TAiIN input setup time | 500 | | ns |



Figure 5.24 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)



 $V_{CC1} = V_{CC2} = 3 V$

Switching Characteristics

 $(V_{CC1} = V_{CC2} = 3 \text{ V}, V_{SS} = 0 \text{ V}, \text{ at } T_{opr} = -20^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}/-40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C} \text{ unless otherwise specified})$

5.3.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.59Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When
Accessing External Area and Using Multiplexed Bus) ⁽⁵⁾

| Symbol | Deremeter | Measuring | Stan | dard | Lloit | |
|--------------------------|---|--------------------|----------|------|-------|--|
| Symbol | Faiametei | Condition | Min. | Max. | 0111 | |
| t _{d(BCLK-AD)} | Address output delay time | | | 50 | ns | |
| t _{h(BCLK-AD)} | Address output hold time (in relation to BCLK) | | 0 | | ns | |
| t _{h(RD-AD)} | Address output hold time (in relation to RD) | | (Note 1) | | ns | |
| t _{h(WR-AD)} | Address output hold time (in relation to WR) | | (Note 1) | | ns | |
| t _{d(BCLK-CS)} | Chip select output delay time | | | 50 | ns | |
| t _{h(BCLK-CS)} | Chip select output hold time (in relation to BCLK) | | 0 | | ns | |
| t _{h(RD-CS)} | Chip select output hold time (in relation to RD) | | (Note 1) | | ns | |
| t _{h(WR-CS)} | Chip select output hold time (in relation to WR) | | (Note 1) | | ns | |
| t _{d(BCLK-RD)} | RD signal output delay time | | | 40 | ns | |
| t _{h(BCLK-RD)} | RD signal output hold time | | 0 | | ns | |
| t _{d(BCLK-WR)} | WR signal output delay time | 0 | | 40 | ns | |
| t _{h(BCLK-WR)} | WR signal output hold time | See Figure 5.30 | 0 | | ns | |
| t _{d(BCLK-DB)} | Data output delay time (in relation to BCLK) | J | | 50 | ns | |
| t _{h(BCLK-DB)} | Data output hold time (in relation to BCLK) | | 0 | | ns | |
| t _{d(DB-WR)} | Data output delay time (in relation to WR) | | (Note 2) | | ns | |
| t _{h(WR-DB)} | Data output hold time (in relation to WR) | | (Note 1) | | ns | |
| t _{d(BCLK-ALE)} | ALE signal output delay time (in relation to BCLK) | | | 25 | ns | |
| t _{h(BCLK-ALE)} | ALE signal output hold time (in relation to BCLK) | | -4 | | ns | |
| t _{d(AD-ALE)} | ALE signal output delay time (in relation to Address) | | (Note 3) | | ns | |
| t _{h(AD-ALE)} | ALE signal output hold time (in relation to Address) | | (Note 4) | | ns | |
| t _{d(AD-RD)} | RD signal output delay from the end of address | | 0 | | ns | |
| t _{d(AD-WR)} | WR signal output delay from the end of address | | 0 | | ns | |
| t _{dz(RD-AD)} | Address output floating start time | | | 8 | ns | |

Notes:

1. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 50[ns] \qquad \text{n is 2 for 2 waits setting, 3 for 3 waits setting.}$$

3. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$$

4. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$$

5. When using multiplexed bus, set $f_{(BCLK)}$ 12.5 MHz or less.



$V_{CC1} = V_{CC2} = 1.8 V$

Timing Requirements

 $(V_{CC1} = V_{CC2} = 1.8 \text{ V}, V_{SS} = 0 \text{ V}, \text{ at } T_{opr} = -20^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}/-40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}$ unless otherwise specified)

5.4.2.4 Timer B Input

Table 5.72 Timer B Input (Counter Input in Event Counter Mode)

| Symbol | Parameter | Standard | Unit | | |
|---------------------|--|----------|-----------|----|--|
| Gymbol | | Min. | Min. Max. | | |
| t _{c(TB)} | TBiIN input cycle time (counted on one edge) | 300 | | ns | |
| t _{w(TBH)} | TBiIN input high pulse width (counted on one edge) | 120 | | ns | |
| t _{w(TBL)} | TBiIN input low pulse width (counted on one edge) | 120 | | ns | |
| t _{c(TB)} | TBilN input cycle time (counted on both edges) 600 | | | | |
| t _{w(TBH)} | TBiIN input high pulse width (counted on both edges) | 240 | | ns | |
| t _{w(TBL)} | TBiIN input low pulse width (counted on both edges) | 240 | | ns | |

Table 5.73 Timer B Input (Pulse Period Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|---------------------|------------------------------|-----------|------|-------|
| | i alameter | Min. Max. | Max. | Offic |
| t _{c(TB)} | TBiIN input cycle time | 1000 | | ns |
| t _{w(TBH)} | TBiIN input high pulse width | 500 | | ns |
| t _{w(TBL)} | TBiIN input low pulse width | 500 | | ns |

Table 5.74 Timer B Input (Pulse Width Measurement Mode)

| Symbol | Parameter | Standard Min. Max. | dard | Lloit |
|----------------------|------------------------------|-----------------------|-------|-------|
| | i didificici | | Offic | |
| t _{c(TB)} | TBiIN input cycle time | 1000 | | ns |
| t _{w(TBH}) | TBiIN input high pulse width | 500 | | ns |
| t ^{w(TBL)} | TBiIN input low pulse width | 500 | | ns |



Figure 5.40 Timer B Input



REVISION HISTORY

M16C/63 Group Datasheet

| D | Data | | Description |
|-------------------|-----------------------|---|---|
| Rev. | Date | Page | Summary |
| 2.00 Feb 07, 2011 | 71 to 78, 92 to 99 | Table 5.35 to Table 5.40 and Table 5.56 to Table 5.61 Memory Expansion Mode and Microprocessor Mode: Deleted the following: • HOLD input setup time • HOLD input hold time • HLDA output delay time | |
| | | 72, 93 | Figure 5.14 and Figure 5.29 Timing Diagram: Deleted lower figure (Common to wait state and no wait state settings). |
| | | 83, 104 | Figure 5.20 and Figure 5.35 Timing Diagram: Changed the width of th(RD-AD). |
| | | 84 | Table 5.41 Electrical Characteristics (1): Added rows for the CEC value to V_{OL}, V_{T+}-V_{T-}, and Leakage current in powered-off state. Added "ZP, IDU, IDV, IDW" to the V_{T+} - V_{T-} row. |
| | | 85 | Table 5.42 Electrical Characteristics (2): Changed "VCC1 = 5.0 V" to "VCC1 = 3.0 V" in the During flash memory program and During flash memory erase rows. |
| | | 92 | Table 5.56 Memory Expansion Mode and Microprocessor Mode:Changed RDY input setup time from 40. |
| | | 105 | Table 5.62 Electrical Characteristics (1): Changed the Measuring Condition over the table. Added "ZP, IDU, IDV, IDW" to the Parameter column and the value to the Measuring Condition in the V_{T+} - V_{T-} row. Changed the Measuring Condition in the I_{IH} row. |
| | | 106, 107 | Table 5.63 Electrical Characteristics (2) and Table 5.64 Electrical Characteristics (3): Changed the Measuring Condition over the table. |
| | | 108 | Table 5.66 External Clock Input (XIN Input): Changed the condition in note 1. |
| 2.20 | Nov 01, 2012 | Overview | |
| | | 2 | Table 1.1 Specifications for the 100-Pin Package (1/2): Added the condition for 100.0 ns and changed the condition for 200 ns in the Minimum instruction execution time in the Description column of the CPU. |
| | | 3 | Table 1.2 Specifications for the 100-Pin Package (2/2): Added "10 MHz/VCC1 = 2.1 to 5.5 V, VCC2 = 2.1 V to VCC1" to the Description column of the Operation Frequency/Supply Voltage. |
| | | 4 | Table 1.3 Specifications for the 80-Pin Package (1/2): Added the condition for 100.0 ns and changed the condition for 200 ns in the Minimum instruction execution time in the Description column of the CPU. |
| | | 5 | Table 1.4 Specifications for the 80-Pin Package ($2/2$): Added "10 MHz/VCC1 = 2.1 to 5.5 V" to the Description column of the Operation Frequency/Supply Voltage. |
| | | Electrical Ch | aracteristics |
| | | 52 | Table 5.4 Recommended Operating Conditions (3/4)• Changed the Parameter "2.7 V $\leq V_{CC1} < 5.5$ V" to "2.7 V $\leq V_{CC1} < 5.5$ V, 1 MHz $\leq f_{(XIN)} \leq 20$ MHz" in $f_{(BCLK)}$.• Added the line for "2.1 V $\leq V_{CC1} < 2.7$ V, 1 MHz $\leq f(XIN) \leq 10$ MHz" in $f_{(BCLK)}$.• Changed the Parameter "1.8 V $\leq V_{CC1} < 2.7$ V" to "1.8 V $\leq V_{CC1} < 2.1$ V, 1 MHz $\leq f_{(XIN)} \leq 10$ |
| | | 53 | MHz" in $f_{(BCLK)}$. |
| 1 | 1 | 00 | $ GCLK $ and v_{CC1} . Nounce the range of 2.1 $v \ge v_{CC1} < 2.7 v$. |

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do
 not access these addresses; the correct operation of LSI is not guaranteed if they are
 accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.