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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f363amdfa-u0

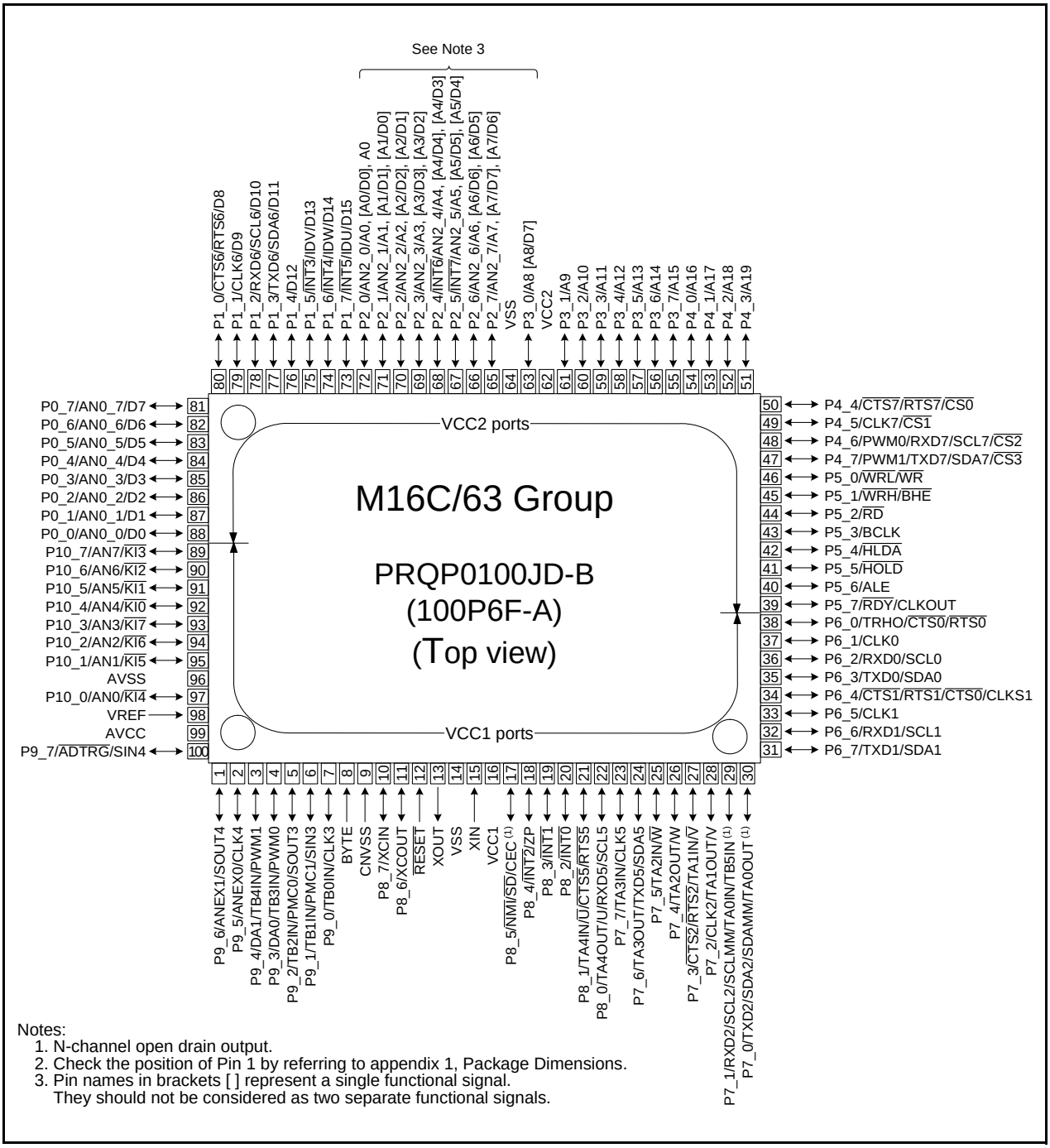
Table 1.2 Specifications for the 100-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2) • On-chip dead time timer
	Real-time clock	• Count: seconds, minutes, hours, days of the week, months, years • Periodic interrupt: 0.25 s, 0.5 s • Automatic correction function
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus, special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 2.15 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		5 MHz/VCC1 = 1.8 to 5.5 V, VCC2 = 1.8 V to VCC1 10 MHz/VCC1 = 2.1 to 5.5 V, VCC2 = 2.1 V to VCC1 20 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		Described in Electrical Characteristics
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		100-pin QFP: PRQP0100JD-B (Previous package code: 100P6F-A) 100-pin LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A) 100-pin LGA: PTLG0100KA-A (Previous package code: 100F0M)

Notes:
1. See Table 1.5 “Product List” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

1.5 Pin Assignments

Figure 1.6 to Figure 1.9 show pin assignments. Table 1.6 to Table 1.9 list pin names.



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

Figure 1.6 Pin Assignment for the 100-Pin Package

Table 1.8 Pin Names for the 80-Pin Package (1/2)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function			
			Interrupt	Timer	Serial interface	A/D converter, D/A converter
1		P9_5			CLK4	ANEX0
2		P9_4		TB4IN/PWM1		DA1
3		P9_3		TB3IN/PWM0		DA0
4		P9_2		TB2IN/PMC0	SOUT3	
5		P9_0		TB0IN	CLK3	
6	CNVSS					
7	XCIN	P8_7				
8	XCOUT	P8_6				
9	$\overline{\text{RESET}}$					
10	XOUT					
11	VSS					
12	XIN					
13	VCC1					
14		P8_5	$\overline{\text{NMI}}$		CEC	
15		P8_4	$\overline{\text{INT2}}$	ZP		
16		P8_3	$\overline{\text{INT1}}$			
17		P8_2	$\overline{\text{INT0}}$			
18		P8_1		TA4IN	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	
19		P8_0		TA4OUT	RXD5/SCL5	
20		P7_7		TA3IN	CLK5	
21		P7_6		TA3OUT	TXD5/SDA5	
22		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM	
23		P7_0		TA0OUT	TXD2/SDA2/SDAMM	
24		P6_7			TXD1/SDA1	
25		P6_6			RXD1/SCL1	
26		P6_5			CLK1	
27		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/ CLKS1	
28		P6_3			TXD0/SDA0	
29		P6_2			RXD0/SCL0	
30		P6_1			CLK0	
31		P6_0		TRHO	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	
32	CLKOUT	P5_7				
33		P5_6				
34		P5_5				
35		P5_4				
36		P5_3				
37		P5_2				
38		P5_1				
39		P5_0				
40		P4_3				

Table 1.13 Pin Functions for the 80-Pin Package (1/2)

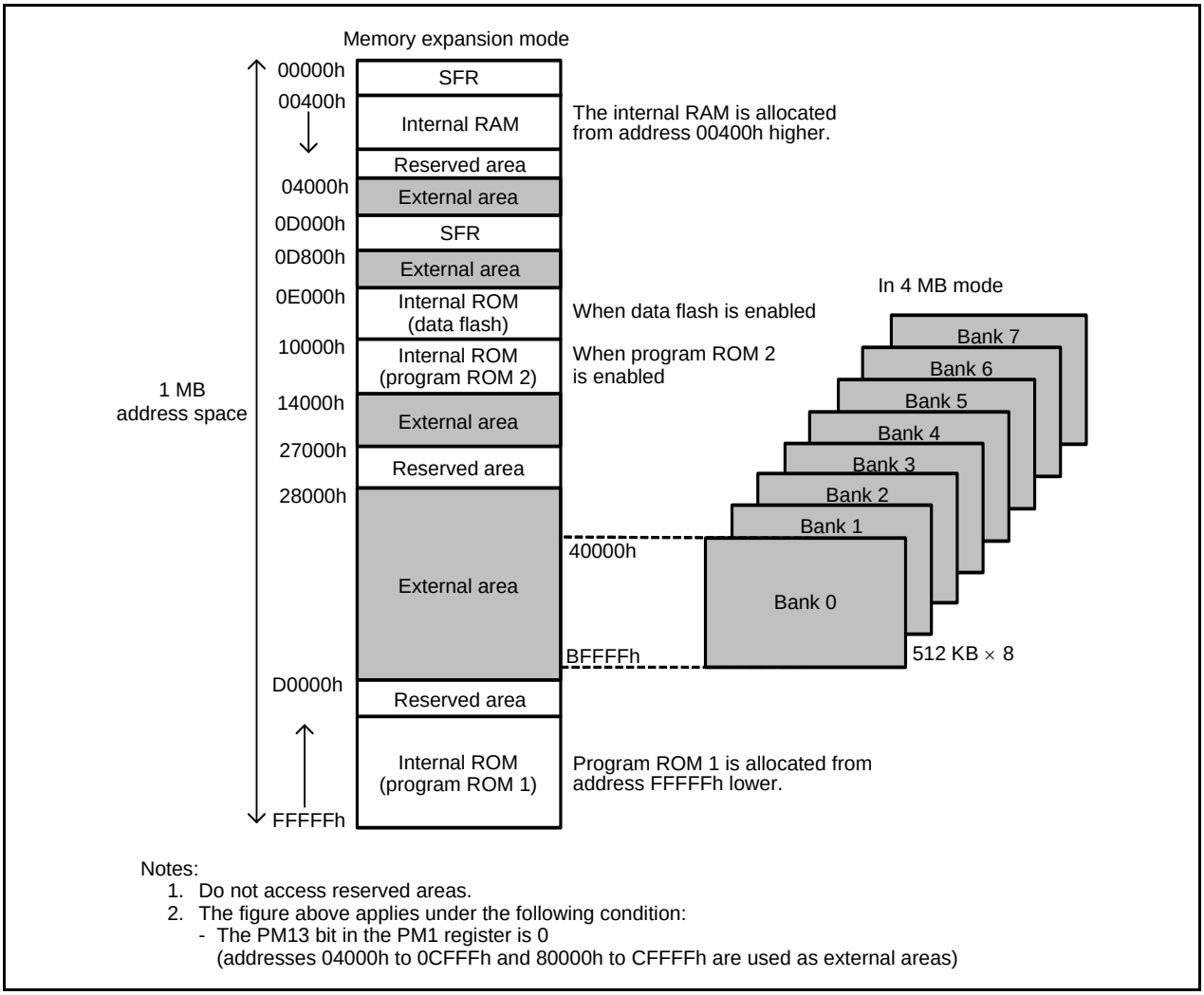
Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VSS	I	-	Apply 1.8 to 5.5 V to the VCC1 pin and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor.
Main clock input	XIN	I	VCC1	I/O pins for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. (1) Input an external clock to XIN pin and leave XOUT pin open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. (1) Input an external clock to XCIN pin and leave XCOUT pin open.
Sub clock output	XCOUT	O	VCC1	
Clock output	CLKOUT	O	VCC1	Outputs a clock with the same frequency as fC, f1, f8, or f32.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input for the $\overline{\text{INT}}$ interrupt.
	$\overline{\text{INT6}}$, $\overline{\text{INT7}}$	I	VCC1	
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input for the $\overline{\text{NMI}}$ interrupt.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	VCC1	Input for the key input interrupt.
Timer A	TA0OUT, TA3OUT, TA4OUT	I/O	VCC1	I/O for timers A0, A3, and A4 (TA0OUT is N-channel open drain output).
	TA0IN, TA3IN, TA4IN	I	VCC1	Input for timers A0, A3, and A4.
	ZP	I	VCC1	Input for Z-phase.
Timer B	TB0IN, TB2IN to TB5IN	I	VCC1	Input for timers B0, and B2 to B5.
Real-time clock output	TRHO	O	VCC1	Output for the real-time clock.
PWM output	PWM0, PWM1	O	VCC1	PWM output.
Remote control signal receiver input	PMC0	I	VCC1	Input for the remote control signal receiver.

Note:
1. Contact the manufacturer of crystal/ceramic resonator regarding oscillation characteristics.

3. Address Space

3.1 Address Space

The M16C/63 Group has a 1 MB address space from 00000h to FFFFFh. Address space is expandable to 4 MB with the memory area expansion function. Addresses 40000h to BFFFFh can be used as external areas from bank 0 to bank 7. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following condition:
   - The PM13 bit in the PM1 register is 0
     (addresses 04000h to 0CFFFh and 80000h to CFFFFh are used as external areas)

Figure 3.1 Address Space

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART7 Special Mode Register 4	U7SMR4	00h
02A5h	UART7 Special Mode Register 3	U7SMR3	000X 0X0Xb
02A6h	UART7 Special Mode Register 2	U7SMR2	X000 0000b
02A7h	UART7 Special Mode Register	U7SMR	X000 0000b
02A8h	UART7 Transmit/Receive Mode Register	U7MR	00h
02A9h	UART7 Bit Rate Register	U7BRG	XXh
02AAh	UART7 Transmit Buffer Register	U7TB	XXh
02ABh			XXh
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	0000 1000b
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	0000 0010b
02AEh	UART7 Receive Buffer Register	U7RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h to 02FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	Reset Value
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 0000b
03D8h	D/A0 Register	DA0	00h
03D9h			
03DAh	D/A1 Register	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

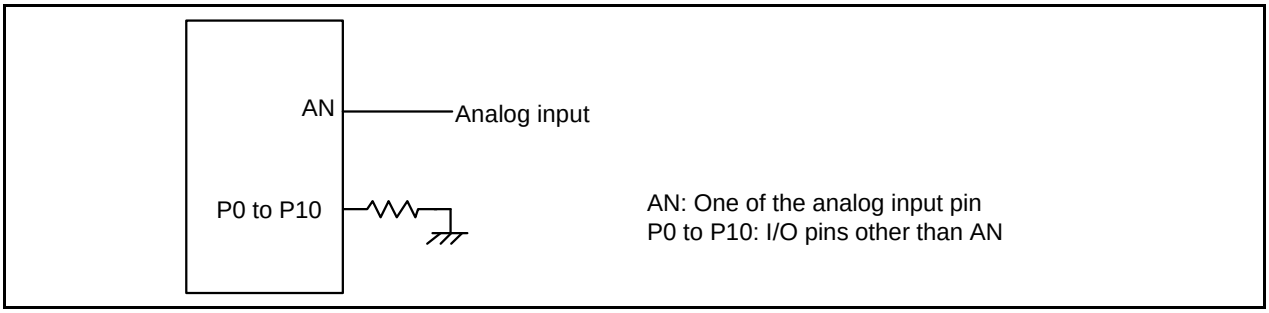


Figure 5.3 A/D Accuracy Measure Circuit

Table 5.7 A/D Conversion Characteristics (2/2) (1)

$AV_{CC} = V_{CC1} = V_{CC2} = V_{REF} = 1.8$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
ϕAD	A/D operating clock frequency	4.0 V ≤ V_{REF} ≤ AV_{CC} ≤ 5.5 V	2		20	MHz
		3.2 V ≤ V_{REF} ≤ AV_{CC} ≤ 5.5 V	2		16	MHz
		3.0 V ≤ V_{REF} ≤ AV_{CC} ≤ 5.5 V	2		10	MHz
		1.8 V ≤ V_{REF} ≤ AV_{CC} ≤ 5.5 V	2		5	MHz
-	Tolerance level impedance			3		kΩ
D_{NL}	Differential non-linearity error	(4)			±1	LSB
-	Offset error	(4)			±3	LSB
-	Gain error	(4)			±3	LSB
t_{CONV}	10-bit conversion time	V_{CC1} = 5 V, ϕAD = 20 MHz	2.15			µs
t_{SAMP}	Sampling time		0.75			µs
V_{REF}	Reference voltage		1.8		AV_{CC}	V
V_{IA}	Analog input voltage (2), (3)		0		V_{REF}	V

Notes:
1. Use when $AV_{CC} = V_{CC1} = V_{CC2}$.
2. Do not use A/D converter when $V_{CC1} > V_{CC2}$.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
4. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.3 “A/D Accuracy Measure Circuit”.

5.1.4 D/A Conversion Characteristics

Table 5.8 D/A Conversion Characteristics

$V_{CC1} = AV_{CC} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				2.5	LSB
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		5	6	8.2	kΩ
I_{VREF}	Reference Power Supply Input Current	See Notes 1 and 2			1.5	mA

Notes:
1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the I_{VREF} of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

5.2 Electrical Characteristics (V_{CC1} = V_{CC2} = 5 V)

5.2.1 Electrical Characteristics

V_{CC1} = V_{CC2} = 5 V

Table 5.19 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 4.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = –20°C to 85°C/–40°C to 85°C, $f_{(BCLK)}$ = 20 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –5 mA	V_{CC1} – 2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –5 mA	V_{CC2} – 2.0		V_{CC2}	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –200 µA	V_{CC1} – 0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –200 µA	V_{CC2} – 0.3		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGHPOWER	I_{OH} = –1 mA	V_{CC1} – 2.0		V_{CC1}	V
			LOWPOWER	I_{OH} = –0.5 mA	V_{CC1} – 2.0		V_{CC1}	
	High output voltage XCOUT			With no load applied		1.5		V
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 5 mA			2.0	
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 200 µA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 200 µA			0.45	
V_{OL}	Low output voltage XOUT		HIGHPOWER	I_{OL} = 1 mA			2.0	V
			LOWPOWER	I_{OL} = 0.5 mA			2.0	
	Low output voltage XCOUT			With no load applied		0		V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V, 3 V, or 1.8 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.20 Electrical Characteristics (2) (1)

$V_{CC1} = V_{CC2} = 4.2$ to $5.5\ V$, $V_{SS} = 0\ V$ at $T_{opr} = -20°C$ to $85°C/-40°C$ to $85°C$, $f_{(BCLK)} = 20$ MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT7, NMI, ADTRG, CTS0 to CTS2, CTS5 to CTS7, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, KI0 to KI7, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, SD, PMC0, PMC1, SCLMM, SDAMM, CEC, ZP, IDU, IDV, IDW		0.5		2.0	V
$V_{T+} - V_{T-}$	Hysteresis	RESET		0.5		2.5	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, BYTE	$V_I = 5\ V$			5.0	µA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, BYTE	$V_I = 0\ V$			–5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$V_I = 0\ V$	30	50	170	kΩ
R_{fXIN}	Feedback resistance XIN				0.8		MΩ
R_{fXCIN}	Feedback resistance XCIN				8		MΩ
V_{RAM}	RAM retention voltage		In stop mode	1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V, 3 V, or 1.8 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.21 Electrical Characteristics (3)

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/−40°C to 85°C, $f_{(BCLK)} = 20$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 20 MHz (no division) XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped CM15 = 1 (drive capacity High) A/D converter stopped		10.7		mA
			$f_{(BCLK)}$ =20 MHz (no division) XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped CM15 = 1 (drive capacity High) A/D converter operating (2)		11.4		mA
			$f_{(BCLK)}$ = 20 MHz XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped CM15 = 0 (drive capacity Low) A/D converter stopped		10.1		mA
			$f_{(BCLK)}$ = 20 MHz (no division) XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped CM15 = 1 (drive capacity High) PCLKSTP1 = FF (peripheral clock stop)		9.1		mA
			$f_{(BCLK)}$ = 20 MHz (no division) XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped CM15 = 0 (drive capacity Low) PCLKSTP1 = FF (peripheral clock stopped)		8.5		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-2 ($f_{(BCLK)}$ = 20 MHz) 125 kHz on-chip oscillator stopped		9.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped, 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		450.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 kHz FMR22 = FMR23 = 1 (in low current consumption read mode) On flash memory (1)		80.0		µA
		Wait mode	$f_{(BCLK)}$ = 32 kHz Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on PM25 = 1 (peripheral function clock fC operating) T_{opr} = 25°C Real-time clock operating		5.6		µA
			$f_{(BCLK)}$ = 32 kHz Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped PM25 = 0 (peripheral function clock fC stopped) T_{opr} = 25°C		5.3		µA
		Stop mode	T_{opr} = 25°C		2.4		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		30.0		mA

Notes:
1. This indicates the memory in which the program to be executed exists.
2. A/D conversion is executed in repeat mode.

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.7 Multi-master I²C-bus

Table 5.34 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

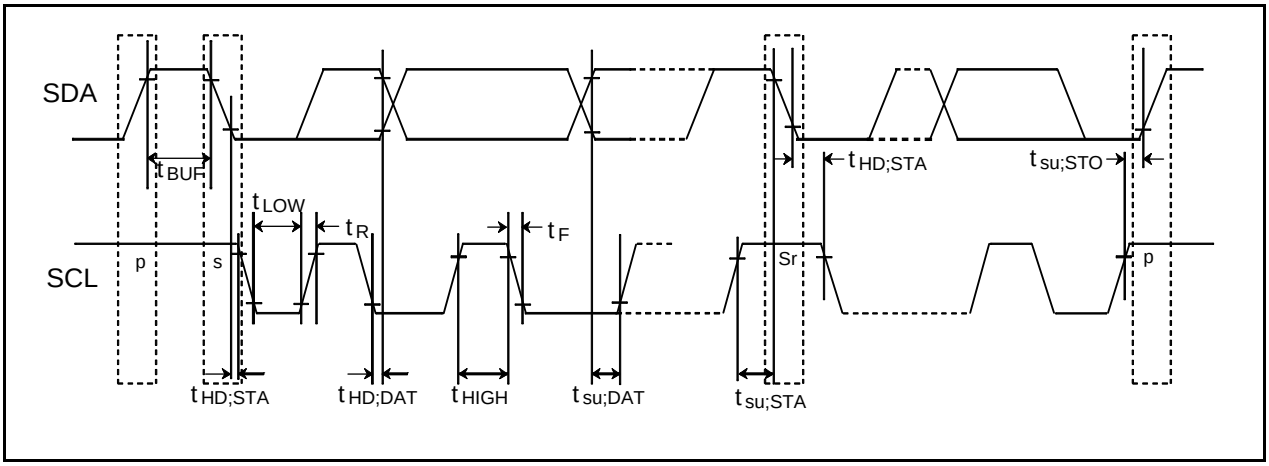


Figure 5.13 Multi-master I²C-bus

$V_{CC1} = V_{CC2} = 5\ V$

5.2.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.1 In No Wait State Setting

Table 5.36 Memory Expansion Mode and Microprocessor Mode (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.15		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

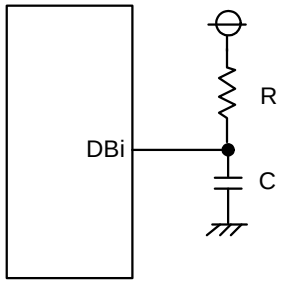
1. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$ $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
   $t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
   = 6.7 ns.



$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.5 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Inserting 1 to 3 Recovery Cycles and Accessing External Area

Table 5.40 Memory Expansion and Microprocessor Modes (in Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Inserting 1 to 3 Recovery Cycles and Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.15		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 4)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 40[ns]$$

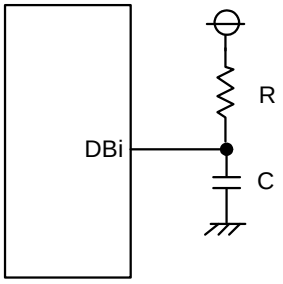
n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{m \times 10^9}{f_{(BCLK)}} - 10[ns]$$

m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



4. Calculated according to the BCLK frequency as follows:

$$\frac{m \times 10^9}{f_{(BCLK)}} + 0[ns]$$

m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.5 Serial Interface

Table 5.53 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

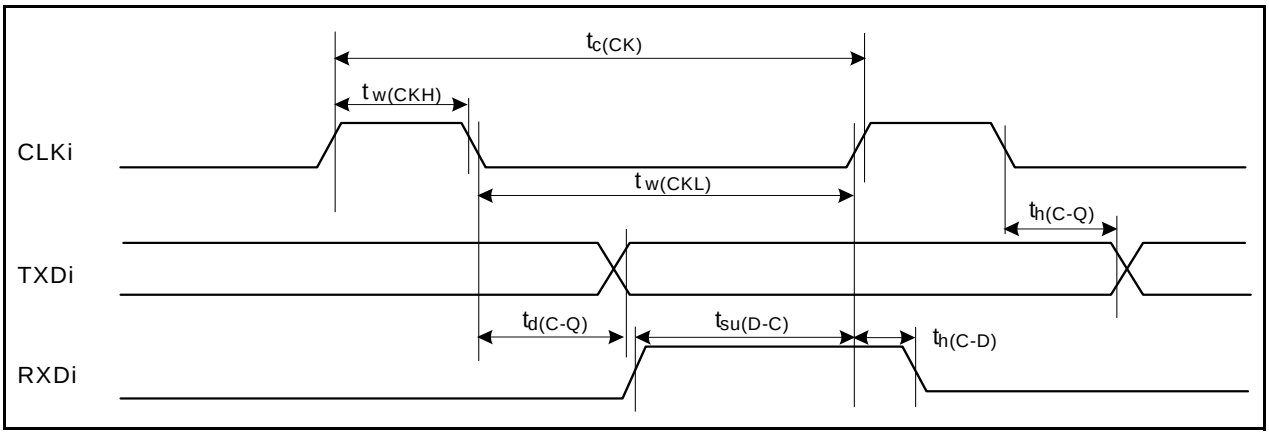


Figure 5.26 Serial Interface

5.3.2.6 External Interrupt $\overline{INTi}$ Input

Table 5.54 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	380		ns

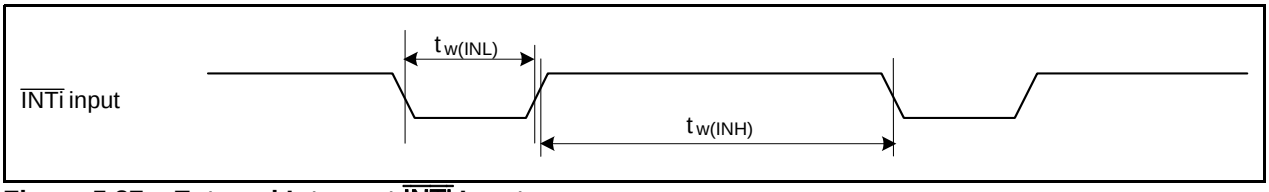


Figure 5.27 External Interrupt $\overline{INTi}$ Input

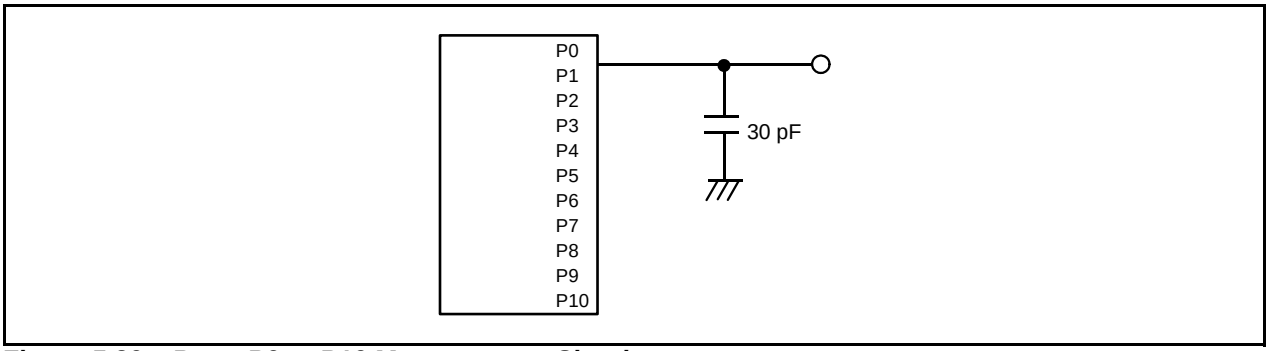


Figure 5.30 Ports P0 to P10 Measurement Circuit

$V_{CC1} = V_{CC2} = 1.8\ V$

Table 5.63 Electrical Characteristics (2) (1)

$1.8\ V \leq V_{CC1} = V_{CC2} < 2.7\ V$, $V_{SS} = 0\ V$ at $T_{opr} = -20$ to 85°C/−40 to 85°C, $f_{(BCLK)} = 5$ MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	$V_I = 0\ V$			−2.0	μA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	$V_I = 0\ V$	70	140	700	kΩ
R_{fXIN}	Feedback resistance XIN				0.8		MΩ
R_{fXCIN}	Feedback resistance XCIN				8		MΩ
V_{RAM}	RAM retention voltage			1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V, 3 V, or 1.8 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 1.8\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 1.8$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

Table 5.71 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	3		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	800		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	800		ns

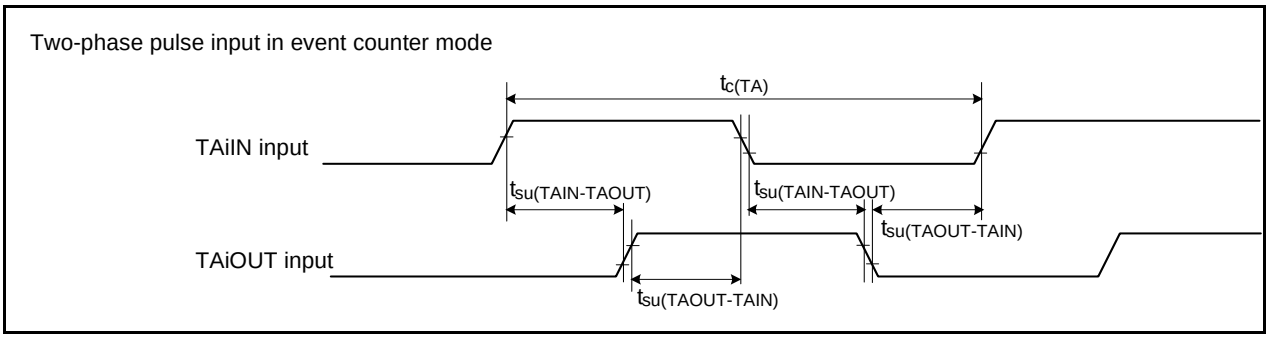


Figure 5.39 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

$V_{CC1} = V_{CC2} = 1.8\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 1.8$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.4.2.5 Serial Interface

Table 5.75 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800		ns
$t_{w(CKH)}$	CLKi input high pulse width	400		ns
$t_{w(CKL)}$	CLKi input low pulse width	400		ns
$t_{d(C-Q)}$	TXDi output delay time		240	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	200		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

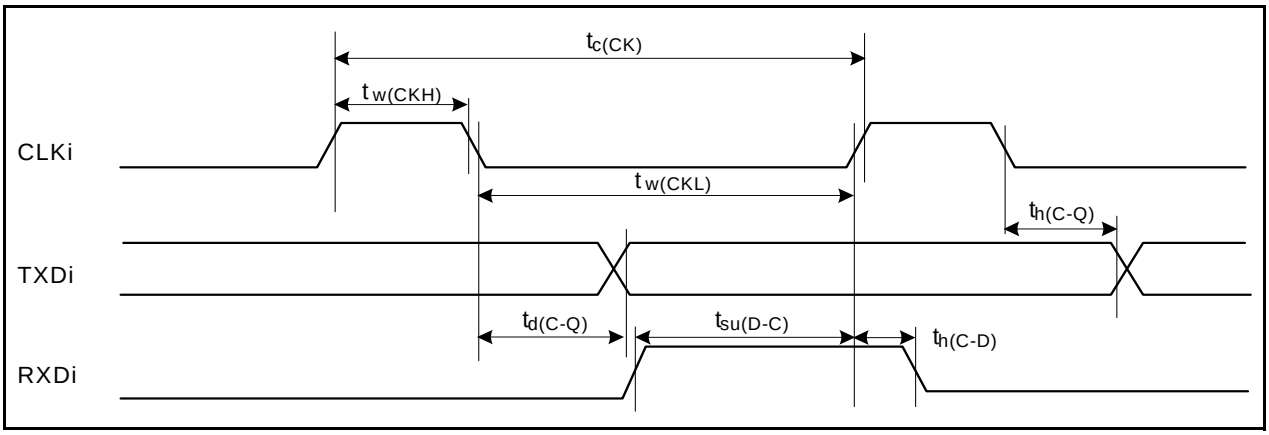


Figure 5.41 Serial Interface

5.4.2.6 External Interrupt $\overline{INTi}$ Input

Table 5.76 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	1000		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	1000		ns
tr(INT)	$\overline{INTi}$ input rising time		100	µs
tf(INT)	$\overline{INTi}$ input falling time		100	µs

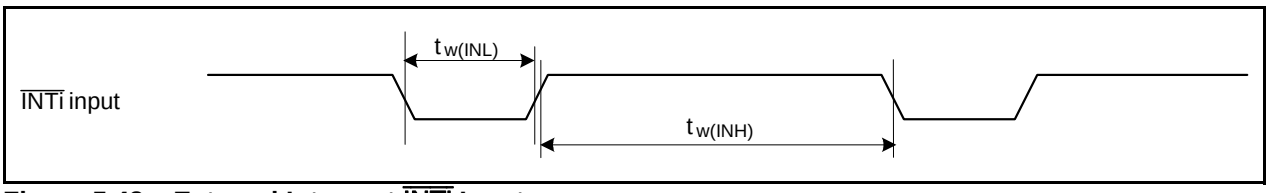


Figure 5.42 External Interrupt $\overline{INTi}$ Input

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