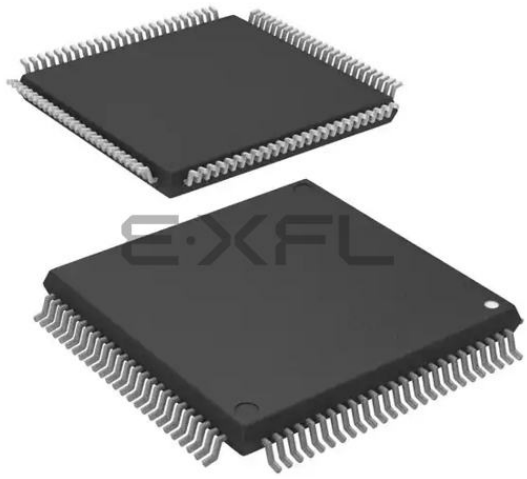
# Renesas Electronics America Inc - R5F363AMDFB#30 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | EBI/EMI, I²C, SIO, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 31K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f363amdfb-30 |

**Table 1.2 Specifications for the 100-Pin Package (2/2)**

| Item | Function | Description |
|---|---|---|
| Timers | Timer A | 16-bit timer × 5<br>Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode<br>Event counter two-phase pulse signal processing (two-phase encoder input) × 3<br>Programmable output mode × 3 |
| | Timer B | 16-bit timer × 6<br>Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode |
| | Three-phase motor control timer functions | • Three-phase inverter control (timer A1, timer A2, timer A4, timer B2)<br>• On-chip dead time timer |
| | Real-time clock | • Count: seconds, minutes, hours, days of the week, months, years<br>• Periodic interrupt: 0.25 s, 0.5 s<br>• Automatic correction function |
| | PWM function | 8 bits × 2 |
| | Remote control signal receiver | • 2 circuits<br>• 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data)<br>• 6-byte receive buffer (1 circuit only)<br>• Operating frequency of 32 kHz |
| Serial Interface | UART0 to UART2, UART5 to UART7 | Clock synchronous/asynchronous × 6 channels<br>$I^2C$-bus, IEBus, special mode 2<br>SIM (UART2) |
| | SI/O3, SI/O4 | Clock synchronization only × 2 channels |
| Multi-master $I^2C$-bus Interface | | 1 channel |
| CEC Functions (2) | | CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz |
| A/D Converter | | 10-bit resolution × 26 channels, including sample and hold function<br>Conversion time: 2.15 µs |
| D/A Converter | | 8-bit resolution × 2 circuits |
| CRC Calculator | | CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$),<br>CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant |
| Flash Memory | | • Program and erase power supply voltage: 2.7 to 5.5 V<br>• Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash)<br>• Program security: ROM code protect, ID code check |
| Debug Functions | | On-chip debug, on-board flash rewrite, address match interrupt × 4 |
| Operation Frequency/Supply Voltage | | 5 MHz/VCC1 = 1.8 to 5.5 V, VCC2 = 1.8 V to VCC1<br>10 MHz/VCC1 = 2.1 to 5.5 V, VCC2 = 2.1 V to VCC1<br>20 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1 |
| Current Consumption | | Described in Electrical Characteristics |
| Operating Temperature | | -20°C to 85°C, -40°C to 85°C (1) |
| Package | | 100-pin QFP: PRQP0100JD-B (Previous package code: 100P6F-A)<br>100-pin LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A)<br>100-pin LGA: PTLG0100KA-A (Previous package code: 100F0M) |

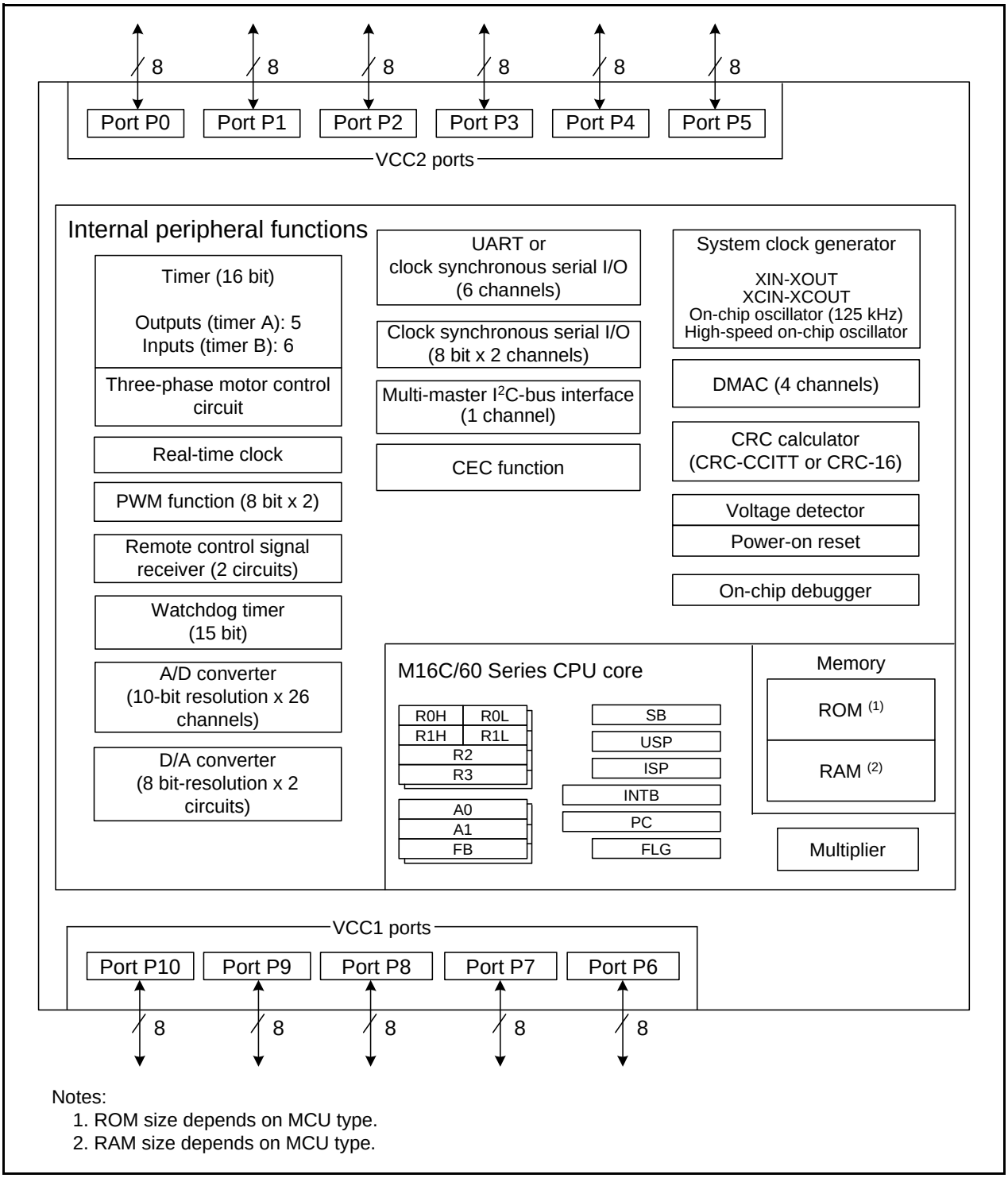
Notes:
1. See Table 1.5 “Product List” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

**Table 1.3 Specifications for the 80-Pin Package (1/2)**

| Item | Function | Description |
|---|---|---|
| CPU | Central processing unit | M16C/60 Series core<br>(multiplier: 16 bit × 16 bit → 32 bit,<br>multiply and accumulate instruction: 16 bit × 16 bit + 32 bit → 32 bit)<br>• Number of basic instructions: 91<br>• Minimum instruction execution time:<br>50.0 ns (f(BCLK) = 20 MHz, VCC1 = 2.7 to 5.5 V)<br>100.0 ns (f(BCLK) = 10 MHz, VCC1 = 2.1 to below 2.7 V)<br>200.0 ns (f(BCLK) = 5 MHz, VCC1 = 1.8 V)<br>• Operating mode: Single-chip |
| Memory | ROM, RAM, data flash | See Table 1.5 “Product List”. |
| Voltage Detection | Voltage detector | • Power-on reset<br>• 3 voltage detection points (detection level of voltage detection 0 and 1 selectable) |
| Clock | Clock generator | • 4 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ±10%)<br>• Oscillation stop detection: Main clock oscillation stop/restart detection function<br>• Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16<br>Sub clock frequency divider circuit: Divide ratio selectable from 1 and 2<br>• Power saving features: Wait mode, stop mode<br>• Real-time clock |
| External Bus Expansion | Bus memory expansion | None |
| I/O Ports | Programmable I/O ports | • CMOS I/O ports: 68 (selectable pull-up resistors)<br>• N-channel open drain ports: 3 |
| Interrupts | | • Interrupt vectors: 70<br>• External interrupt inputs: 14 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 5, key input × 8)<br>• Interrupt priority levels: 7 |
| Watchdog Timer | | 15-bit timer × 1 (with prescaler)<br>Automatic reset start function selectable |
| DMA | DMAC | • 4 channels, cycle steal mode<br>• Trigger sources: 43<br>• Transfer modes: 2 (single transfer, repeat transfer) |

## 1.4 Block Diagram

Figure 1.4 and Figure 1.5 show block diagrams.




Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

**Figure 1.4 Block Diagram for the 100-Pin Package**

**Table 4.11 SFR Information (11)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 02A0h | | | |
| 02A1h | | | |
| 02A2h | | | |
| 02A3h | | | |
| 02A4h | UART7 Special Mode Register 4 | U7SMR4 | 00h |
| 02A5h | UART7 Special Mode Register 3 | U7SMR3 | 000X 0X0Xb |
| 02A6h | UART7 Special Mode Register 2 | U7SMR2 | X000 0000b |
| 02A7h | UART7 Special Mode Register | U7SMR | X000 0000b |
| 02A8h | UART7 Transmit/Receive Mode Register | U7MR | 00h |
| 02A9h | UART7 Bit Rate Register | U7BRG | XXh |
| 02AAh | UART7 Transmit Buffer Register | U7TB | XXh |
| 02ABh | | | XXh |
| 02ACh | UART7 Transmit/Receive Control Register 0 | U7C0 | 0000 1000b |
| 02ADh | UART7 Transmit/Receive Control Register 1 | U7C1 | 0000 0010b |
| 02AEh | UART7 Receive Buffer Register | U7RB | XXh |
| 02AFh | | | XXh |
| 02B0h | I2C0 Data Shift Register | S00 | XXh |
| 02B1h | | | |
| 02B2h | I2C0 Address Register 0 | S0D0 | 0000 000Xb |
| 02B3h | I2C0 Control Register 0 | S1D0 | 00h |
| 02B4h | I2C0 Clock Control Register | S20 | 00h |
| 02B5h | I2C0 Start/Stop Condition Control Register | S2D0 | 0001 1010b |
| 02B6h | I2C0 Control Register 1 | S3D0 | 0011 0000b |
| 02B7h | I2C0 Control Register 2 | S4D0 | 00h |
| 02B8h | I2C0 Status Register 0 | S10 | 0001 000Xb |
| 02B9h | I2C0 Status Register 1 | S11 | XXXX X000b |
| 02BAh | I2C0 Address Register 1 | S0D1 | 0000 000Xb |
| 02BBh | I2C0 Address Register 2 | S0D2 | 0000 000Xb |
| 02BCh | | | |
| 02BDh | | | |
| 02BEh | | | |
| 02BFh | | | |
| 02C0h to 02FFh | | | |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.12 SFR Information (12)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0300h | Timer B3/B4/B5 Count Start Flag | TBSR | 000X XXXXb |
| 0301h | | | |
| 0302h | Timer A1-1 Register | TA11 | XXh |
| 0303h | | | XXh |
| 0304h | Timer A2-1 Register | TA21 | XXh |
| 0305h | | | XXh |
| 0306h | Timer A4-1 Register | TA41 | XXh |
| 0307h | | | XXh |
| 0308h | Three-Phase PWM Control Register 0 | INVC0 | 00h |
| 0309h | Three-Phase PWM Control Register 1 | INVC1 | 00h |
| 030Ah | Three-Phase Output Buffer Register 0 | IDB0 | XX11 1111b |
| 030Bh | Three-Phase Output Buffer Register 1 | IDB1 | XX11 1111b |
| 030Ch | Dead Time Timer | DTT | XXh |
| 030Dh | Timer B2 Interrupt Generation Frequency Set Counter | ICTB2 | XXh |
| 030Eh | Position-Data-Retain Function Control Register | PDRF | XXXX 0000b |
| 030Fh | | | |
| 0310h | Timer B3 Register | TB3 | XXh |
| 0311h | | | XXh |
| 0312h | Timer B4 Register | TB4 | XXh |
| 0313h | | | XXh |
| 0314h | Timer B5 Register | TB5 | XXh |
| 0315h | | | XXh |
| 0316h | | | |
| 0317h | | | |
| 0318h | Port Function Control Register | PFCR | 0011 1111b |
| 0319h | | | |
| 031Ah | | | |
| 031Bh | Timer B3 Mode Register | TB3MR | 00XX 0000b |
| 031Ch | Timer B4 Mode Register | TB4MR | 00XX 0000b |
| 031Dh | Timer B5 Mode Register | TB5MR | 00XX 0000b |
| 031Eh | | | |
| 031Fh | | | |
| 0320h | Count Start Flag | TABSR | 00h |
| 0321h | | | |
| 0322h | One-Shot Start Flag | ONSF | 00h |
| 0323h | Trigger Select Register | TRGSR | 00h |
| 0324h | Increment/Decrement Flag | UDF | 00h |
| 0325h | | | |
| 0326h | Timer A0 Register | TA0 | XXh |
| 0327h | | | XXh |
| 0328h | Timer A1 Register | TA1 | XXh |
| 0329h | | | XXh |
| 032Ah | Timer A2 Register | TA2 | XXh |
| 032Bh | | | XXh |
| 032Ch | Timer A3 Register | TA3 | XXh |
| 032Dh | | | XXh |
| 032Eh | Timer A4 Register | TA4 | XXh |
| 032Fh | | | XXh |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.14 SFR Information (14)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0360h | Pull-Up Control Register 0 | PUR0 | 00h |
| 0361h | Pull-Up Control Register 1 | PUR1 | 0000 0000b (2)<br>0000 0010b |
| 0362h | Pull-Up Control Register 2 | PUR2 | 00h |
| 0363h | | | |
| 0364h | | | |
| 0365h | | | |
| 0366h | Port Control Register | PCR | 0000 0XX0b |
| 0367h | | | |
| 0368h | | | |
| 0369h | NMI/SD Digital Filter Register | NMIDF | XXXX X000b |
| 036Ah | | | |
| 036Bh | | | |
| 036Ch | | | |
| 036Dh | | | |
| 036Eh | | | |
| 036Fh | | | |
| 0370h | PWM Control Register 0 | PWMCON0 | 00h |
| 0371h | | | |
| 0372h | PWM0 Prescaler | PWMPRE0 | 00h |
| 0373h | PWM0 Register | PWMREG0 | 00h |
| 0374h | PWM1 Prescaler | PWMPRE1 | 00h |
| 0375h | PWM1 Register | PWMREG1 | 00h |
| 0376h | PWM Control Register 1 | PWMCON1 | 00h |
| 0377h | | | |
| 0378h | | | |
| 0379h | | | |
| 037Ah | | | |
| 037Bh | | | |
| 037Ch | Count Source Protection Mode Register | CSPR | 00h (3) |
| 037Dh | Watchdog Timer Refresh Register | WDTR | XXh |
| 037Eh | Watchdog Timer Start Register | WDTS | XXh |
| 037Fh | Watchdog Timer Control Register | WDC | 00XX XXXXb |
| 0380h to 038Fh | | | |

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
 - 00000000b when a low-level signal is input to the CNVSS pin
 - 00000010b when a high-level signal is input to the CNVSS pin
 Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detect reset are as follows:
 - 00000000b when bits PM01 and PM00 in the PM0 register are 00b (single-chip mode).
 - 00000010b when bits PM01 and PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).
3. When the CSPROINI bit in the OFS1 address is 0, the reset value is 1000 0000b.

## 5.1.2 Recommended Operating Conditions

**Table 5.2 Recommended Operating Conditions (1/4)**

$V_{CC1}$ = $V_{CC2}$ = 1.8 to 5.5 V at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

| Symbol | Parameter | | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CC1}$ | Supply voltage | CEC function is not used ($V_{CC1} \geq V_{CC2}$) | | 2.7 | | 5.5 | V |
| | | CEC function is not used ($V_{CC1} = V_{CC2}$) | | 1.8 | | 5.5 | V |
| | | CEC function is used | | 2.7 | | 3.63 | V |
| $V_{CC2}$ | Supply voltage | | $V_{CC1} \geq 2.7$ | 2.7 | | $V_{CC1}$ | V |
| | | | $V_{CC1} < 2.7$ | | $V_{CC1}$ | | V |
| $AV_{CC}$ | Analog supply voltage | | | | $V_{CC1}$ | | V |
| $V_{SS}$ | Supply voltage | | | | 0 | | V |
| $AV_{SS}$ | Analog supply voltage | | | | 0 | | V |
| $V_{IH}$ | High input voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7 | 2.7 V ≤ $V_{CC1}$ ≤ 5.5 V | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | | 1.8 V ≤ $V_{CC1}$ < 2.7 V | 0.85$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode) | 2.7 V ≤ $V_{CC1}$ ≤ 5.5 V | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | | 1.8 V ≤ $V_{CC1}$ < 2.7 V | 0.85$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor modes) | 2.7 V ≤ $V_{CC1}$ ≤ 5.5 V | 0.5$V_{CC2}$ | | $V_{CC2}$ | V |
| | | | 1.8 V ≤ $V_{CC1}$ < 2.7 V | 0.55$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE | 2.7 V ≤ $V_{CC1}$ ≤ 5.5 V | 0.8$V_{CC1}$ | | $V_{CC1}$ | V |
| | | | 1.8 V ≤ $V_{CC1}$ < 2.7 V | 0.85$V_{CC1}$ | | $V_{CC1}$ | V |
| | | P7_0, P7_1, P8_5 | 2.7 V ≤ $V_{CC1}$ ≤ 5.5 V | 0.8$V_{CC1}$ | | 6.5 | V |
| | | | 1.8 V ≤ $V_{CC1}$ < 2.7 V | 0.85$V_{CC1}$ | | 6.5 | V |
| | | CEC | | 0.7$V_{CC1}$ | | | V |
| $V_{IL}$ | Low input voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7 | | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode) | | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor mode) | | 0 | | 0.16$V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{\text{RESET}}$, CNVSS, BYTE | | 0 | | 0.2$V_{CC1}$ | V |
| | | CEC | | | | 0.26$V_{CC1}$ | V |

**Table 5.3 Recommended Operating Conditions (2/4)**

$V_{CC1}$ = $V_{CC2}$ = 1.8 to 5.5 V at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

| Symbol | Parameter | | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{OH(sum)}$ | High peak output current (100-pin package) | $V_{CC1}$, $V_{CC2}$ ≥ 2.7 V | Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7 | | | -40.0 | mA |
| | | | Sum of $I_{OH(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 | | | -40.0 | mA |
| | | | Sum of $I_{OH(peak)}$ at P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4 | | | -40.0 | mA |
| | | | Sum of $I_{OH(peak)}$ at P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | -40.0 | mA |
| | | $V_{CC1}$, $V_{CC2}$ < 2.7 V | Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7 | | | -5.0 | mA |
| | | | Sum of $I_{OH(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 | | | -5.0 | mA |
| | | | Sum of $I_{OH(peak)}$ at P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4 | | | -5.0 | mA |
| | | | Sum of $I_{OH(peak)}$ at P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | -5.0 | mA |
| | High peak output current (80-pin package) | $V_{CC1}$, $V_{CC2}$ ≥ 2.7 V | Sum of all ports | | | -80.0 | mA |
| | | $V_{CC1}$, $V_{CC2}$ < 2.7 V | Sum of all ports | | | -10.0 | mA |
| $I_{OH(peak)}$ | High peak output current | $V_{CC1}$, $V_{CC2}$ ≥ 2.7 V | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | –10.0 | mA |
| | | $V_{CC1}$, $V_{CC2}$ < 2.7 V | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | –1.0 | mA |
| $I_{OH(avg)}$ | High average output current (1) | $V_{CC1}$, $V_{CC2}$ ≥ 2.7 V | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | –5.0 | mA |
| | | $V_{CC1}$, $V_{CC2}$ < 2.7 V | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | –0.5 | mA |

Note:
1. The average output current is the mean value within 100 ms.

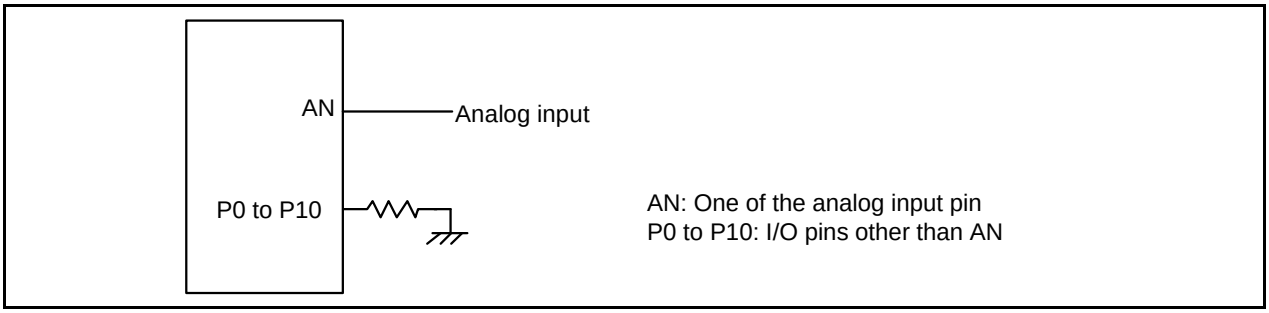



**Figure 5.3 A/D Accuracy Measure Circuit**

**Table 5.7 A/D Conversion Characteristics (2/2) (1)**

$AV_{CC} = V_{CC1} = V_{CC2} = V_{REF} = 1.8$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| ϕAD | A/D operating clock frequency | 4.0 V ≤ $V_{REF}$ ≤ $AV_{CC}$ ≤ 5.5 V | 2 | | 20 | MHz |
| | | 3.2 V ≤ $V_{REF}$ ≤ $AV_{CC}$ ≤ 5.5 V | 2 | | 16 | MHz |
| | | 3.0 V ≤ $V_{REF}$ ≤ $AV_{CC}$ ≤ 5.5 V | 2 | | 10 | MHz |
| | | 1.8 V ≤ $V_{REF}$ ≤ $AV_{CC}$ ≤ 5.5 V | 2 | | 5 | MHz |
| - | Tolerance level impedance | | | 3 | | kΩ |
| $D_{NL}$ | Differential non-linearity error | (4) | | | ±1 | LSB |
| - | Offset error | (4) | | | ±3 | LSB |
| - | Gain error | (4) | | | ±3 | LSB |
| $t_{CONV}$ | 10-bit conversion time | $V_{CC1}$ = 5 V, ϕAD = 20 MHz | 2.15 | | | µs |
| $t_{SAMP}$ | Sampling time | | 0.75 | | | µs |
| $V_{REF}$ | Reference voltage | | 1.8 | | $AV_{CC}$ | V |
| $V_{IA}$ | Analog input voltage (2), (3) | | 0 | | $V_{REF}$ | V |

Notes:
1. Use when $AV_{CC} = V_{CC1} = V_{CC2}$.
2. Do not use A/D converter when $V_{CC1} > V_{CC2}$.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
4. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to $V_{SS}$. See Figure 5.3 “A/D Accuracy Measure Circuit”.

## 5.1.4 D/A Conversion Characteristics

**Table 5.8 D/A Conversion Characteristics**

$V_{CC1} = AV_{CC} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| - | Resolution | | | | 8 | Bits |
| - | Absolute Accuracy | | | | 2.5 | LSB |
| $t_{SU}$ | Setup Time | | | | 3 | µs |
| $R_O$ | Output Resistance | | 5 | 6 | 8.2 | kΩ |
| $I_{VREF}$ | Reference Power Supply Input Current | See Notes 1 and 2 | | | 1.5 | mA |

Notes:
1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the $I_{VREF}$ of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

$V_{CC1} = V_{CC2} = 5\ V$

**Table 5.20 Electrical Characteristics (2) (1)**

$V_{CC1} = V_{CC2} = 4.2$ to $5.5\ V$, $V_{SS} = 0\ V$ at $T_{opr} = -20°C$ to $85°C/-40°C$ to $85°C$, $f_{(BCLK)} = 20$ MHz unless otherwise specified.

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{T+} - V_{T-}$ | Hysteresis | HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT7, NMI, ADTRG, CTS0 to CTS2, CTS5 to CTS7, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, KI0 to KI7, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, SD, PMC0, PMC1, SCLMM, SDAMM, CEC, ZP, IDU, IDV, IDW | | 0.5 | | 2.0 | V |
| $V_{T+} - V_{T-}$ | Hysteresis | RESET | | 0.5 | | 2.5 | V |
| $I_{IH}$ | High input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, BYTE | $V_I = 5\ V$ | | | 5.0 | µA |
| $I_{IL}$ | Low input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, BYTE | $V_I = 0\ V$ | | | –5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | $V_I = 0\ V$ | 30 | 50 | 170 | kΩ |
| $R_{fXIN}$ | Feedback resistance XIN | | | | 0.8 | | MΩ |
| $R_{fXCIN}$ | Feedback resistance XCIN | | | | 8 | | MΩ |
| $V_{RAM}$ | RAM retention voltage | | In stop mode | 1.8 | | | V |

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V, 3 V, or 1.8 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

**Table 5.28 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 800 | | ns |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT input setup time | 200 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN input setup time | 200 | | ns |

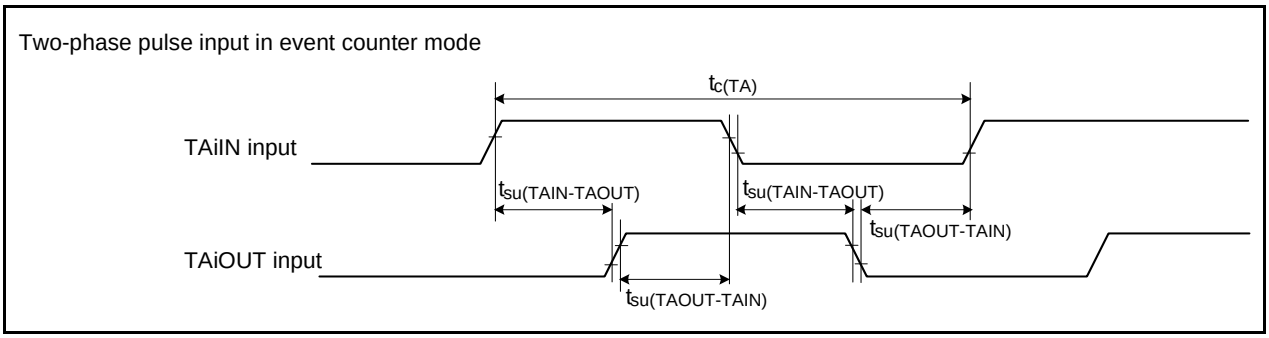



**Figure 5.9 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

$V_{CC1} = V_{CC2} = 5\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

### 5.2.2.4 Timer B Input

**Table 5.29 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | TBiIN input high pulse width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN input low pulse width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN input high pulse width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input low pulse width (counted on both edges) | 80 | | ns |

**Table 5.30 Timer B Input (Pulse Period Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input high pulse width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN input low pulse width | 200 | | ns |

**Table 5.31 Timer B Input (Pulse Width Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input high pulse width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN input low pulse width | 200 | | ns |

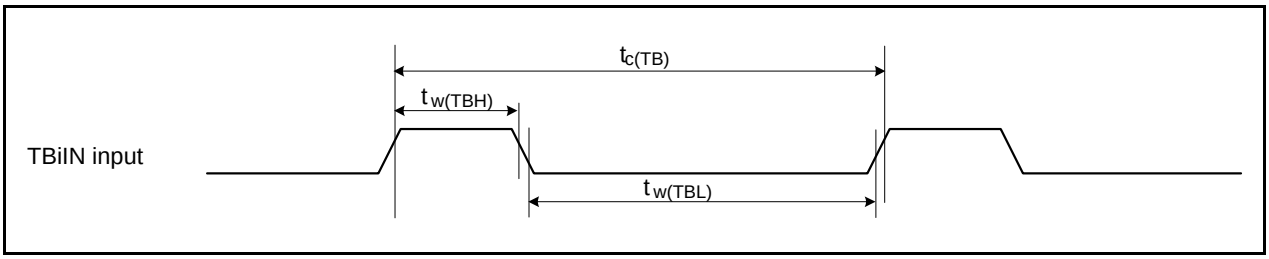



**Figure 5.10 Timer B Input**

$V_{CC1} = V_{CC2} = 5\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

### 5.2.2.7 Multi-master I²C-bus

**Table 5.34 Multi-master I²C-bus**

| Symbol | Parameter | Standard Clock Mode | | Fast-mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{BUF}$ | Bus free time | 4.7 | | 1.3 | | µs |
| $t_{HD;STA}$ | Hold time in start condition | 4.0 | | 0.6 | | µs |
| $t_{LOW}$ | Hold time in SCL clock 0 status | 4.7 | | 1.3 | | µs |
| $t_R$ | SCL, SDA signals' rising time | | 1000 | 20 + 0.1 Cb | 300 | ns |
| $t_{HD;DAT}$ | Data hold time | 0 | | 0 | 0.9 | µs |
| $t_{HIGH}$ | Hold time in SCL clock 1 status | 4.0 | | 0.6 | | µs |
| $f_F$ | SCL, SDA signals' falling time | | 300 | 20 + 0.1 Cb | 300 | ns |
| $t_{su;DAT}$ | Data setup time | 250 | | 100 | | ns |
| $t_{su;STA}$ | Setup time in restart condition | 4.7 | | 0.6 | | µs |
| $t_{su;STO}$ | Stop condition setup time | 4.0 | | 0.6 | | µs |

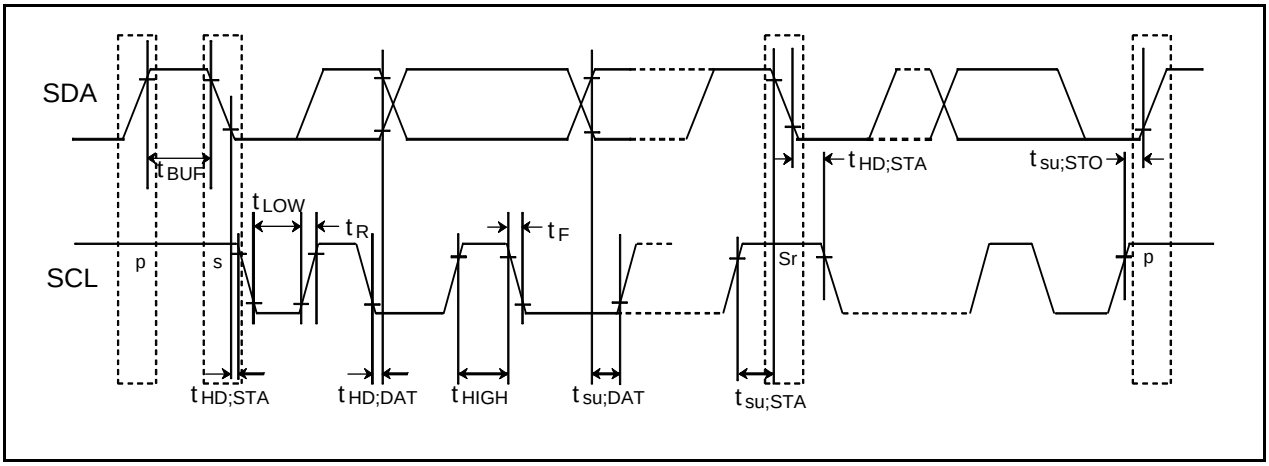
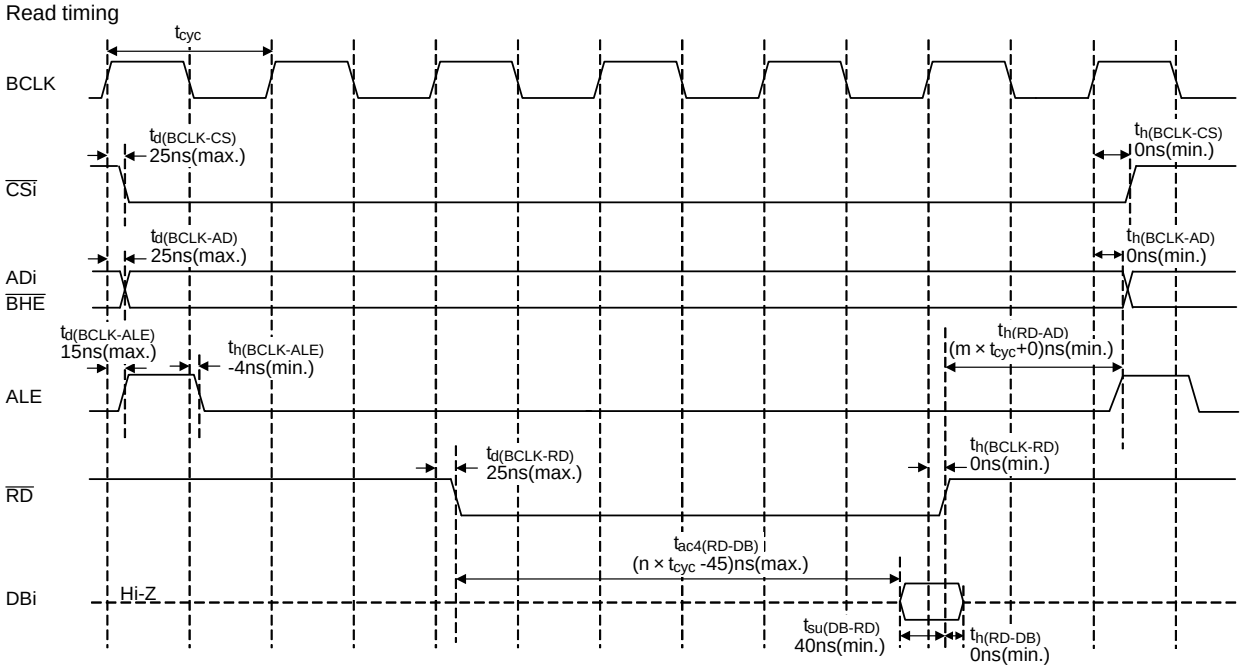



**Figure 5.13 Multi-master I²C-bus**

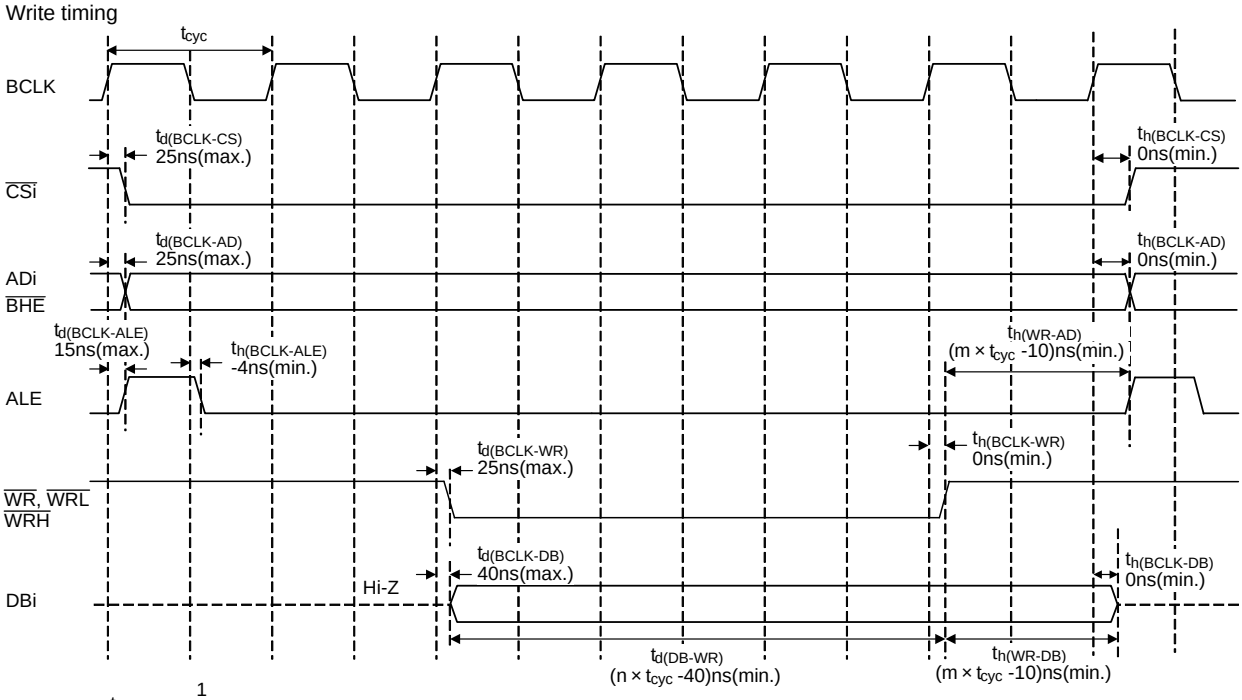
Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and
when inserting 1 to 3 recovery cycles and accessing external area)

$V_{CC1} = V_{CC2} = 5V$

Read timing




Write timing




$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V
- Output timing voltage: $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

m: 1 (when 1 recovery cycle inserted )
2 (when 2 recovery cycles inserted)
3 (when 3 recovery cycles inserted)

**Figure 5.20 Timing Diagram**

$V_{CC1} = V_{CC2} = 3\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

### 5.3.2.3 Timer A Input

**Table 5.45 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 150 | | ns |
| $t_{w(TAH)}$ | TAiIN input high pulse width | 60 | | ns |
| $t_{w(TAL)}$ | TAiIN input low pulse width | 60 | | ns |

**Table 5.46 Timer A Input (Gating Input in Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 600 | | ns |
| $t_{w(TAH)}$ | TAiIN input high pulse width | 300 | | ns |
| $t_{w(TAL)}$ | TAiIN input low pulse width | 300 | | ns |

**Table 5.47 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 300 | | ns |
| $t_{w(TAH)}$ | TAiIN input high pulse width | 150 | | ns |
| $t_{w(TAL)}$ | TAiIN input low pulse width | 150 | | ns |

**Table 5.48 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN input high pulse width | 150 | | ns |
| $t_{w(TAL)}$ | TAiIN input low pulse width | 150 | | ns |

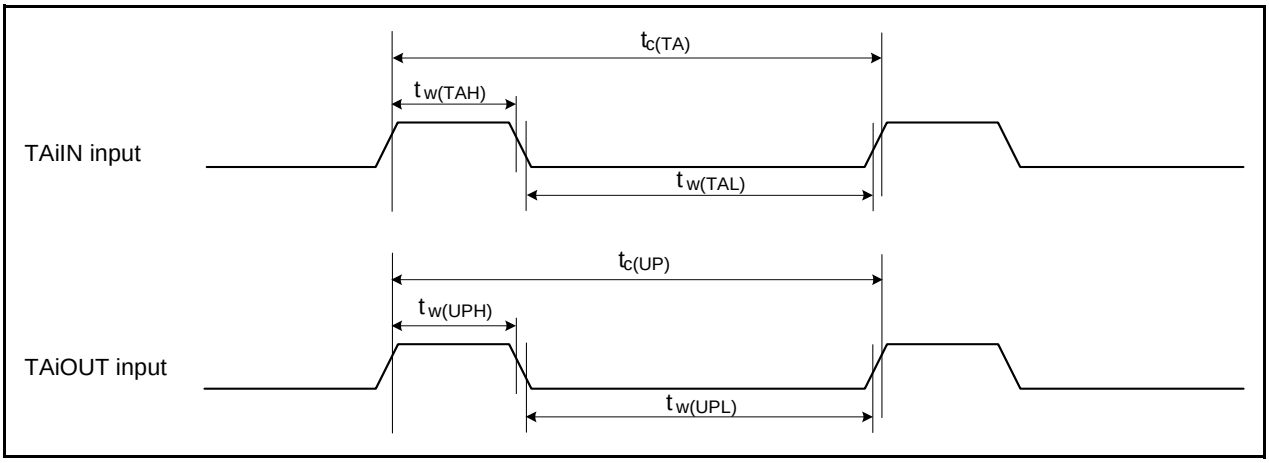



**Figure 5.23 Timer A Input**

$V_{CC1} = V_{CC2} = 3\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

**Table 5.49 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 2 | | µs |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT input setup time | 500 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN input setup time | 500 | | ns |

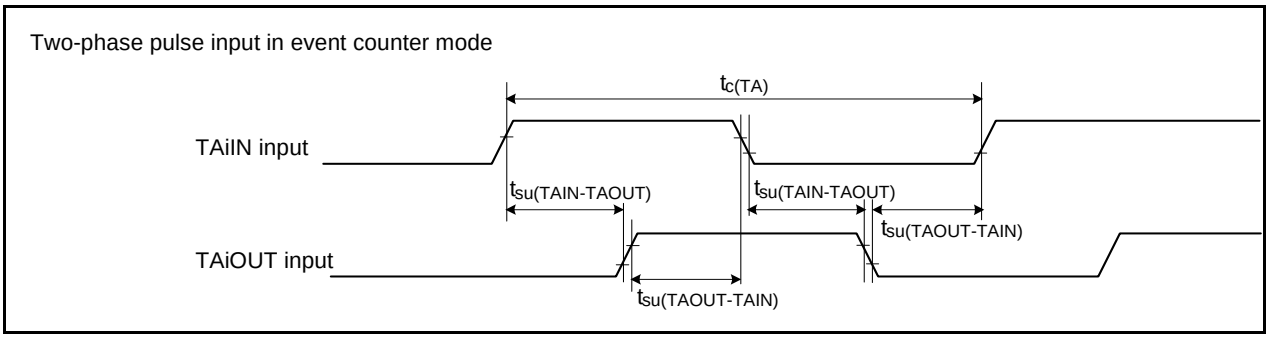
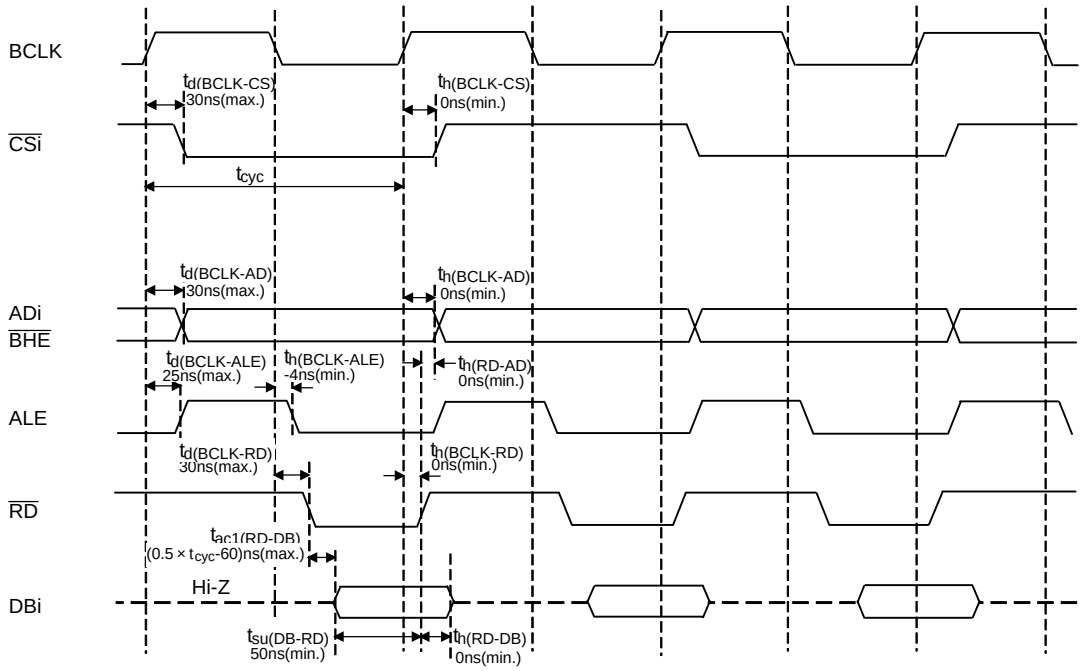



**Figure 5.24 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

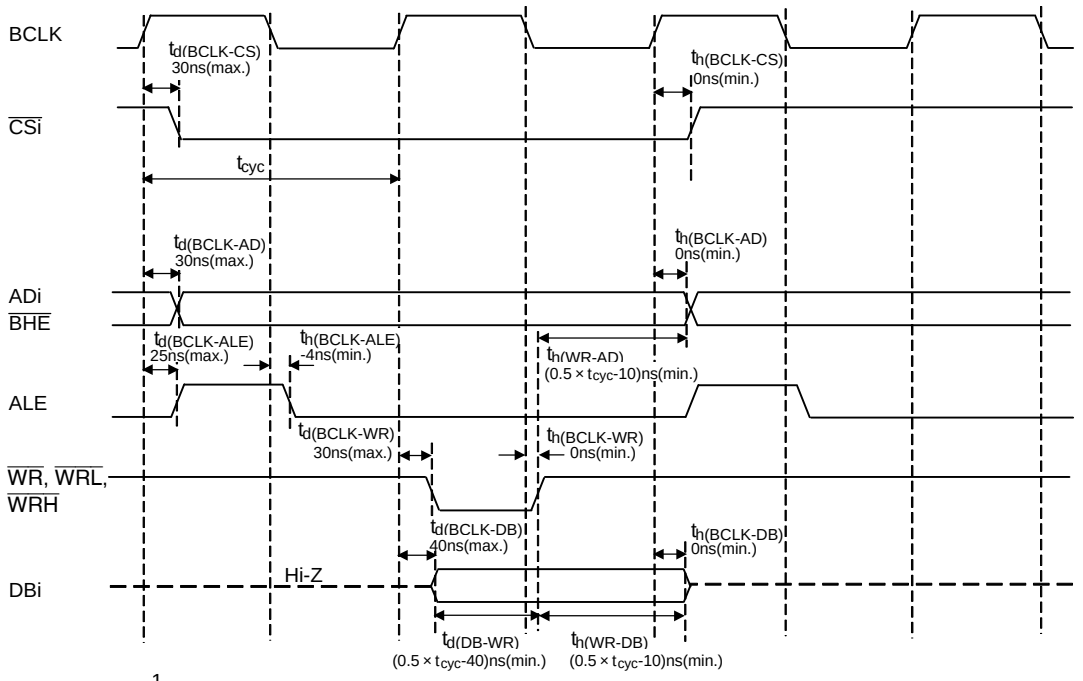
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$V_{CC1} = V_{CC2} = 3V$

Read timing




Write timing




$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

**Figure 5.31 Timing Diagram**

## 5.4 Electrical Characteristics ($V_{CC1}$ = $V_{CC2}$ = 1.8 V)

### 5.4.1 Electrical Characteristics

$V_{CC1}$ = $V_{CC2}$ = 1.8 V

**Table 5.62 Electrical Characteristics (1) (1)**

1.8 V ≤ $V_{CC1}$ = $V_{CC2}$ < 2.7 V, $V_{SS}$ = 0 V at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C, $f_{(BCLK)}$ = 5 MHz unless otherwise specified.

| Symbol | Parameter | | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | High output voltage | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | $I_{OH}$ = –1 mA | $V_{CC1}$ – 0.5 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 | | $I_{OH}$ = –1 mA | $V_{CC2}$ – 0.5 | | $V_{CC2}$ | |
| $V_{OH}$ | High output voltage XOUT | | HIGHPOWER | $I_{OH}$ = –0.1 mA | $V_{CC1}$ – 0.5 | | $V_{CC1}$ | V |
| | | | LOWPOWER | $I_{OH}$ = –50 µA | $V_{CC1}$ – 0.5 | | $V_{CC1}$ | |
| | High output voltage XCOUT | | | With no load applied | | 1.5 | | V |
| $V_{OL}$ | Low output voltage | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 | | $I_{OL}$ = 1 mA | | | 0.5 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 | | $I_{OL}$ = 1 mA | | | 0.5 | |
| $V_{OL}$ | Low output voltage XOUT | | HIGHPOWER | $I_{OL}$ = 0.1 mA | | | 0.5 | V |
| | | | LOWPOWER | $I_{OL}$ = 50 µA | | | 0.5 | |
| | Low output voltage XCOUT | | | With no load applied | | 0 | | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$ to $\overline{CTS7}$, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI7}$, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{SD}$, PMC0, PMC1, SCLMM, SDAMM, CEC | | $V_{CC1}$ = $V_{CC2}$ = 1.8 V | 0.02 | | 0.1 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{RESET}$ | | $V_{CC1}$ = $V_{CC2}$ = 1.8 V | 0.05 | | 0.15 | V |
| $I_{IH}$ | High input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS, BYTE | | $V_I$ = 1.8 V | | | 2.0 | µA |

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V, 3 V, or 1.8 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 1.8\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 1.8$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

**Table 5.71 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 3 | | µs |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT input setup time | 800 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN input setup time | 800 | | ns |

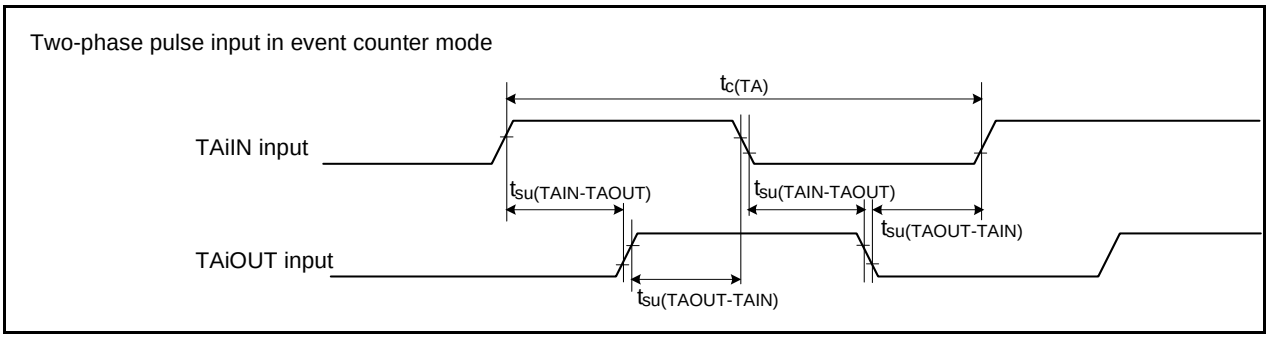
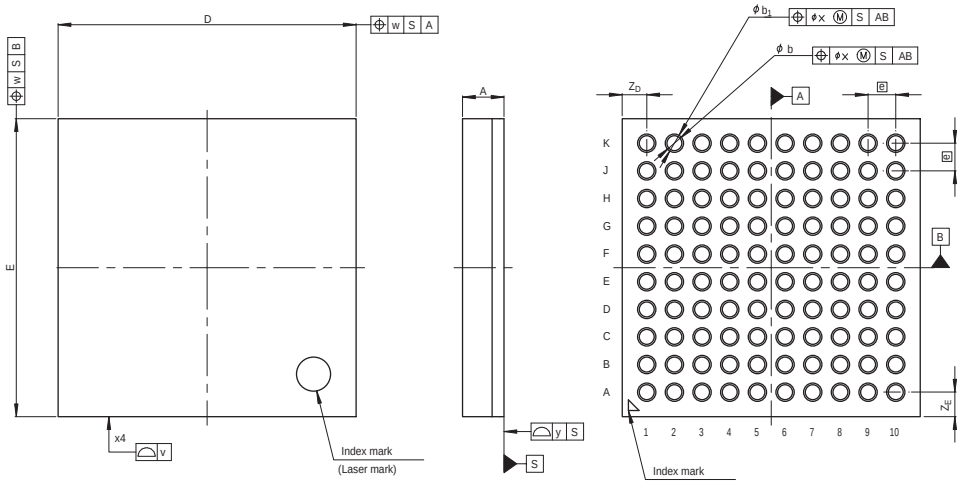


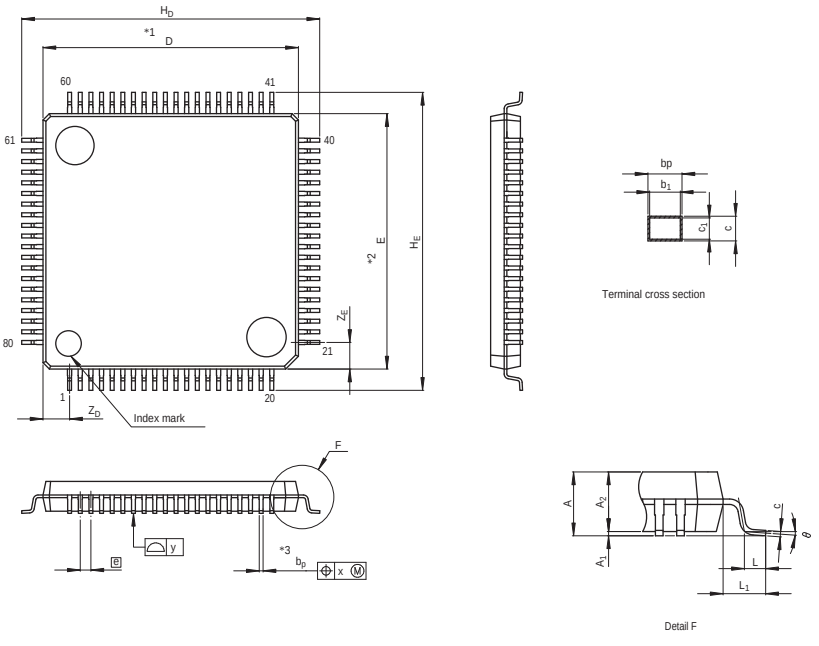

**Figure 5.39 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA100-5.5x5.5-0.5 | PTLG0100KA-A | 100F0M | 0.1g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 5.5 | — |
| E | — | 5.5 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.5 | — |
| b | 0.21 | 0.25 | 0.29 |
| $b_1$ | 0.29 | 0.34 | 0.39 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.5 | — |
| $Z_E$ | — | 0.5 | — |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP80-12x12-0.50 | PLQP0080KB-A | 80P6Q-A | 0.5g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 11.9 | 12.0 | 12.1 |
| E | 11.9 | 12.0 | 12.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 13.8 | 14.0 | 14.2 |
| $H_E$ | 13.8 | 14.0 | 14.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 10° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.3 | 0.5 | 0.7 |
| $L_1$ | — | 1.0 | — |