# Renesas Electronics America Inc - R5F363AMNFA#U0 Datasheet

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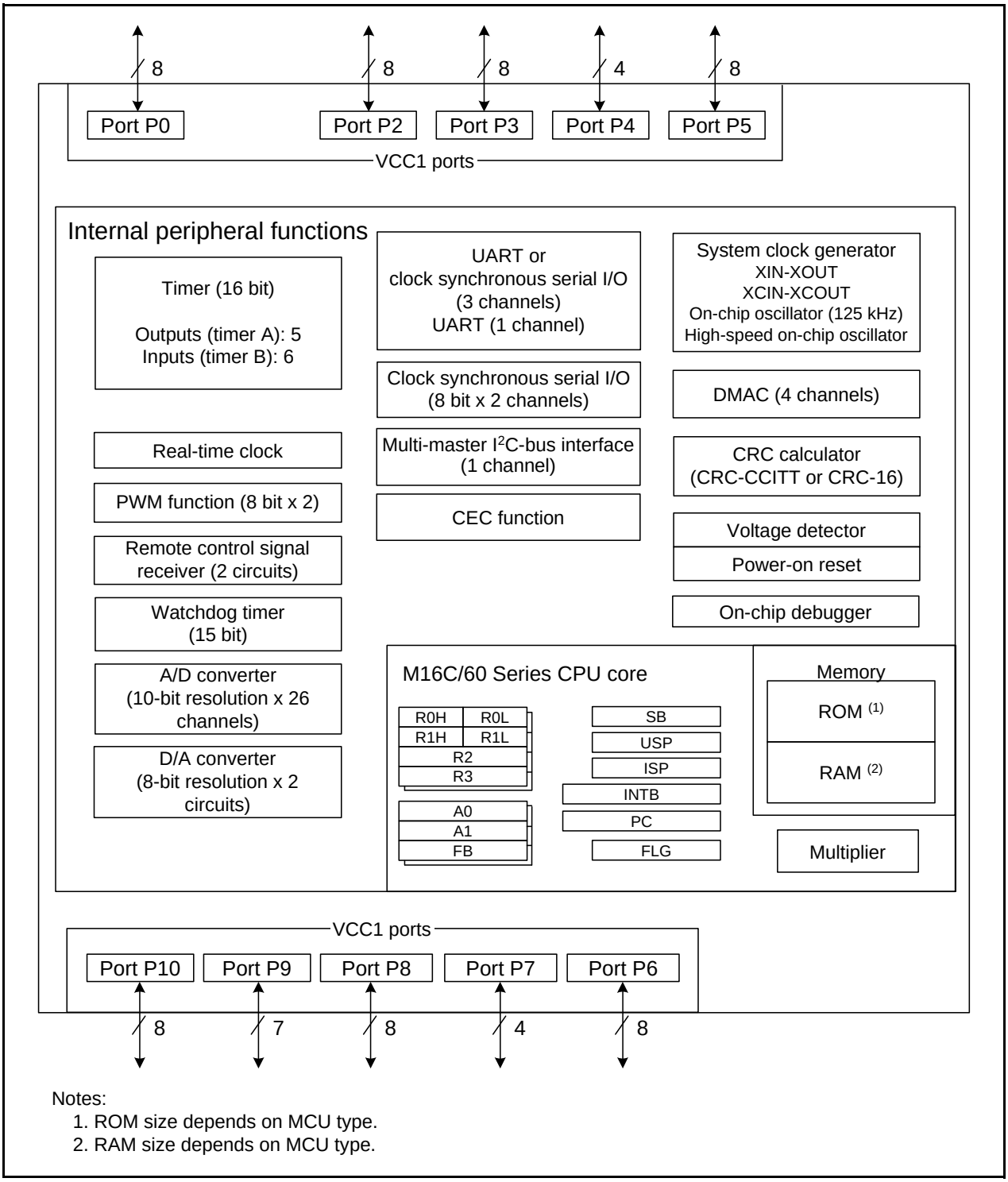
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

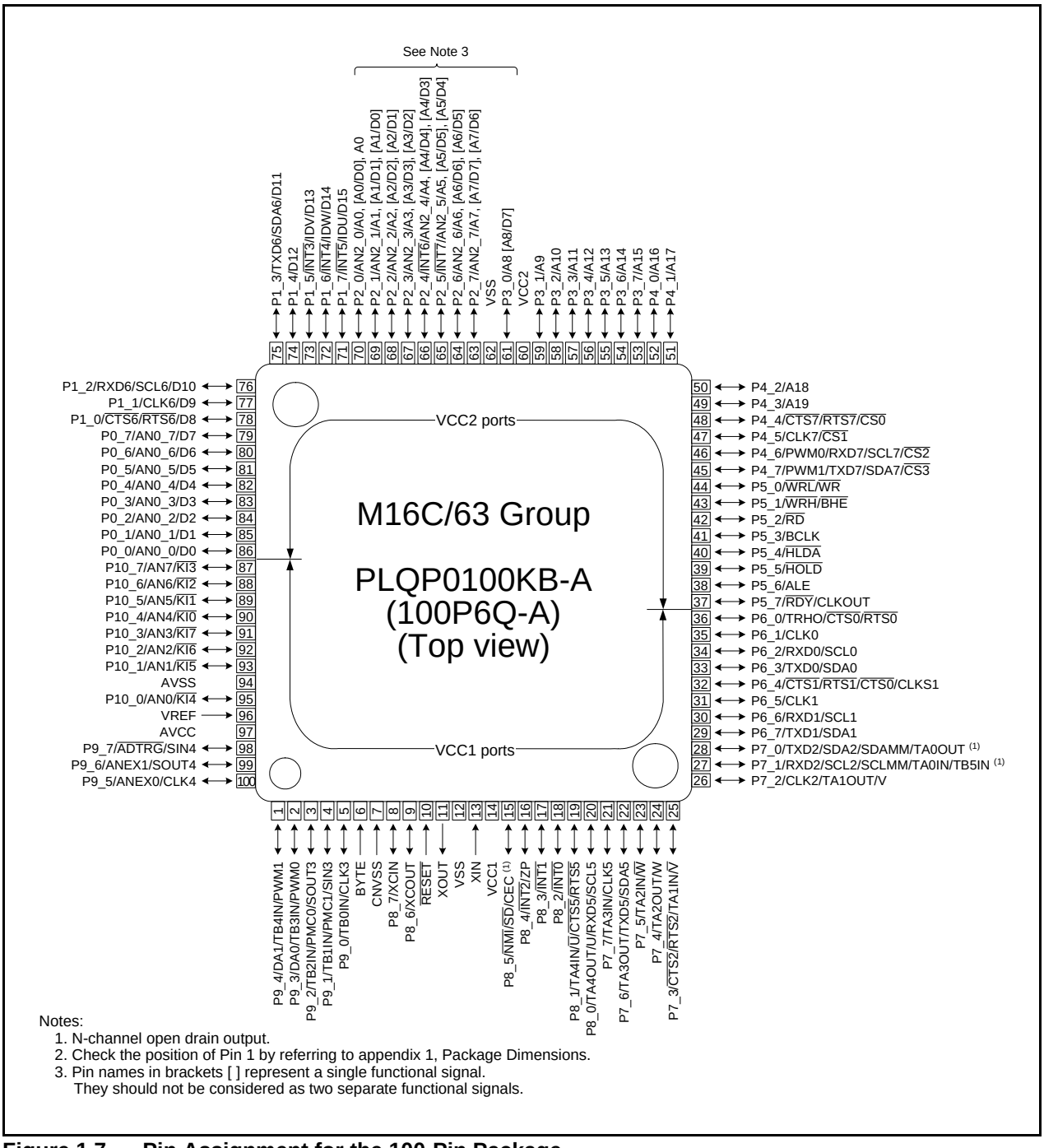
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | EBI/EMI, I²C, SIO, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 31K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-QFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f363amnfa-u0 |




Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

**Figure 1.5 Block Diagram for the 80-Pin Package**




Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

**Figure 1.7 Pin Assignment for the 100-Pin Package**

**Table 1.13 Pin Functions for the 80-Pin Package (1/2)**

| Signal Name | Pin Name | I/O | Power Supply | Description |
|---|---|---|---|---|
| Power supply input | VCC1, VSS | I | - | Apply 1.8 to 5.5 V to the VCC1 pin and 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | I | VCC1 | This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS. |
| Reset input | $\overline{\text{RESET}}$ | I | VCC1 | Driving this pin low resets the MCU. |
| CNVSS | CNVSS | I | VCC1 | Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. |
| Main clock input | XIN | I | VCC1 | I/O pins for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. (1) Input an external clock to XIN pin and leave XOUT pin open. |
| Main clock output | XOUT | O | VCC1 | |
| Sub clock input | XCIN | I | VCC1 | I/O pins for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. (1) Input an external clock to XCIN pin and leave XCOUT pin open. |
| Sub clock output | XCOUT | O | VCC1 | |
| Clock output | CLKOUT | O | VCC1 | Outputs a clock with the same frequency as fC, f1, f8, or f32. |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ | I | VCC1 | Input for the $\overline{\text{INT}}$ interrupt. |
| | $\overline{\text{INT6}}$, $\overline{\text{INT7}}$ | I | VCC1 | |
| $\overline{\text{NMI}}$ interrupt input | $\overline{\text{NMI}}$ | I | VCC1 | Input for the $\overline{\text{NMI}}$ interrupt. |
| Key input interrupt input | $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$ | I | VCC1 | Input for the key input interrupt. |
| Timer A | TA0OUT, TA3OUT, TA4OUT | I/O | VCC1 | I/O for timers A0, A3, and A4 (TA0OUT is N-channel open drain output). |
| | TA0IN, TA3IN, TA4IN | I | VCC1 | Input for timers A0, A3, and A4. |
| | ZP | I | VCC1 | Input for Z-phase. |
| Timer B | TB0IN, TB2IN to TB5IN | I | VCC1 | Input for timers B0, and B2 to B5. |
| Real-time clock output | TRHO | O | VCC1 | Output for the real-time clock. |
| PWM output | PWM0, PWM1 | O | VCC1 | PWM output. |
| Remote control signal receiver input | PMC0 | I | VCC1 | Input for the remote control signal receiver. |

Note:
1. Contact the manufacturer of crystal/ceramic resonator regarding oscillation characteristics.

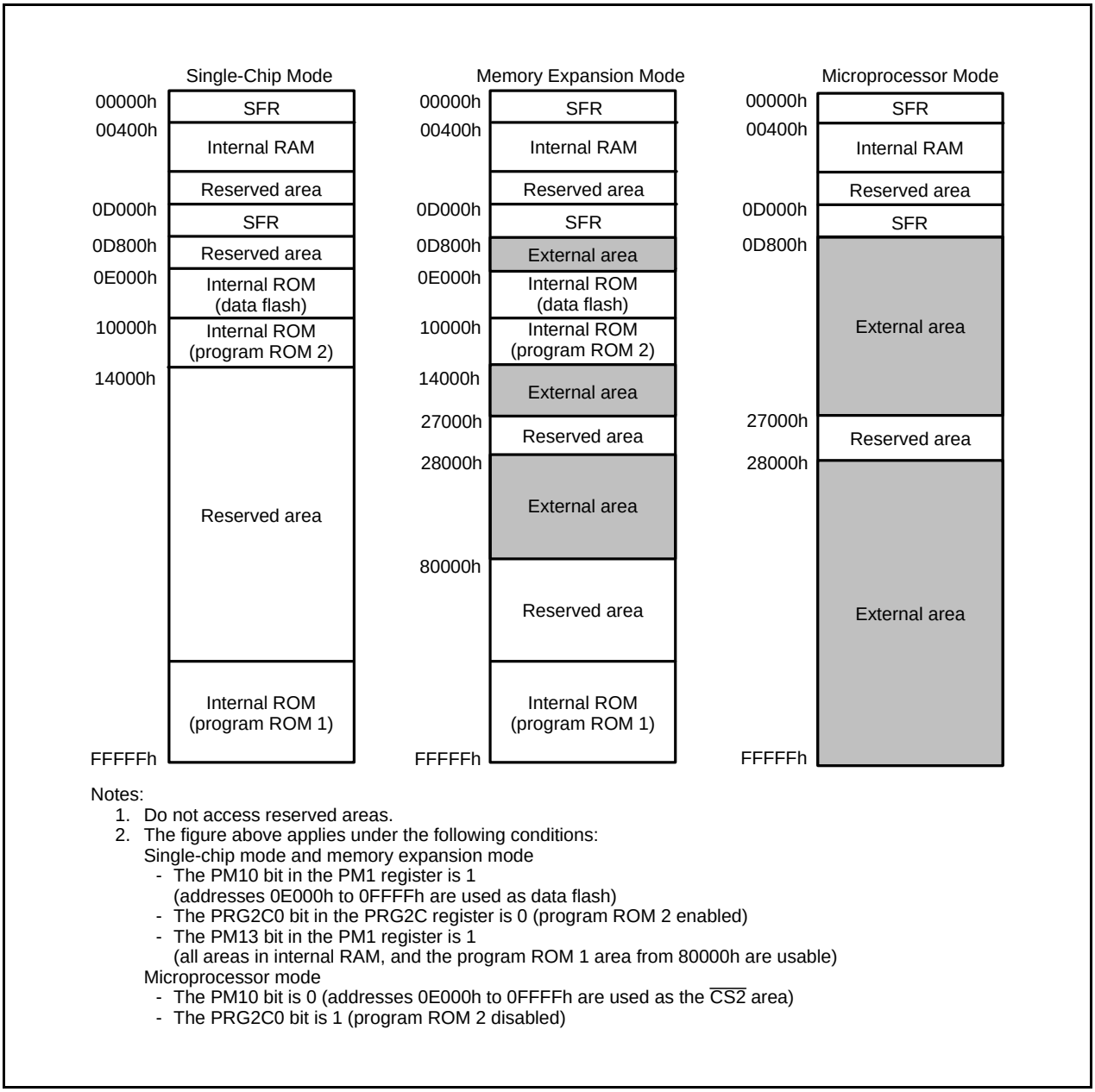
## 3.3 Accessible Area in Each Mode

Areas that can be accessed vary depending on processor mode and the status of each control bit. Figure 3.3 shows the Accessible Area in Each Mode.

In single-chip mode, the SFRs, internal RAM, and internal ROM can be accessed.

In memory expansion mode, the SFRs, internal RAM, internal ROM, and external areas can be accessed. Address space is expandable to 4 MB with the memory area expansion function.

In microprocessor mode, the SFRs, internal RAM, and external areas can be accessed. Address space is expandable to 4 MB with the memory area expansion function. Allocate ROM to the fixed vector table from FFFDCh to FFFFFh.




Notes:
1. Do not access reserved areas.
2. The figure above applies under the following conditions:
   Single-chip mode and memory expansion mode
   - The PM10 bit in the PM1 register is 1
     (addresses 0E000h to 0FFFFh are used as data flash)
   - The PRG2C0 bit in the PRG2C register is 0 (program ROM 2 enabled)
   - The PM13 bit in the PM1 register is 1
     (all areas in internal RAM, and the program ROM 1 area from 80000h are usable)

   Microprocessor mode
   - The PM10 bit is 0 (addresses 0E000h to 0FFFFh are used as the $\overline{CS2}$ area)
   - The PRG2C0 bit is 1 (program ROM 2 disabled)

**Figure 3.3 Accessible Area in Each Mode**

**Table 4.9 SFR Information (9)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0240h | | | |
| 0241h | | | |
| 0242h | | | |
| 0243h | | | |
| 0244h | UART0 Special Mode Register 4 | U0SMR4 | 00h |
| 0245h | UART0 Special Mode Register 3 | U0SMR3 | 000X 0X0Xb |
| 0246h | UART0 Special Mode Register 2 | U0SMR2 | X000 0000b |
| 0247h | UART0 Special Mode Register | U0SMR | X000 0000b |
| 0248h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 0249h | UART0 Bit Rate Register | U0BRG | XXh |
| 024Ah | UART0 Transmit Buffer Register | U0TB | XXh |
| 024Bh | | | XXh |
| 024Ch | UART0 Transmit/Receive Control Register 0 | U0C0 | 0000 1000b |
| 024Dh | UART0 Transmit/Receive Control Register 1 | U0C1 | 00XX 0010b |
| 024Eh | UART0 Receive Buffer Register | U0RB | XXh |
| 024Fh | | | XXh |
| 0250h | UART Transmit/Receive Control Register 2 | UCON | X000 0000b |
| 0251h | | | |
| 0252h | UART Clock Select Register | UCLKSEL0 | X0h |
| 0253h | | | |
| 0254h | UART1 Special Mode Register 4 | U1SMR4 | 00h |
| 0255h | UART1 Special Mode Register 3 | U1SMR3 | 000X 0X0Xb |
| 0256h | UART1 Special Mode Register 2 | U1SMR2 | X000 0000b |
| 0257h | UART1 Special Mode Register | U1SMR | X000 0000b |
| 0258h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 0259h | UART1 Bit Rate Register | U1BRG | XXh |
| 025Ah | UART1 Transmit Buffer Register | U1TB | XXh |
| 025Bh | | | XXh |
| 025Ch | UART1 Transmit/Receive Control Register 0 | U1C0 | 0000 1000b |
| 025Dh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00XX 0010b |
| 025Eh | UART1 Receive Buffer Register | U1RB | XXh |
| 025Fh | | | XXh |
| 0260h | | | |
| 0261h | | | |
| 0262h | | | |
| 0263h | | | |
| 0264h | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 0265h | UART2 Special Mode Register 3 | U2SMR3 | 000X 0X0Xb |
| 0266h | UART2 Special Mode Register 2 | U2SMR2 | X000 0000b |
| 0267h | UART2 Special Mode Register | U2SMR | X000 0000b |
| 0268h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 0269h | UART2 Bit Rate Register | U2BRG | XXh |
| 026Ah | UART2 Transmit Buffer Register | U2TB | XXh |
| 026Bh | | | XXh |
| 026Ch | UART2 Transmit/Receive Control Register 0 | U2C0 | 0000 1000b |
| 026Dh | UART2 Transmit/Receive Control Register 1 | U2C1 | 0000 0010b |
| 026Eh | UART2 Receive Buffer Register | U2RB | XXh |
| 026Fh | | | XXh |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.12 SFR Information (12)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0300h | Timer B3/B4/B5 Count Start Flag | TBSR | 000X XXXXb |
| 0301h | | | |
| 0302h | Timer A1-1 Register | TA11 | XXh |
| 0303h | | | XXh |
| 0304h | Timer A2-1 Register | TA21 | XXh |
| 0305h | | | XXh |
| 0306h | Timer A4-1 Register | TA41 | XXh |
| 0307h | | | XXh |
| 0308h | Three-Phase PWM Control Register 0 | INVC0 | 00h |
| 0309h | Three-Phase PWM Control Register 1 | INVC1 | 00h |
| 030Ah | Three-Phase Output Buffer Register 0 | IDB0 | XX11 1111b |
| 030Bh | Three-Phase Output Buffer Register 1 | IDB1 | XX11 1111b |
| 030Ch | Dead Time Timer | DTT | XXh |
| 030Dh | Timer B2 Interrupt Generation Frequency Set Counter | ICTB2 | XXh |
| 030Eh | Position-Data-Retain Function Control Register | PDRF | XXXX 0000b |
| 030Fh | | | |
| 0310h | Timer B3 Register | TB3 | XXh |
| 0311h | | | XXh |
| 0312h | Timer B4 Register | TB4 | XXh |
| 0313h | | | XXh |
| 0314h | Timer B5 Register | TB5 | XXh |
| 0315h | | | XXh |
| 0316h | | | |
| 0317h | | | |
| 0318h | Port Function Control Register | PFCR | 0011 1111b |
| 0319h | | | |
| 031Ah | | | |
| 031Bh | Timer B3 Mode Register | TB3MR | 00XX 0000b |
| 031Ch | Timer B4 Mode Register | TB4MR | 00XX 0000b |
| 031Dh | Timer B5 Mode Register | TB5MR | 00XX 0000b |
| 031Eh | | | |
| 031Fh | | | |
| 0320h | Count Start Flag | TABSR | 00h |
| 0321h | | | |
| 0322h | One-Shot Start Flag | ONSF | 00h |
| 0323h | Trigger Select Register | TRGSR | 00h |
| 0324h | Increment/Decrement Flag | UDF | 00h |
| 0325h | | | |
| 0326h | Timer A0 Register | TA0 | XXh |
| 0327h | | | XXh |
| 0328h | Timer A1 Register | TA1 | XXh |
| 0329h | | | XXh |
| 032Ah | Timer A2 Register | TA2 | XXh |
| 032Bh | | | XXh |
| 032Ch | Timer A3 Register | TA3 | XXh |
| 032Dh | | | XXh |
| 032Eh | Timer A4 Register | TA4 | XXh |
| 032Fh | | | XXh |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.15 SFR Information (15)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0390h | DMA2 Source Select Register | DM2SL | 00h |
| 0391h | | | |
| 0392h | DMA3 Source Select Register | DM3SL | 00h |
| 0393h | | | |
| 0394h | | | |
| 0395h | | | |
| 0396h | | | |
| 0397h | | | |
| 0398h | DMA0 Source Select Register | DM0SL | 00h |
| 0399h | | | |
| 039Ah | DMA1 Source Select Register | DM1SL | 00h |
| 039Bh | | | |
| 039Ch | | | |
| 039Dh | | | |
| 039Eh | | | |
| 039Fh | | | |
| 03A0h | | | |
| 03A1h | | | |
| 03A2h | Open-Circuit Detection Assist Function Register | AINRST | XX00 XXXXb |
| 03A3h | | | |
| 03A4h | | | |
| 03A5h | | | |
| 03A6h | | | |
| 03A7h | | | |
| 03A8h | | | |
| 03A9h | | | |
| 03AAh | | | |
| 03ABh | | | |
| 03ACh | | | |
| 03ADh | | | |
| 03AEh | | | |
| 03AFh | | | |
| 03B0h | | | |
| 03B1h | | | |
| 03B2h | | | |
| 03B3h | | | |
| 03B4h | SFR Snoop Address Register | CRCSAR | XXXX XXXXb |
| 03B5h | | | 00XX XXXXb |
| 03B6h | CRC Mode Register | CRCMR | 0XXX XXX0b |
| 03B7h | | | |
| 03B8h | | | |
| 03B9h | | | |
| 03BAh | | | |
| 03BBh | | | |
| 03BCh | CRC Data Register | CRCD | XXh |
| 03BDh | | | XXh |
| 03BEh | CRC Input Register | CRCIN | XXh |
| 03BFh | | | |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

## 5.1.5 Flash Memory Electrical Characteristics

### Table 5.9 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

$V_{CC1}$ = 1.8 to 5.5 V, $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| - | CPU rewrite mode | | | | 10 (1) | MHz |
| f(SLOW_R) | Slow read mode | | | | 5 (3) | MHz |
| - | Low current consumption read mode | | | fC(32.768) | 35 | kHz |
| - | Data flash read | 3.0 V < $V_{CC1}$ ≤ 5.5 V | | | 20 (2) | MHz |

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is 1.8 ≤ $V_{CC1}$ ≤ 3.0 V, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

### Table 5.10 Flash Memory (Program ROM 1, 2) Electrical Characteristics

$V_{CC1}$ = 2.7 to 5.5 V at $T_{opr}$ = 0°C to 60°C (option: -40°C to 85°C), unless otherwise specified.

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| - | Program and erase cycles (1), (3), (4) | $V_{CC1}$ = 3.3 V, $T_{opr}$ = 25°C | 1,000 (2) | | | times |
| - | 2 word program time | $V_{CC1}$ = 3.3 V, $T_{opr}$ = 25°C | | 150 | 4000 | µs |
| - | Lock bit program time | $V_{CC1}$ = 3.3 V, $T_{opr}$ = 25°C | | 70 | 3000 | µs |
| - | Block erase time | $V_{CC1}$ = 3.3 V, $T_{opr}$ = 25°C | | 0.2 | 3.0 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | | | $5 + \frac{3}{f_{(BCLK)}}$ | ms |
| - | Interval from erase start/restart until following suspend request | | 0 | | | µs |
| - | Suspend interval necessary for auto-erasure to complete (7) | | 20 | | | ms |
| - | Time from suspend until erase restart | | | | $30 + \frac{1}{f_{(BCLK)}}$ | µs |
| - | Program, erase voltage | | 2.7 | | 5.5 | V |
| - | Read voltage | $T_{opr}$= -20°C to 85°C/-40°C to 85°C | 2.7 | | 5.5 | V |
| - | Program, erase temperature | | 0 | | 60 | °C |
| $t_{PS}$ | Flash memory circuit stabilization wait time | | | | 50 | µs |
| - | Data hold time (6) | Ambient temperature = 55°C | 20 | | | year |

Notes:
1. Definition of program and erase cycles:
   The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

**Table 5.11 Flash Memory (Data Flash) Electrical Characteristics**

$V_{CC1}$ = 2.7 to 5.5 V at $T_{opr}$ = -20 to 85°C/-40 to 85°C, unless otherwise specified.

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| - | Program and erase cycles (1), (3), (4) | $V_{CC1}$ = 3.3 V, $T_{opr}$ = 25°C | 10,000 (2) | | | times |
| - | 2 word program time | $V_{CC1}$ = 3.3 V, $T_{opr}$ = 25°C | | 300 | 4000 | µs |
| - | Lock bit program time | $V_{CC1}$ = 3.3 V, $T_{opr}$ = 25°C | | 140 | 3000 | µs |
| - | Block erase time | $V_{CC1}$ = 3.3 V, $T_{opr}$ = 25°C | | 0.2 | 3.0 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | | | $5 + \frac{3}{f_{(BCLK)}}$ | ms |
| - | Interval from erase start/restart until following suspend request | | 0 | | | µs |
| - | Suspend interval necessary for auto-erasure to complete (7) | | 20 | | | ms |
| - | Time from suspend until erase restart | | | | $30 + \frac{1}{f_{(BCLK)}}$ | µs |
| - | Program, erase voltage | | 2.7 | | 5.5 | V |
| - | Read voltage | | 2.7 | | 5.5 | V |
| - | Program, erase temperature | | –20/–40 | | 85 | °C |
| $t_{PS}$ | Flash memory circuit stabilization wait time | | | | 50 | µs |
| - | Data hold time (6) | Ambient temperature = 55°C | 20 | | | year |

Notes:
1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

### Table 5.14 Voltage Detector 2 Electrical Characteristics

The measurement condition is $V_{CC1}$ = 1.8 to 5.5 V, $T_{opr}$ = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level Vdet2_0 | When $V_{CC1}$ is falling | 3.70 | 4.00 | 4.30 | V |
| - | Hysteresis width at the rising of $V_{CC1}$ in voltage detector 2 | | | 0.15 | | V |
| - | Voltage detector 2 response time (2) | When $V_{CC1}$ falls from 5 V to (Vdet2_0 - 0.1) V | | | 200 | µs |
| - | Voltage detector self power consumption | VC27 = 1, $V_{CC1}$ = 5.0 V | | 1.7 | | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detector operation starts (1) | | | | 100 | µs |

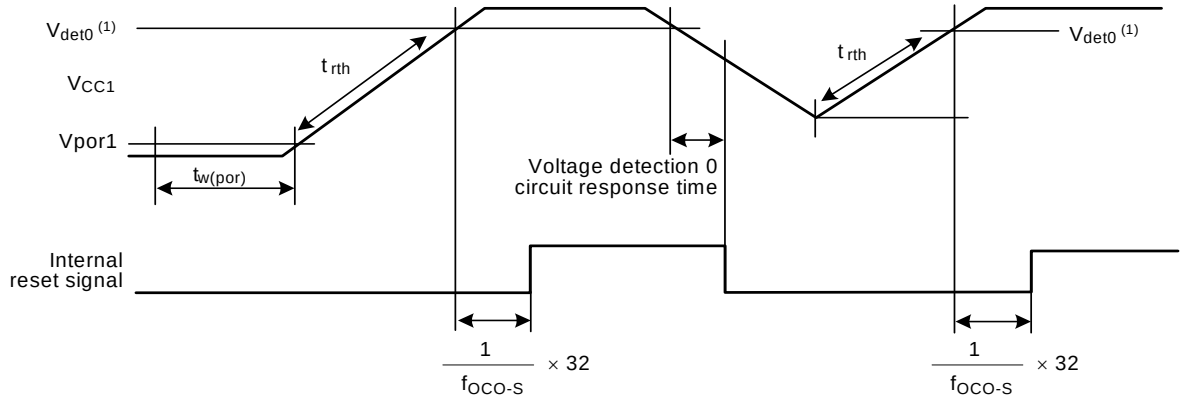
Notes:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.
2. Time from when passing the $V_{det2}$ until when a voltage monitor 2 reset is generated.

### Table 5.15 Power-On Reset Circuit

The measurement condition is $V_{CC1}$ = 2.0 to 5.5 V, $T_{opr}$ = -20°C to 85°C/ -40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por1}$ | Voltage at which power-on reset enabled (1) | | | | 0.5 | V |
| $t_{rth}$ | External power $V_{CC1}$ rise gradient | | 2.0 | | 50000 | mV/ms |
| $t_{w(por)}$ | Time necessary to enable power-on reset | | 300 | | | ms |

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0. Also, set the VDSEL1 bit to 0 (Vdet0_2).




Note:
1. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit.

**Figure 5.4 Power-On Reset Circuit Electrical Characteristics**

$V_{CC1} = V_{CC2} = 5\ V$

## 5.2.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

### 5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

**Table 5.22 Reset Input ($\overline{\text{RESET}}$ Input)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(RSTL)}$ | $\overline{\text{RESET}}$ input low pulse width | 10 | | µs |

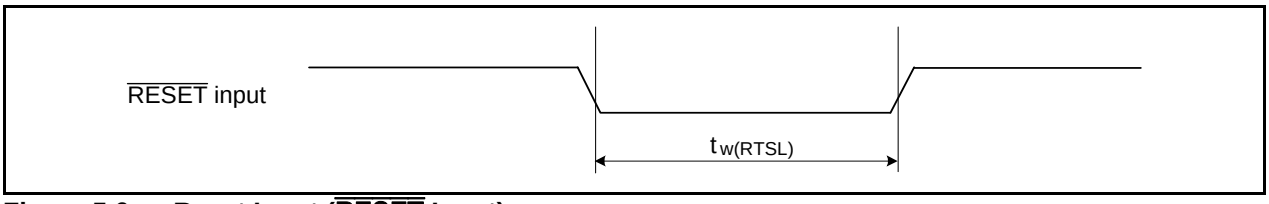



**Figure 5.6 Reset Input ($\overline{\text{RESET}}$ Input)**

### 5.2.2.2 External Clock Input

**Table 5.23 External Clock Input (XIN Input) (1)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External clock input cycle time | 50 | | ns |
| $t_{w(H)}$ | External clock input high pulse width | 20 | | ns |
| $t_{w(L)}$ | External clock input low pulse width | 20 | | ns |
| $t_r$ | External clock rise time | | 9 | ns |
| $t_f$ | External clock fall time | | 9 | ns |

Note:
1. The condition is $V_{CC1} = V_{CC2} = 3.0$ to 5.0 V.

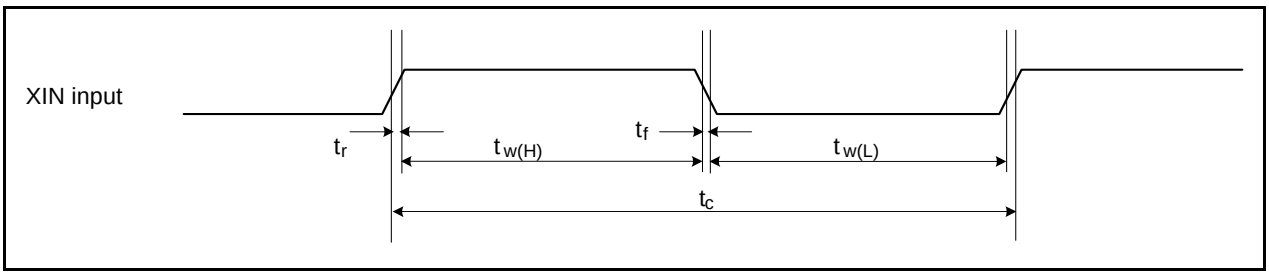



**Figure 5.7 External Clock Input (XIN Input)**

$V_{CC1} = V_{CC2} = 5\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

### 5.2.2.5 Serial Interface

**Table 5.32 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi input high pulse width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi input low pulse width | 100 | | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | | ns |

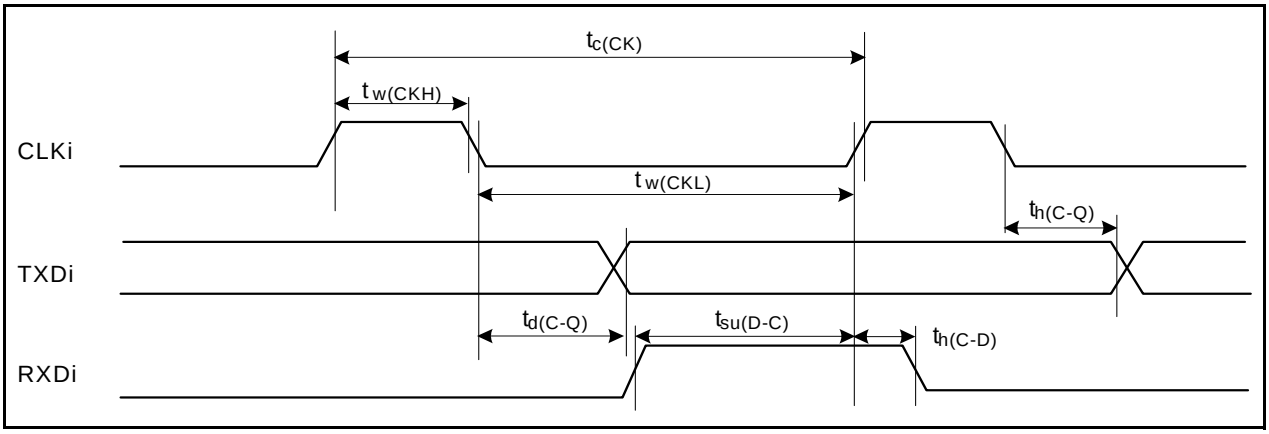



**Figure 5.11 Serial Interface**

### 5.2.2.6 External Interrupt $\overline{INTi}$ Input

**Table 5.33 External Interrupt $\overline{INTi}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{INTi}$ input high pulse width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{INTi}$ input low pulse width | 250 | | ns |

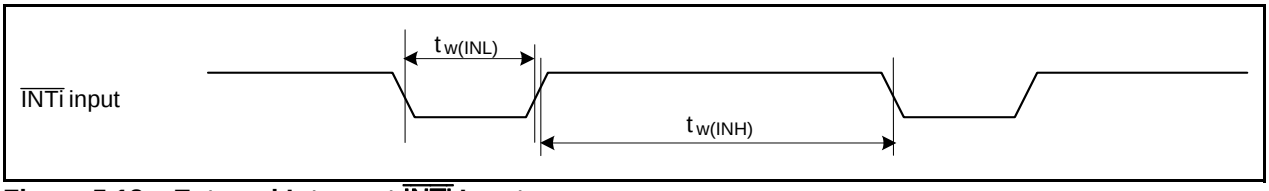
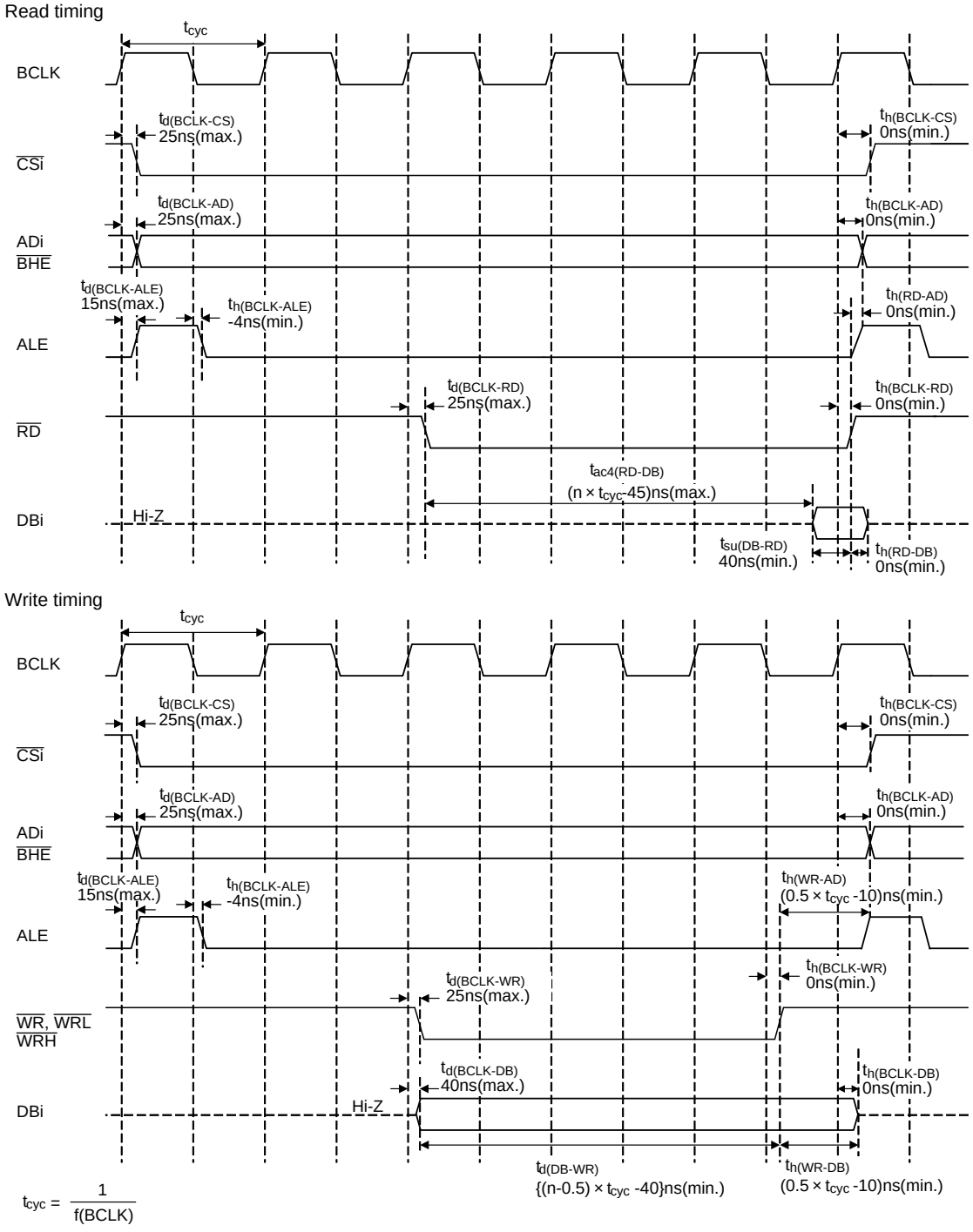



**Figure 5.12 External Interrupt $\overline{INTi}$ Input**

Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 5V$




$t_{cyc} = \frac{1}{f(BCLK)}$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V
- Output timing voltage: $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V

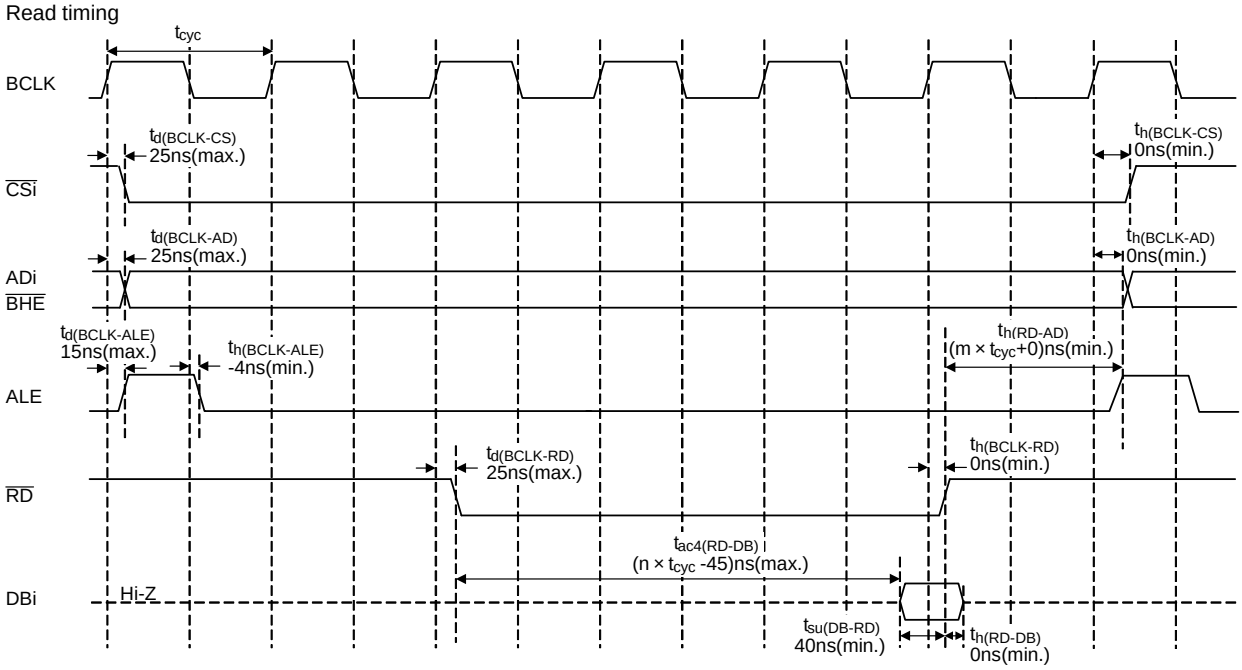
n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

**Figure 5.19 Timing Diagram**

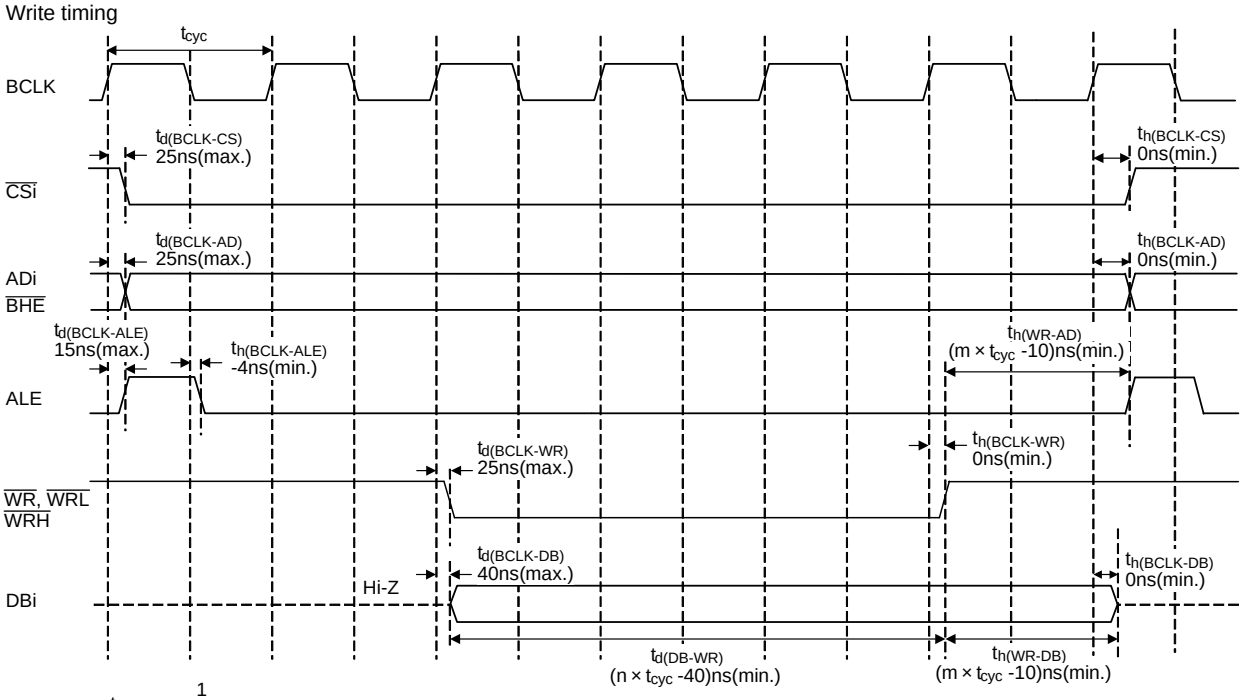
Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and
when inserting 1 to 3 recovery cycles and accessing external area)

$V_{CC1} = V_{CC2} = 5V$

Read timing




Write timing




$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V
- Output timing voltage: $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

m: 1 (when 1 recovery cycle inserted )
2 (when 2 recovery cycles inserted)
3 (when 3 recovery cycles inserted)

**Figure 5.20 Timing Diagram**

$V_{CC1} = V_{CC2} = 3$ V

**Table 5.42 Electrical Characteristics (2)**

$V_{CC1} = V_{CC2} = 2.7$ to 3.3 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/–40°C to 85°C, $f_{(BCLK)} = 20$ MHz unless otherwise specified.

| Symbol | Parameter | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power supply current<br><br>In single-chip, mode, the output pin are open and other pins are $V_{SS}$ | High-speed mode | $f_{(BCLK)}$ = 20 MHz (no division)<br>XIN = 20 MHz (square wave)<br>125 kHz on-chip oscillator stopped<br>CM15 = 1 (drive capacity High)<br>A/D converter stopped | | 9.5 | | mA |
| | | | $f_{(BCLK)}$ = 20 MHz (no division)<br>XIN = 20 MHz (square wave)<br>125 kHz on-chip oscillator stopped<br>CM15 = 1 (drive capacity High)<br>A/D converter operating (2) | | 10.2 | | mA |
| | | | $f_{(BCLK)}$ = 20 MHz<br>XIN = 20 MHz (square wave)<br>125 kHz on-chip oscillator stopped<br>CM15 = 0 (drive capacity Low)<br>A/D converter stopped | | 9.2 | | mA |
| | | | $f_{(BCLK)}$ = 20 MHz (no division)<br>XIN = 20 MHz (square wave)<br>125 kHz on-chip oscillator stopped<br>CM15 = 1 (drive capacity High)<br>PCLKSTP1 = FF (peripheral clock stopped) | | 7.9 | | mA |
| | | | $f_{(BCLK)}$ = 20 MHz (no division)<br>XIN = 20 MHz (square wave)<br>125 kHz on-chip oscillator stopped<br>CM15 = 0 (drive capacity Low)<br>PCLKSTP1 = FF (peripheral clock stopped) | | 7.6 | | mA |
| | | 40 MHz on-chip oscillator mode | Main clock stopped<br>40 MHz on-chip oscillator on,<br>divide-by-2 ($f_{(BCLK)}$ = 20 MHz)<br>125 kHz on-chip oscillator stopped | | 9.0 | | mA |
| | | 125 kHz on-chip oscillator mode | Main clock stopped<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator on, no division<br>FMR22 = 1 (slow read mode) | | 450.0 | | µA |
| | | Low-power mode | $f_{(BCLK)}$ = 32 MHz<br>FMR 22 = FMR23 = 1 (in low-current consumption read mode)<br>On flash memory (1) | | 80.0 | | µA |
| | | Wait mode | f(BCLK) = 32 kHz<br>Main clock stopped<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator on<br>PM25 = 1 (peripheral function clock fC operating)<br>$T_{opr}$ = 25°C<br>Real-time clock operating | | 5.3 | | µA |
| | | | $f_{(BCLK)}$ = 32 MHz<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator stopped<br>PM25 = 0 (peripheral function clock fC stopped)<br>$T_{opr}$ = 25°C | | 5.0 | | µA |
| | | Stop mode | $T_{opr}$ = 25°C | | 2.2 | | µA |
| | | During flash memory program | $f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait)<br>$V_{CC1}$ = 3.0 V | | 20.0 | | mA |
| | | During flash memory erase | $f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait)<br>$V_{CC1}$ = 3.0 V | | 30.0 | | mA |

Notes:
1. This indicates the memory in which the program to be executed exists.
2. A/D conversion is executed in repeat mode.

$V_{CC1} = V_{CC2} = 3\ V$

## 5.3.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

### 5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

**Table 5.43 Reset Input ($\overline{\text{RESET}}$ Input)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(RSTL)}$ | $\overline{\text{RESET}}$ input low pulse width | 10 | | µs |

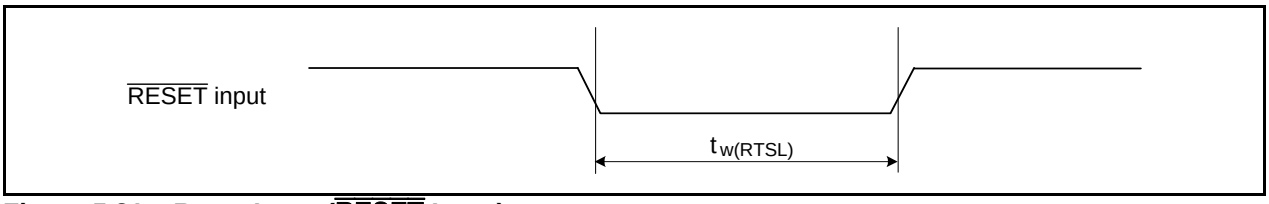



**Figure 5.21 Reset Input ($\overline{\text{RESET}}$ Input)**

### 5.3.2.2 External Clock Input

**Table 5.44 External Clock Input (XIN Input) (1)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External clock input cycle time | 50 | | ns |
| $t_{w(H)}$ | External clock input high pulse width | 20 | | ns |
| $t_{w(L)}$ | External clock input low pulse width | 20 | | ns |
| $t_r$ | External clock rise time | | 9 | ns |
| $t_f$ | External clock fall time | | 9 | ns |

Note:
1. The condition is $V_{CC1} = V_{CC2} = 2.7$ to 3.0 V.

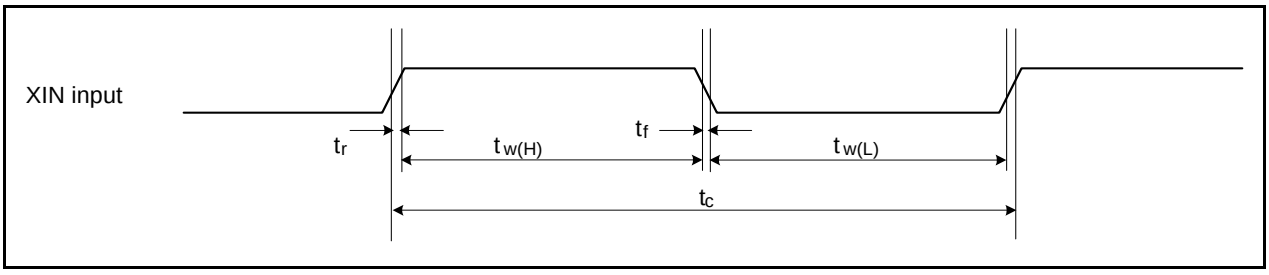



**Figure 5.22 External Clock Input (XIN Input)**

$V_{CC1} = V_{CC2} = 3\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

### 5.3.2.4 Timer B Input

**Table 5.50 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on one edge) | 150 | | ns |
| $t_{w(TBH)}$ | TBiIN input high pulse width (counted on one edge) | 60 | | ns |
| $t_{w(TBL)}$ | TBiIN input low pulse width (counted on one edge) | 60 | | ns |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on both edges) | 300 | | ns |
| $t_{w(TBH)}$ | TBiIN input high pulse width (counted on both edges) | 120 | | ns |
| $t_{w(TBL)}$ | TBiIN input low pulse width (counted on both edges) | 120 | | ns |

**Table 5.51 Timer B Input (Pulse Period Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN input high pulse width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN input low pulse width | 300 | | ns |

**Table 5.52 Timer B Input (Pulse Width Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN input high pulse width | 300 | | ns |
| $t^{w(TBL)}$ | TBiIN input low pulse width | 300 | | ns |

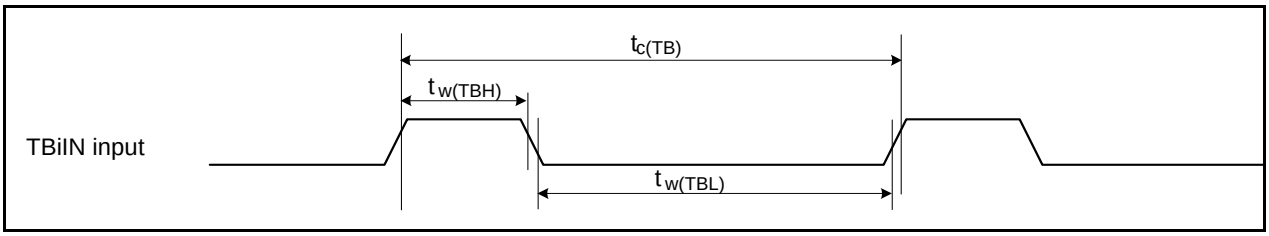
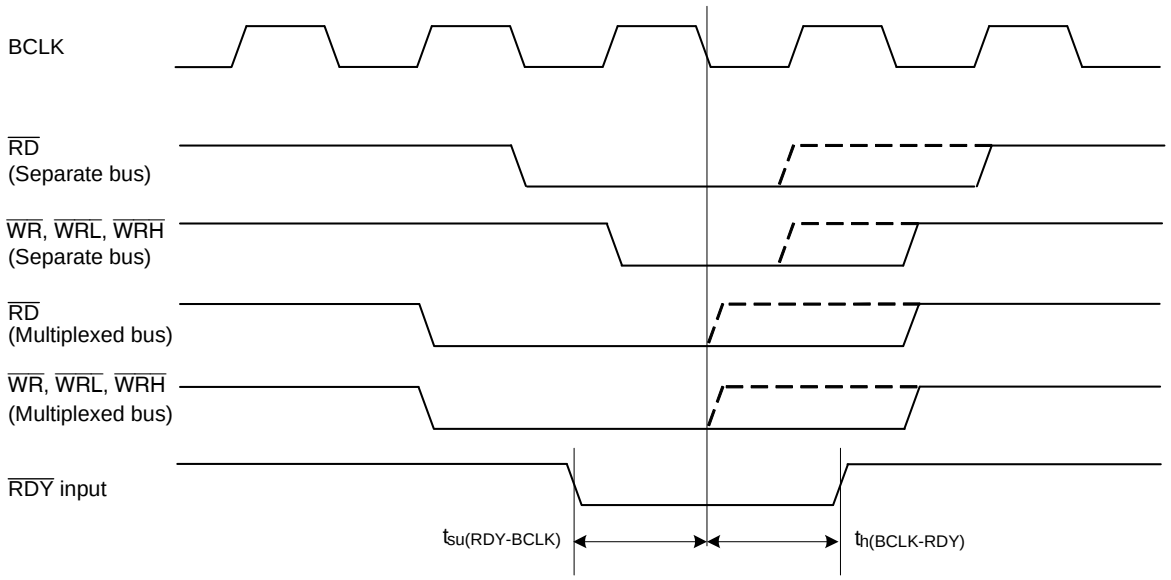



**Figure 5.25 Timer B Input**

Memory Expansion Mode and Microprocessor Mode

$V_{CC1} = V_{CC2} = 3\ V$

**(**Effective in wait state setting**)**




Measuring conditions

- $V_{CC1} = V_{CC2} = 3\ V$
- Input timing voltage: $V_{IL} = 0.6\ V$, $V_{IH} = 2.4\ V$
- Output timing voltage: $V_{OL} = 1.5\ V$, $V_{OH} = 1.5\ V$

**Figure 5.29 Timing Diagram**

$V_{CC1} = V_{CC2} = 3\ V$

**Switching Characteristics**

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

### 5.3.4.2 In 1 to 3 Waits Setting and When Accessing External Area

**Table 5.58 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)**

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address output delay time | See Figure 5.30 | | 30 | ns |
| $t_{h(BCLK-AD)}$ | Address output hold time (in relation to BCLK) | | 0 | | ns |
| $t_{h(RD-AD)}$ | Address output hold time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address output hold time (in relation to WR) | | (Note 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip select output delay time | | | 30 | ns |
| $t_{h(BCLK-CS)}$ | Chip select output hold time (in relation to BCLK) | | 0 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE signal output delay time | | | 25 | ns |
| $t_{h(BCLK-ALE)}$ | ALE signal output hold time | | -4 | | ns |
| $t_{d(BCLK-RD)}$ | RD signal output delay time | | | 30 | ns |
| $t_{h(BCLK-RD)}$ | RD signal output hold time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR signal output delay time | | | 30 | ns |
| $t_{h(BCLK-WR)}$ | WR signal output hold time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data output delay time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data output hold time (in relation to BCLK) (3) | | 0 | | ns |
| $t_{d(DB-WR)}$ | Data output delay time (in relation to WR) | | (Note 1) | | ns |
| $t_{h(WR-DB)}$ | Data output hold time (in relation to WR) (3) | | (Note 2) | | ns |

Notes:

1. Calculated according to the BCLK frequency as follows:

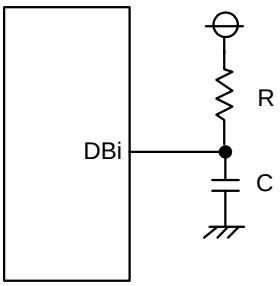
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

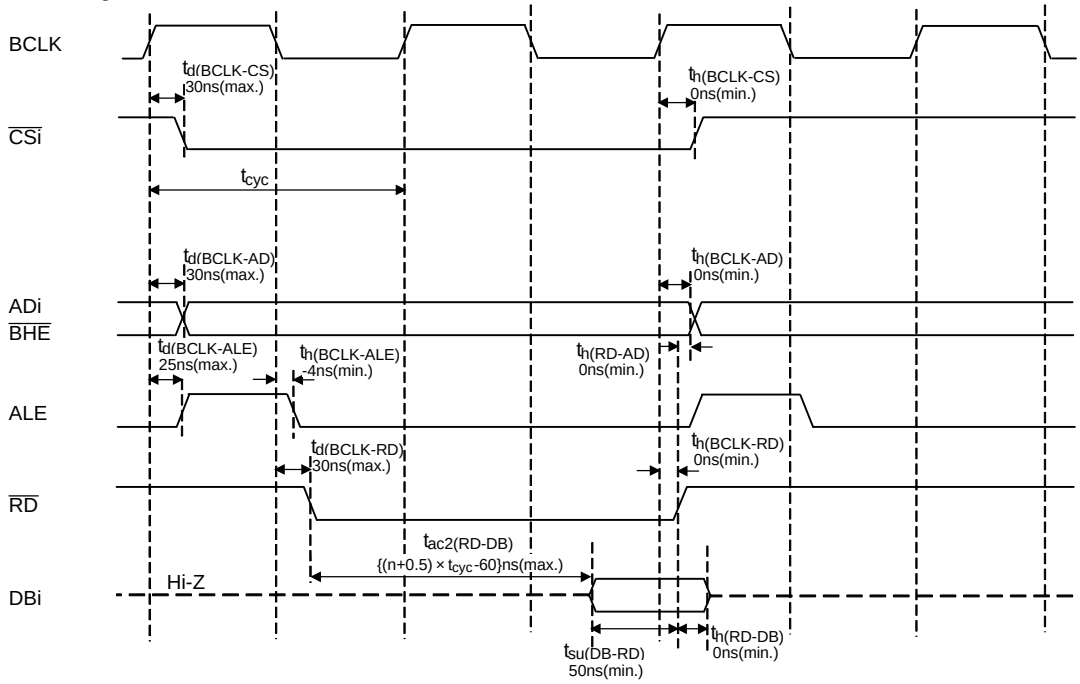
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



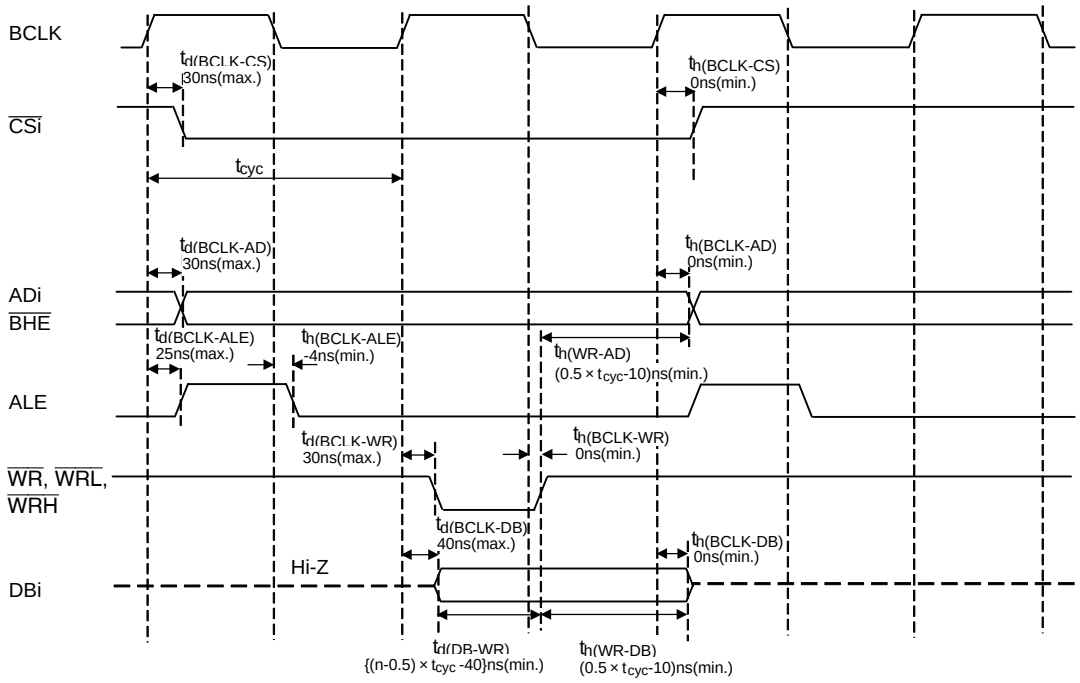
Memory Expansion Mode and Microprocessor Mode
(in 1 to 3 waits setting and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$

Read timing




Write timing




$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 1 (when 1 wait)
2 (when 2 waits)
3 (when 3 waits)

**Figure 5.32 Timing Diagram**