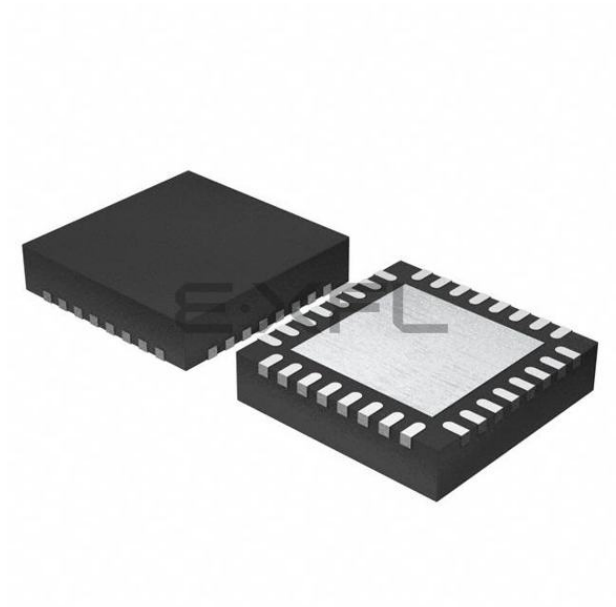

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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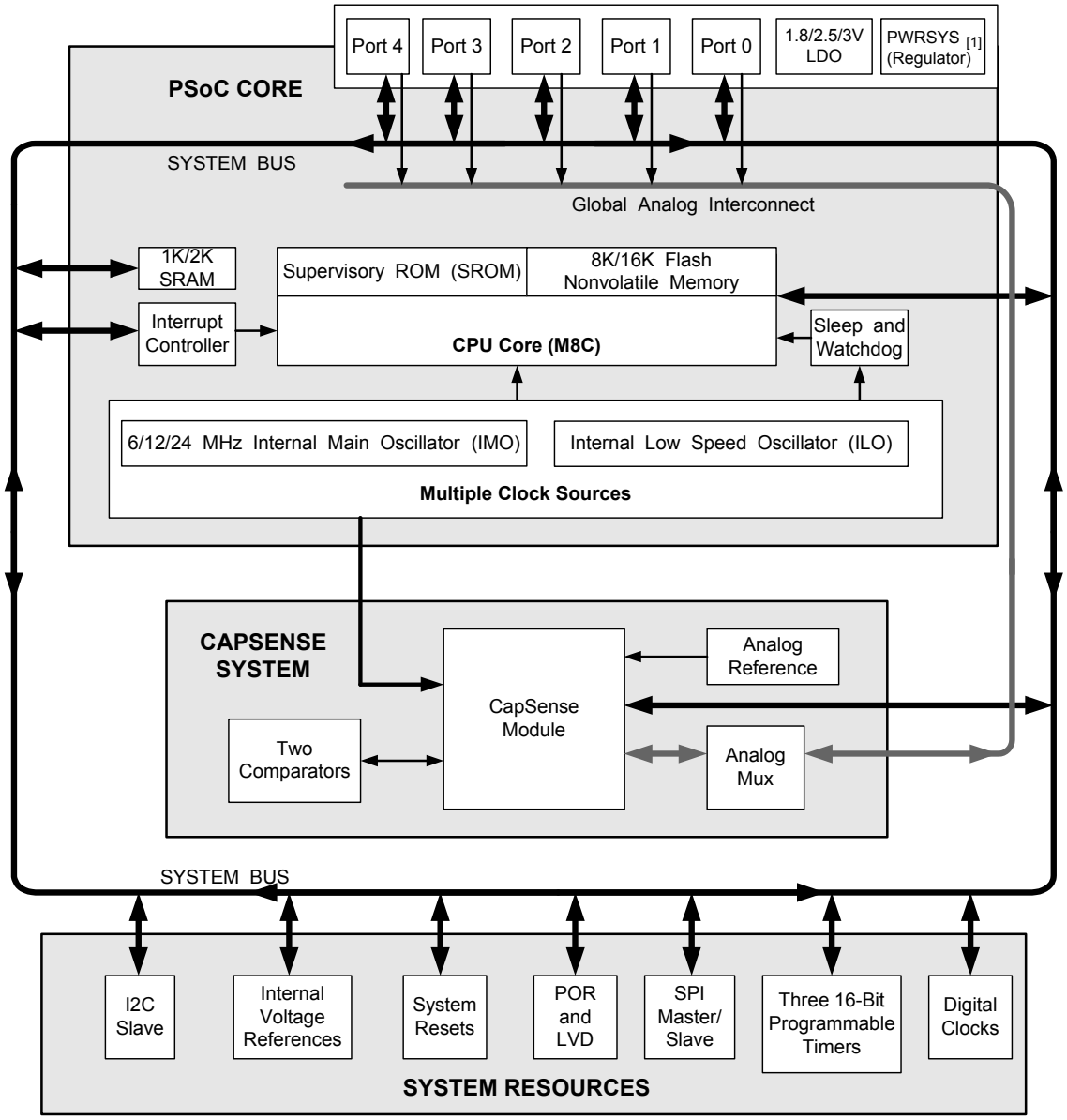
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY8C20xx6A
RAM Size	2K x 8
Interface	I²C, SPI
Number of I/O	28
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20446a-24lqxit

Logic Block Diagram



Note
1. Internal voltage regulator for internal circuitry

PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low-cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The core
- CapSense analog system
- System resources (including a full-speed USB port).

A common, versatile bus allows connection between the I/O and the analog system.

Each CY8C20336H/446H PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

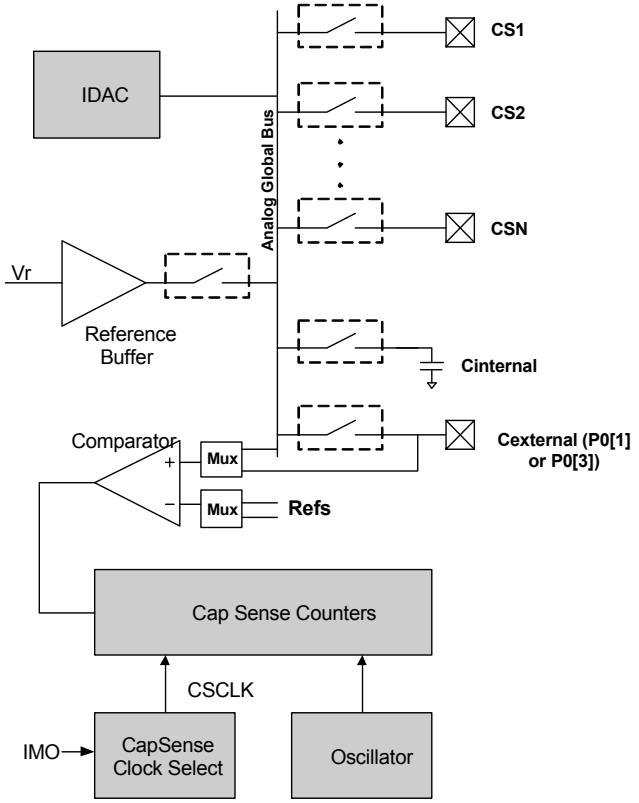
CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1-V or 1.2-V analog reference, which together support capacitive sensing of up to 28 inputs[2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

SmartSense™

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy-to-use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

Figure 1. CapSense System Block Diagram



Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Haptics TS2000 Controller

The CY8C20336H/CY8C20446H family of devices feature an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

Note
2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I^2C + 1 pin for modulator capacitor.

Additional System Resources

System resources provide additional capability, such as configurable USB and I^2C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I^2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I^2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I^2C enhanced slave interface appears as a 32-byte RAM buffer to the external I^2C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note I2C Enhanced Slave Operation - AN56007.
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

For in depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

The CY8C20336H/CY8C20446H PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

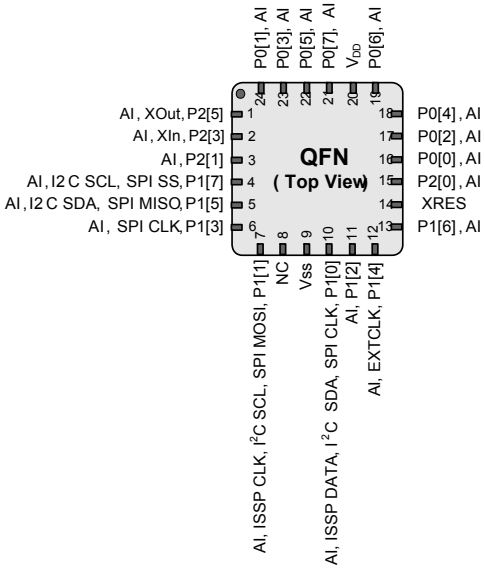
24-Pin QFN

Table 1. Pin Definitions - CY8C20336H [3, 4]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[5], I^2C SCL, SPI MOSI
8			NC	No connection
9	Power		Vss	Ground connection
10	IOHR	I	P1[0]	ISSP DATA[5], I^2C SDA, SPI CLK
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down
15	I/O	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		V_{DD}	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C20336H PSoC Device



Notes
3. During power-up or reset event, device P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter any issues.
4. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
5. These are the ISSP pins, which are not High Z at POR (Power On Reset).

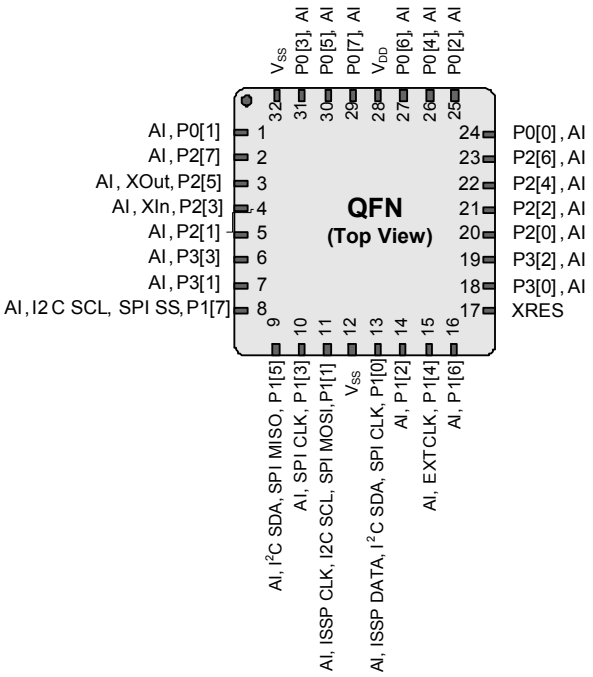
32-Pin QFN

Table 2. Pin Definitions - CY8C20446H PSoC Device [6, 7]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I^2C SCL, SPI SS
9	IOHR	I	P1[5]	I^2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[8], I^2C SCL, SPI MOSI.
12	Power		Vss	Ground connection.
13	IOHR	I	P1[0]	ISSP DATA[8], I^2C SDA., SPI CLK
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V_{DD}	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 3. CY8C20446H PSoC Device



Notes
6. During power-up or reset event, device P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter any issues.
7. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
8. These are the ISSP pins, which are not High Z at POR (Power On Reset).

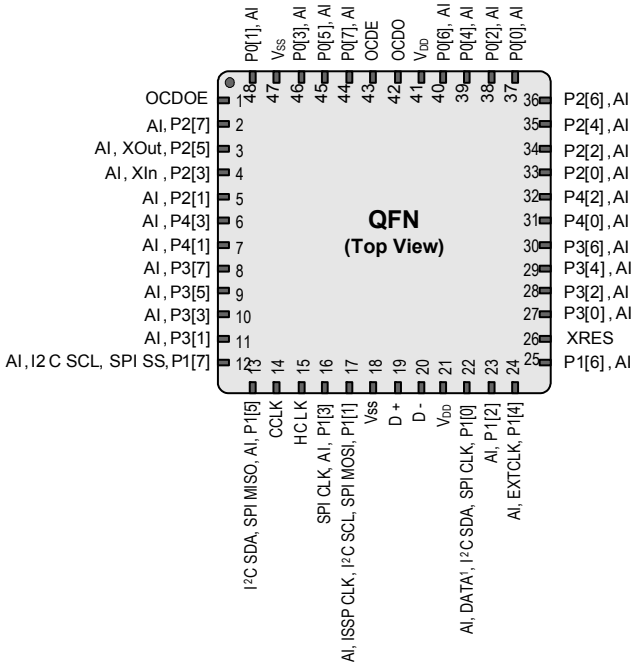
48-Pin QFN OCD

The 48-pin QFN part is for the CY8C20066A On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.[9]

Table 3. Pin Definitions - CY8C20066A PSoC Device [10, 11]

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			CCLK	OCD CPU clock output
15			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK[12], I^2C SCL, SPI MOSI
18	Power		Vss	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[12], I^2C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			OCDO	OCD even data I/O
43			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

Figure 4. CY8C20066A PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

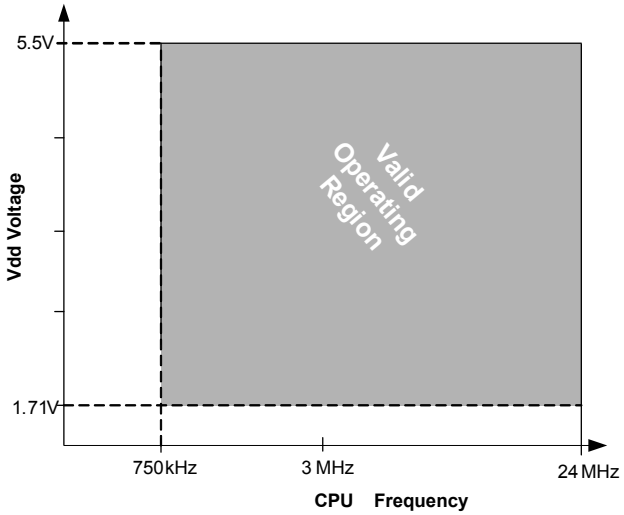
Notes

9. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
10. During power-up or reset event, device P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter any issues.
11. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
12. These are the ISSP pins, which are not High Z at power on reset (POR).

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36H/46H PSoC devices. For the latest electrical specifications, confirm that you have the most recent data sheet by visiting the web at http://www.cypress.com/psoc.

Figure 5. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to V_{SS}		–0.5	–	+6.0	V
V_{IO}	DC input voltage		V_{SS} – 0.5	–	V_{DD} + 0.5	V
V_{IOZ}	DC voltage applied to tristate		V_{SS} –0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin		–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
LU	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature		–40	–	+85	°C
T_C	Commercial temperature range		0	–	70	°C
T_J	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 28. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85°C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7. 3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.60	8	kΩ
V_{OH1}	High output voltage port 2 or 3 pins	I_{OH} ≤ 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage port 2 or 3 pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH3}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH5}	High output voltage port 1 pins with LDO regulator enabled for 3 V out	I_{OH} < 10 µA, V_{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V_{OH6}	High output voltage port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, V_{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage port 1 pins with LDO enabled for 2.5 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V_{OH10}	High output voltage port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.80	V
V_{IH}	Input high voltage		2.00	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

Table 8. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.60	8	kΩ
V_{OH1}	High output voltage port 2 or 3 pins	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage port 2 or 3 pins	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.40	–	–	V
V_{OH3}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH5A}	High output voltage port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V_{OH6A}	High output voltage port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.72	V
V_{IH}	Input high voltage		1.40	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

Table 9. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.60	8	kΩ
V_{OH1}	High output voltage port 2 or 3 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage port 2 or 3 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH3}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V_{IL}	Input low voltage		–	–	0.30 × V_{DD}	V
V_{IH}	Input high voltage		0.65 × V_{DD}	–	–	V

Table 9. 1.71 V to 2.4 V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

Table 10.DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	900	–	1575	Ω
Rusba	USB D+ pull-up resistance	While receiving traffic	1425	–	3090	Ω
Vohusb	Static output high		2.8	–	3.6	V
Volusb	Static output low		–	–	0.3	V
Vdi	Differential input sensitivity		0.2	–	–	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single-ended receiver threshold		0.8	–	2.0	V
Cin	Transceiver capacitance		–	–	50	pF
Iio	High-Z state data line leakage	On D+ or D- line	–10	–	+10	µA
Rps2	PS/2 pull-up resistance		3000	5000	7000	Ω
Rext	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus		–	–	800	Ω
R_{GND}	Resistance of initialization switch to V_{SS}		–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V_{DD}	0.0	–	1.8	V
I_{LPC}	LPC supply current		–	10	40	µA
V_{OSLPC}	LPC voltage offset		–	2.5	30	mV

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C ≤ TA ≤ 85 °C, 1.71 V ≤ V_{DD} ≤ 5.5 V.

Table 13. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator response time	50-mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to V_{DD} – 0.2 V	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	µA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input Range			0	–	1.5	V

ADC Electrical Specifications

Table 14.ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range		0	–	VREFADC	V
C_{IIN}	Input capacitance		–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage		1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications on page 18 for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data clock)	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity		–1	–	+2	LSB
INL	Integral nonlinearity		–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current		–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (V_{DD} > 3.0 V)	–	24	–	dB
		PSRR (V_{DD} < 3.0 V)	–	30	–	dB

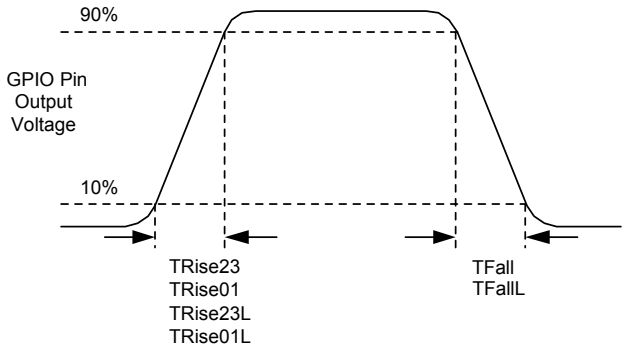
AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode port 0, 1	0 0	– –	6 MHz for 1.71 V <V_{DD} < 2.40 V 12 MHz for 2.40 V < V_{DD}< 5.50 V	MHz
T_{RISE23}	Rise time, strong mode, Cload = 50 pF ports 2 or 3	V_{DD} = 3.0 to 3.6 V, 10% – 90%	15	–	80	ns
$T_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, ports 2 or 3	V_{DD} = 1.71 to 3.0 V, 10% – 90%	15	–	80	ns
T_{RISE01}	Rise time, strong mode, Cload = 50 pF ports 0 or 1	V_{DD} = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	–	50	ns
$T_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, ports 0 or 1	V_{DD} = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	10	–	80	ns
T_{FALL}	Fall time, strong mode, Cload = 50 pF all ports	V_{DD} = 3.0 to 3.6 V, 10% – 90%	10	–	50	ns
T_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	V_{DD} = 1.71 to 3.0 V, 10% – 90%	10	–	70	ns

Figure 6. GPIO Timing Diagram



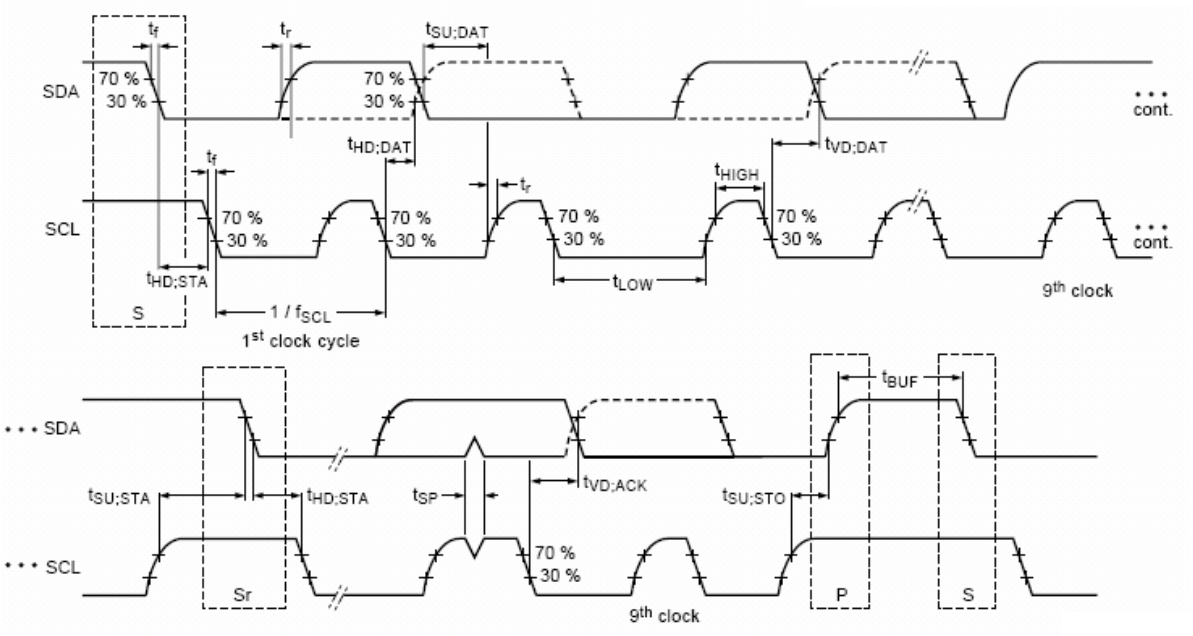
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 24. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.9	µs
$t_{SU;DAT}$	Data setup time	250	–	100[20]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUF}	Bus-free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SP}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns

Figure 8. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

20. A Fast-Mode I²C-bus device can be used in a Standard Mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Figure 10. SPI Master Mode 1 and 3

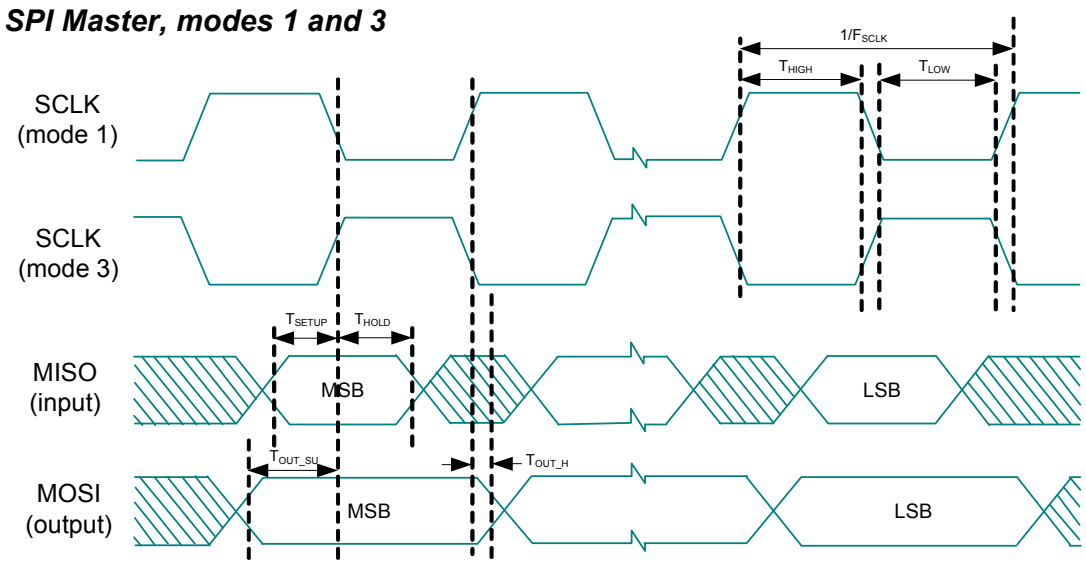


Table 26. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
T_{LOW}	SCLK low time	–	42	–	–	ns
T_{HIGH}	SCLK high time	–	42	–	–	ns
T_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
T_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
T_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
T_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
T_{SS_HIGH}	SS high time	–	50	–	–	ns
T_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
T_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 11. SPI Slave Mode 0 and 2

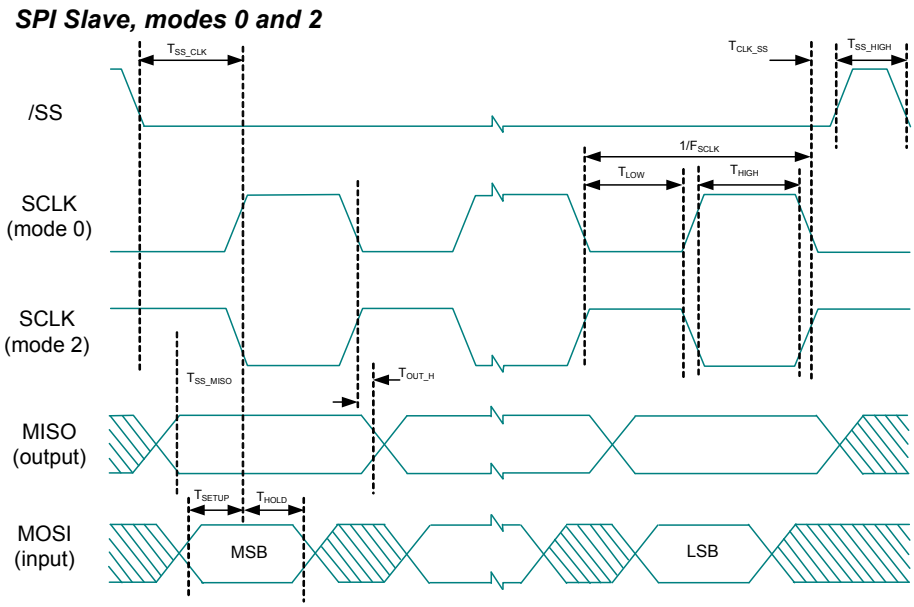


Figure 12. SPI Slave Mode 1 and 3

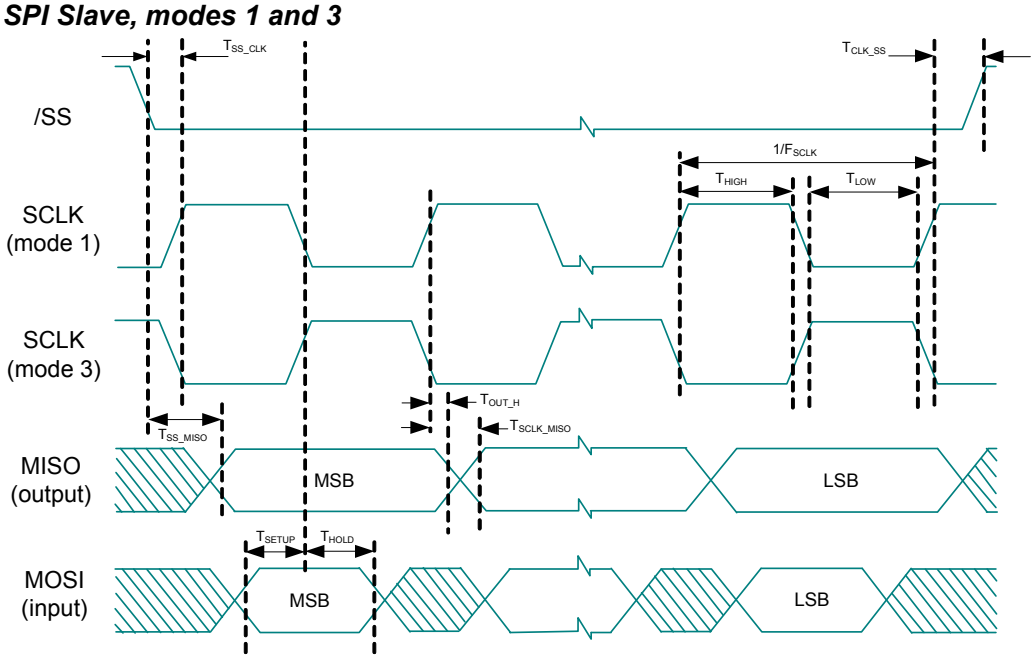
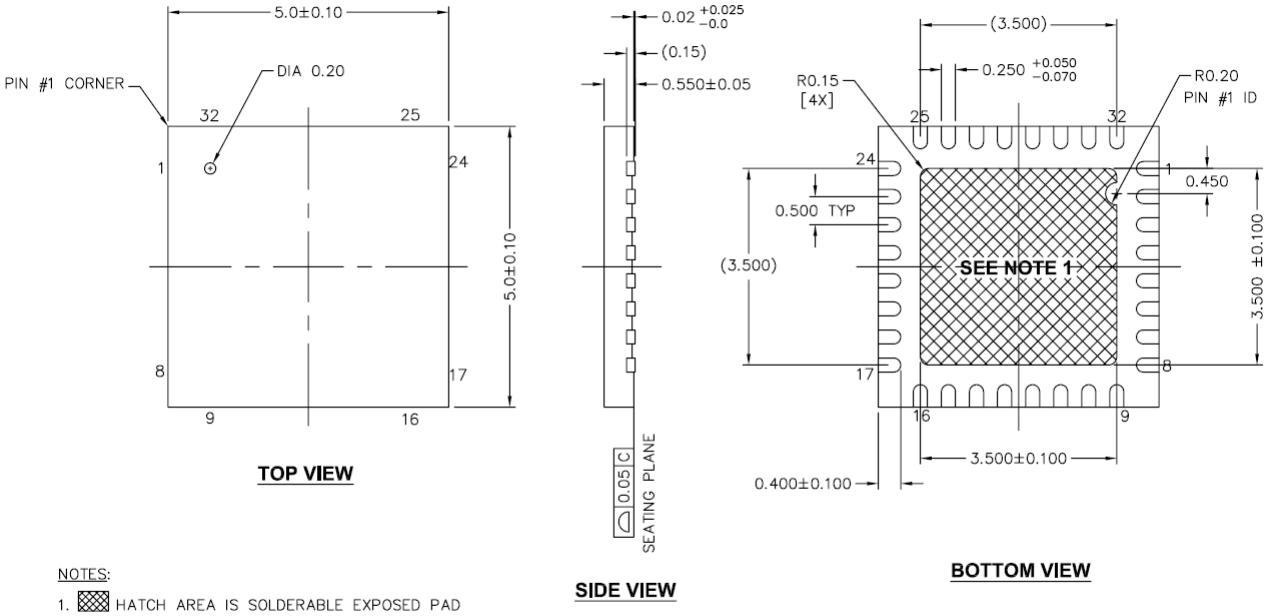


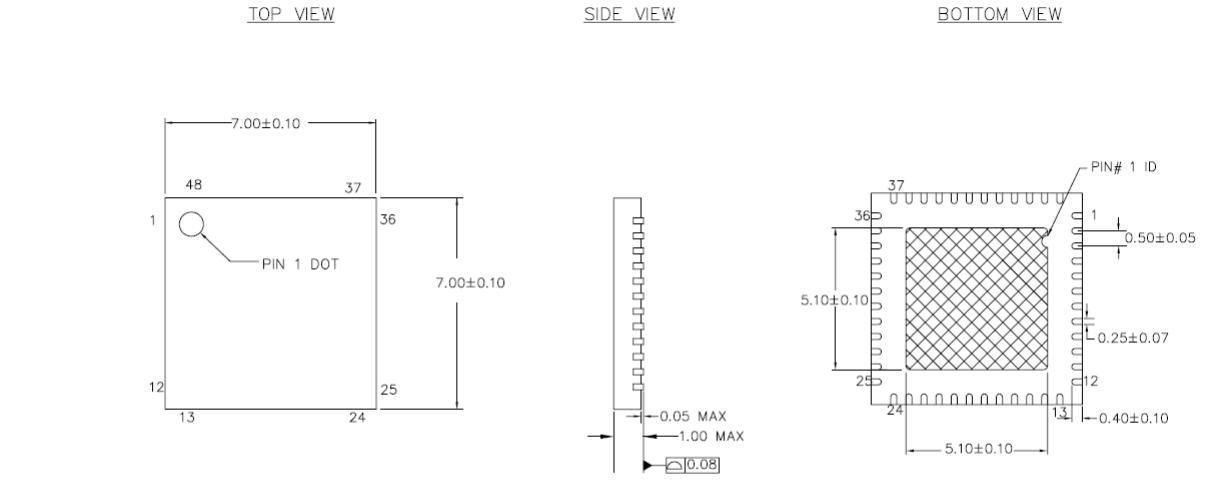
Figure 14. 32-Pin (5 × 5 × 0.55 mm) QFN



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Figure 15. 48-Pin (7 × 7 × 1.0 mm) QFN



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *G

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 27. Thermal Impedances per Package

Package	Typical θ_{JA} [21]
24-QFN[22]	20.90 °C/W
32-QFN[22]	19.51 °C/W
48-QFN[22]	17.68 °C/W

Capacitance on Crystal Pins

Table 28. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
24-pin QFN	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

Notes
21. $T_J = T_A$ + Power x θ_{JA}.
22. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.
23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240-V power supply, Euro-Plug adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466A-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3280-20x66 Universal CapSense Controller

The CY3280-20X66 CapSense Controller Kit is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller board
- CY3240-I2USB bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 retractable cable
- CY3280-20x66 Kit CD

Ordering Information

The following table lists the CY8C20336H/CY8C20446H PSoC devices' key package features and ordering codes.

Table 31. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (KB)	SRAM (KB)	CapSense Blocks	Digital I/O Pins	Analog Inputs[27]	XRES Pin	USB
24-pin (4 × 4 × 0.6mm) QFN	CY8C20336H-24LQXI	8	1	1	20	20	Yes	No
32 pin (5 × 5 × 0.6 mm) QFN	CY8C20446H-24LQXI	16	2	1	28	28	Yes	No
48 pin (7 × 7 mm) QFN (OCD)[28]	CY8C20066A-24LTXI	32	2	1	36	36	Yes	Yes

Ordering Code Definitions