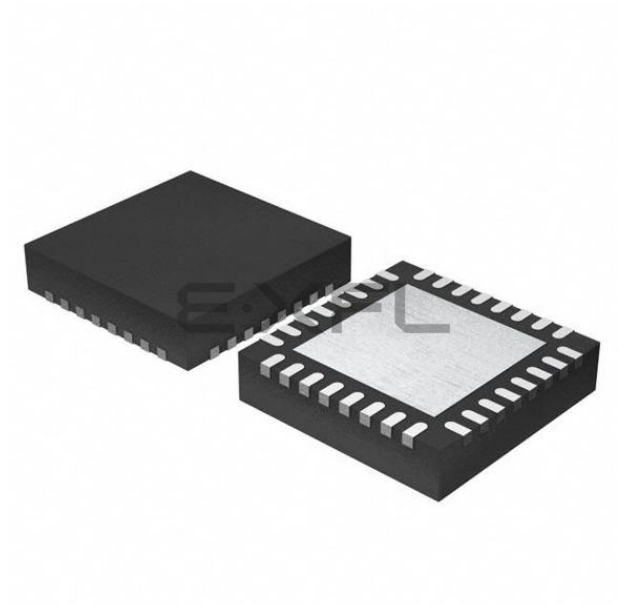

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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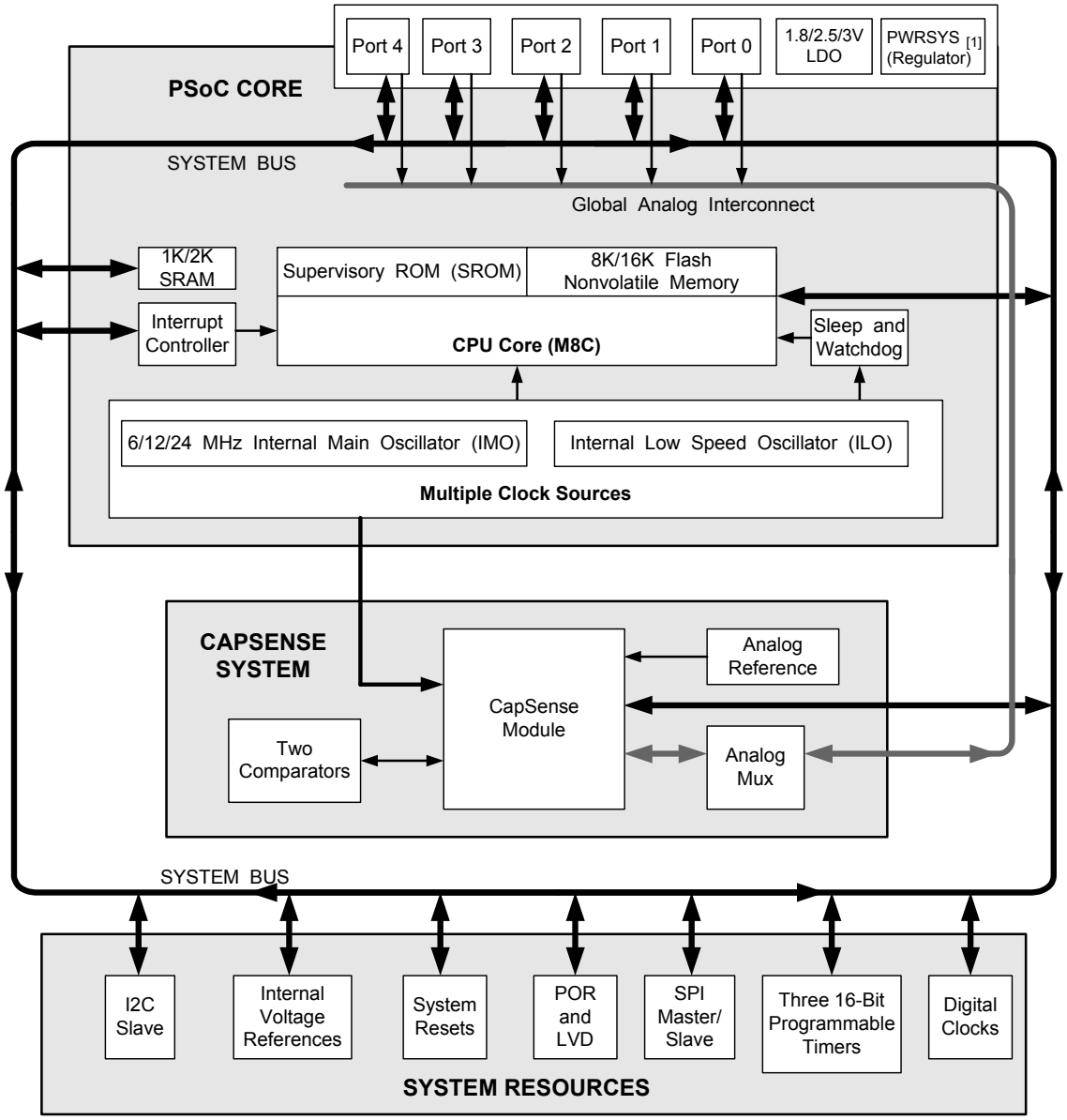
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY8C20xx6A
RAM Size	2K x 8
Interface	I²C, SPI, USB
Number of I/O	28
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20496a-24lqxi

Logic Block Diagram



Note
1. Internal voltage regulator for internal circuitry

Contents

Additional System Resources

System resources provide additional capability, such as configurable USB and I^2C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I^2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I^2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I^2C enhanced slave interface appears as a 32-byte RAM buffer to the external I^2C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note I2C Enhanced Slave Operation - AN56007.
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

For in depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Pinouts

The CY8C20336H/CY8C20446H PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

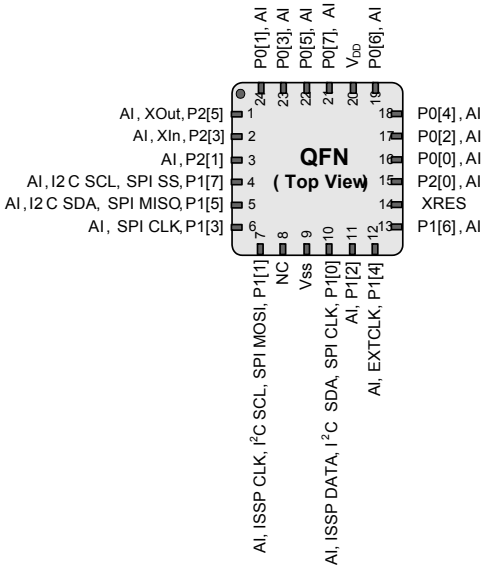
24-Pin QFN

Table 1. Pin Definitions - CY8C20336H [3, 4]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[5], I^2C SCL, SPI MOSI
8			NC	No connection
9	Power		Vss	Ground connection
10	IOHR	I	P1[0]	ISSP DATA[5], I^2C SDA, SPI CLK
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down
15	I/O	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		V_{DD}	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C20336H PSoC Device



Notes
3. During power-up or reset event, device P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter any issues.
4. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
5. These are the ISSP pins, which are not High Z at POR (Power On Reset).

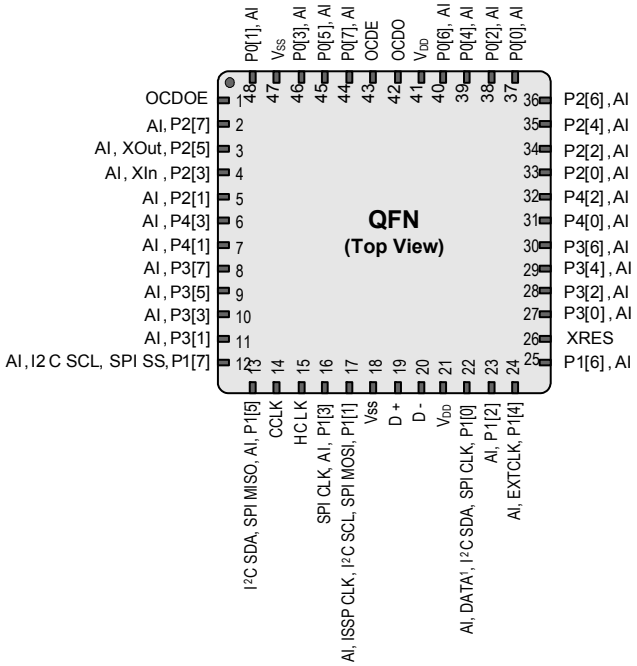
48-Pin QFN OCD

The 48-pin QFN part is for the CY8C20066A On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.[9]

Table 3. Pin Definitions - CY8C20066A PSoC Device [10, 11]

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			CCLK	OCD CPU clock output
15			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK[12], I^2C SCL, SPI MOSI
18	Power		Vss	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[12], I^2C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			OCDO	OCD even data I/O
43			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

Figure 4. CY8C20066A PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

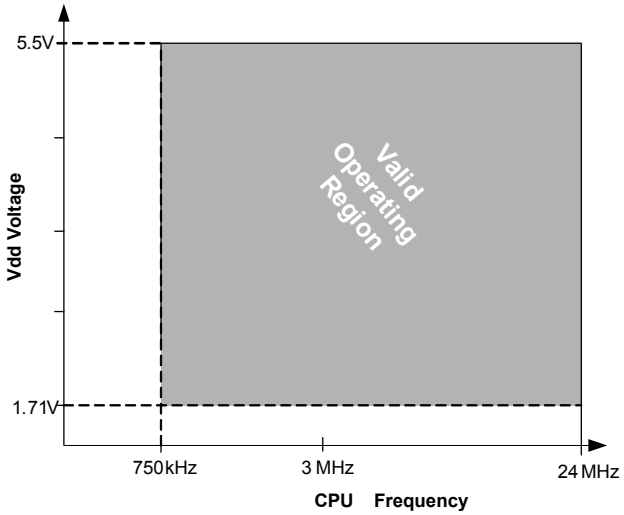
Notes

9. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
10. During power-up or reset event, device P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter any issues.
11. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
12. These are the ISSP pins, which are not High Z at power on reset (POR).

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36H/46H PSoC devices. For the latest electrical specifications, confirm that you have the most recent data sheet by visiting the web at http://www.cypress.com/psoc.

Figure 5. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to V_{SS}		–0.5	–	+6.0	V
V_{IO}	DC input voltage		V_{SS} – 0.5	–	V_{DD} + 0.5	V
V_{IOZ}	DC voltage applied to tristate		V_{SS} –0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin		–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
LU	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature		–40	–	+85	°C
T_C	Commercial temperature range		0	–	70	°C
T_J	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 28. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR0}	1.66 V selected in PSoC Designer	V_{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V_{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	
V_{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	
V_{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	
V_{LVD0}	2.45 V selected in PSoC Designer		2.40	2.45	2.51	V
V_{LVD1}	2.71 V selected in PSoC Designer		2.64[14]	2.71	2.78	
V_{LVD2}	2.92 V selected in PSoC Designer		2.85[15]	2.92	2.99	
V_{LVD3}	3.02 V selected in PSoC Designer		2.95[16]	3.02	3.09	
V_{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V_{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V_{LVD6}	1.80 V selected in PSoC Designer		1.75[17]	1.80	1.84	
V_{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Vdd_{IWRITE}	Supply voltage for flash write operations		1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify		–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See the appropriate DC General Purpose I/O Specifications on page 13	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications on page 13 table on pages 15 or 16	V_{IH}	–	–	V
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	V_{SS} + 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications on page 13 table on page 16. For V_{DD} > 3 V use V_{OH4} in Table 5 on page 11.	V_{OH}	–	V_{DD}	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	50,000	–	–	-
$Flash_{DR}$	Flash data retention	Following maximum flash write cycles; ambient temperature of 55 °C	10	20	–	Years

Notes
14. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
15. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
16. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
17. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{IMO24}	IMO frequency at 24-MHz setting		22.8	24	25.2	MHz
F_{IMO12}	IMO frequency at 12-MHz setting		11.4	12	12.6	MHz
F_{IMO6}	IMO frequency at 6-MHz setting		5.7	6.0	6.3	MHz
F_{CPU}	CPU frequency		0.75	–	25.20	MHz
F_{32K1}	ILO frequency		19	32	50	kHz
F_{32K_U}	ILO untrimmed frequency		13	32	82	kHz
DC_{IMO}	Duty cycle of IMO		40	50	60	%
DC_{ILO}	ILO duty cycle		40	50	60	%
SR_{POWER_UP}	Power supply slew rate	V_{DD} slew rate during power-up	–	–	250	V/ms
T_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
T_{XRST2}	External reset pulse width after power-up[18]	Applies after part has booted	10	–	–	µs

Note
18. The minimum required XRES pulse length is longer when programming the device (see Table 23 on page 21).

AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode port 0, 1	0 0	– –	6 MHz for 1.71 V <V_{DD} < 2.40 V 12 MHz for 2.40 V < V_{DD}< 5.50 V	MHz
T_{RISE23}	Rise time, strong mode, Cload = 50 pF ports 2 or 3	V_{DD} = 3.0 to 3.6 V, 10% – 90%	15	–	80	ns
$T_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, ports 2 or 3	V_{DD} = 1.71 to 3.0 V, 10% – 90%	15	–	80	ns
T_{RISE01}	Rise time, strong mode, Cload = 50 pF ports 0 or 1	V_{DD} = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	–	50	ns
$T_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, ports 0 or 1	V_{DD} = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	10	–	80	ns
T_{FALL}	Fall time, strong mode, Cload = 50 pF all ports	V_{DD} = 3.0 to 3.6 V, 10% – 90%	10	–	50	ns
T_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	V_{DD} = 1.71 to 3.0 V, 10% – 90%	10	–	70	ns

Figure 6. GPIO Timing Diagram

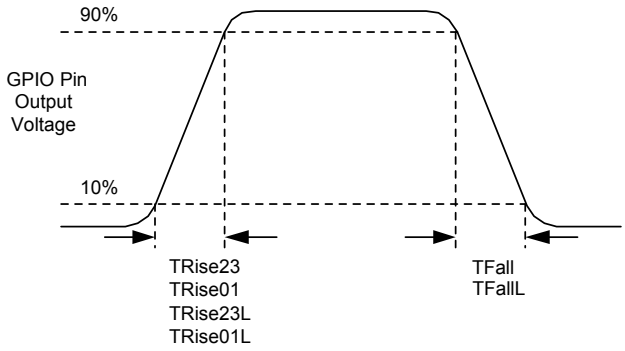


Table 19.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{DRATE}	Full-speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
T_{JR1}	Receiver jitter tolerance	To next transition	–18.5	–	18.5	ns
T_{JR2}	Receiver jitter tolerance	To pair transition	–9	–	9	ns
T_{DJ1}	FS driver jitter	To next transition	–3.5	–	3.5	ns
T_{DJ2}	FS driver jitter	To pair transition	–4.0	–	4.0	ns
T_{FDEOP}	Source jitter for differential transition	To SE0 transition	–2	–	5	ns
T_{FEOPT}	Source SE0 interval of EOP		160	–	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP		82	–		ns
T_{FST}	Width of SE0 interval during differential transition		–	–	14	ns

Table 20. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{FR}	Transition rise time	50 pF	4	–	20	ns
T_{FF}	Transition fall time	50 pF	4	–	20	ns
T_{FRFM}[19]	Rise/fall time matching		90	–	111	%
Vcrs	Output signal crossover voltage		1.30	–	2.00	V

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 21. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

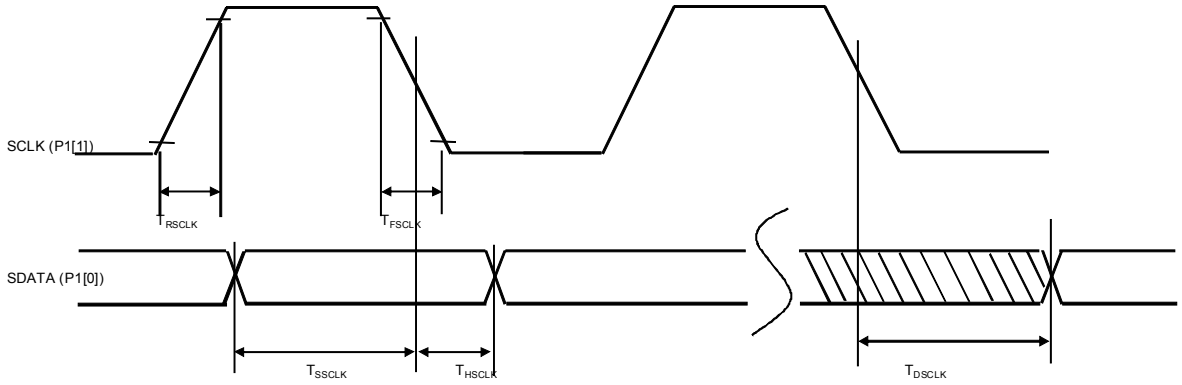
Table 22. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency (external oscillator frequency)		0.75	–	25.20	MHz
	High period		20.60	–	5300	ns
	Low period		20.60	–	–	ns
	Power-up IMO to switch		150	–	–	µs

Note
19. T_{FRFM} is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.

AC Programming Specifications

Figure 7. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK		1	–	20	ns
T_{FSCLK}	Fall time of SCLK		1	–	20	ns
T_{SSCLK}	Data Setup time to falling edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold time from falling edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash erase time (Block)		–	–	18	ms
T_{WRITE}	Flash block write time		–	–	25	ms
T_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
T_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \le V_{DD} \le 3.6$	–	–	85	ns
T_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \le V_{DD} \le 3.0$	–	–	130	ns
T_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	µs
T_{XRES}	XRES Pulse Length		300	–	–	µs
$T_{VDDWAIT}$	V_{DD} stable to wait-and-poll hold off		0.1	–	1	ms
$T_{VDDXRES}$	V_{DD} stable to XRES assertion delay		14.27	–	–	ms
T_{POLL}	SDATA high pulse time		0.01	–	200	ms
T_{ACQ}	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.		3.20	–	19.60	ms
$T_{XRESINI}$	“Key window” time after an XRES event, based on eight ILO clocks		98	–	615	µs

Table 25. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	– –	– –	6 3	MHz
DC	SCLK duty cycle		–	50	–	%
T_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	60 100	– –	– –	ns
T_{HOLD}	SCLK to MISO hold time		40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
T_{OUT_H}	MOSI high time		40	–	–	ns

Figure 9. SPI Master Mode 0 and 2

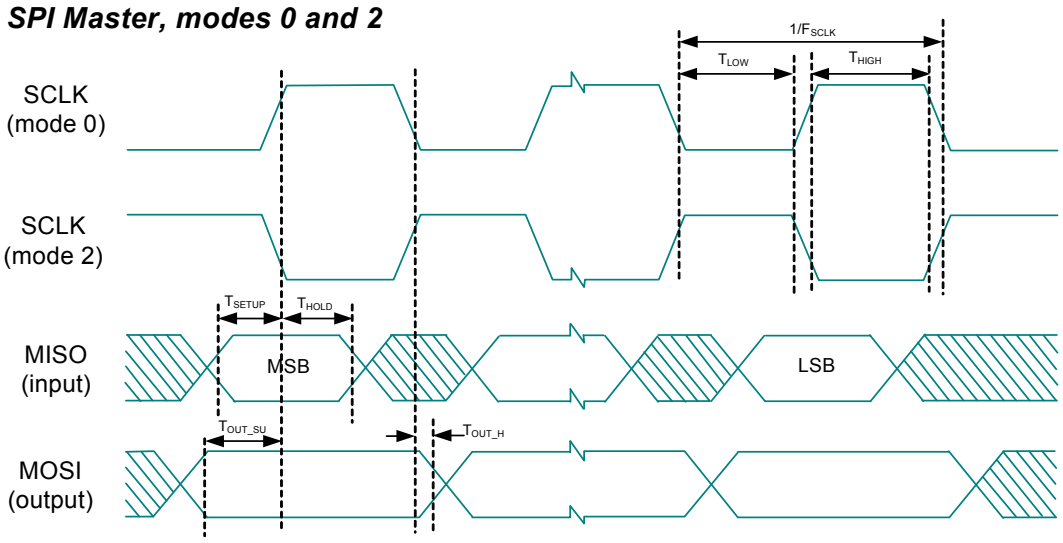


Figure 11. SPI Slave Mode 0 and 2

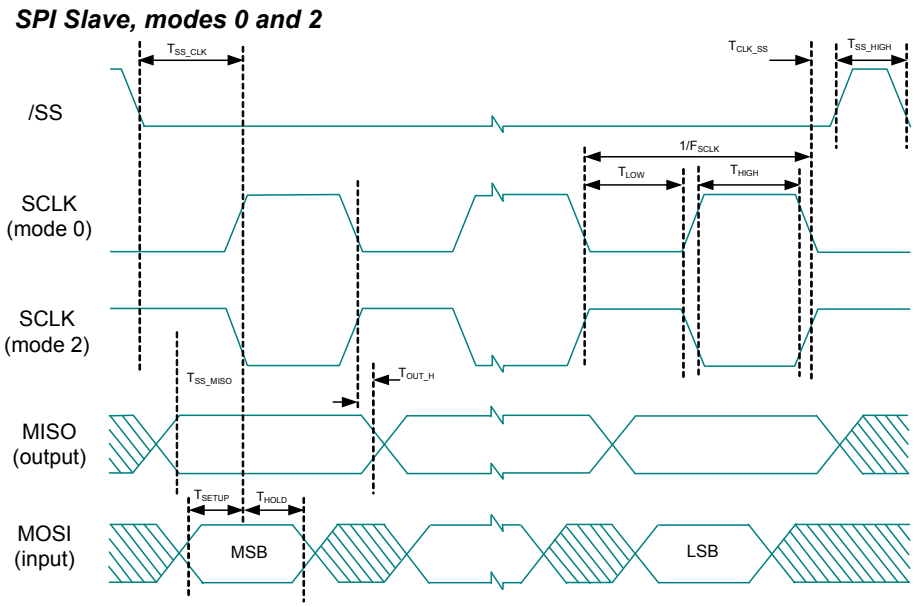
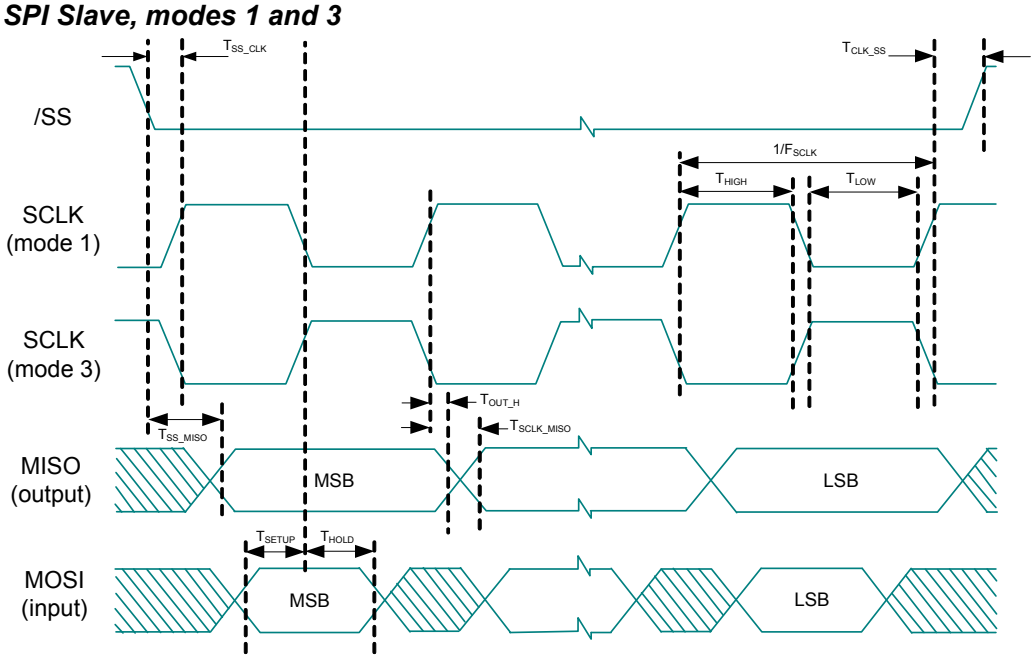


Figure 12. SPI Slave Mode 1 and 3

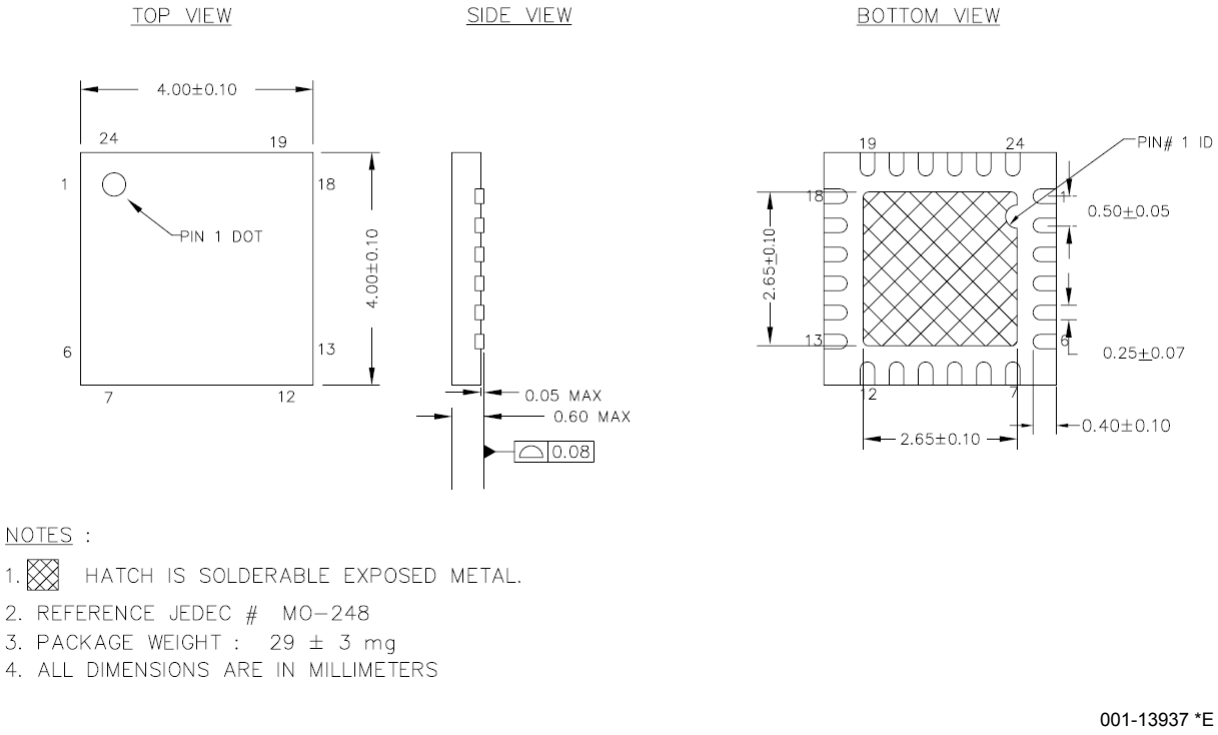


Packaging Information

This section illustrates the packaging specifications for the CY8C20336H/CY8C20446H PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

Figure 13. 24-Pin (4 × 4 × 0.55 mm) QFN



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *E

Thermal Impedances

Table 27. Thermal Impedances per Package

Package	Typical θ_{JA} [21]
24-QFN[22]	20.90 °C/W
32-QFN[22]	19.51 °C/W
48-QFN[22]	17.68 °C/W

Capacitance on Crystal Pins

Table 28. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
24-pin QFN	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

Notes
21. $T_J = T_A$ + Power x θ_{JA}.
22. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.
23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240-V power supply, Euro-Plug adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466A-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3280-20x66 Universal CapSense Controller

The CY3280-20X66 CapSense Controller Kit is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller board
- CY3240-I2USB bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 retractable cable
- CY3280-20x66 Kit CD

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 30. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit[24]	Foot Kit[25]	Adapter[26]
CY8C20336H-24LQXI	24-pin QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 24
CY8C20446H-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 26

Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/?rID2748.

Notes

24. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
25. Foot kit includes surface mount feet that can be soldered to the target PCB.
26. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.
27. Dual-function digital I/O pins also connect to the common analog mux.
28. This part is available in limited quantities for in-circuit debugging during prototype development. It is not available in production volumes.

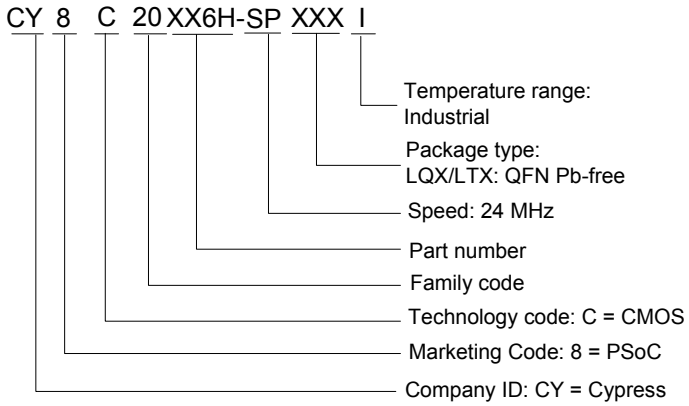
Ordering Information

The following table lists the CY8C20336H/CY8C20446H PSoC devices' key package features and ordering codes.

Table 31. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (KB)	SRAM (KB)	CapSense Blocks	Digital I/O Pins	Analog Inputs[27]	XRES Pin	USB
24-pin (4 × 4 × 0.6mm) QFN	CY8C20336H-24LQXI	8	1	1	20	20	Yes	No
32 pin (5 × 5 × 0.6 mm) QFN	CY8C20446H-24LQXI	16	2	1	28	28	Yes	No
48 pin (7 × 7 mm) QFN (OCD)[28]	CY8C20066A-24LTXI	32	2	1	36	36	Yes	Yes

Ordering Code Definitions



Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
EOP	end of packet
FSR	full scale range
GPIO	general purpose input/output
GUI	graphical user interface
I^2C	inter-integrated circuit
ICE	in-circuit emulator
IDAC	digital analog converter current
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	mega instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debugger
POR	power on reset
PPOR	precision power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC®	Programmable System-on-Chip
SLIMO	slow internal main oscillator
SRAM	static random access memory
SNR	signal to noise ratio
QFN	quad flat no-lead
SCL	serial I^2C clock
SDA	serial I^2C data
SDATA	serial ISSP data
SPI	serial peripheral interface
SS	slave select
SSOP	shrink small outline package
TC	test controller
USB	universal serial bus
USB D+	USB Data +
USB D-	USB Data-
WLCSP	wafer level chip scale package
XTAL	crystal

Units of Measure

Table 32 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Table 32. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
g	gram
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
KHz	kilohertz
Ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
Ω	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
s	sigma: one standard deviation
V	volts
W	watt