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[Embedded - Microcontrollers - Application Specific](#) represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

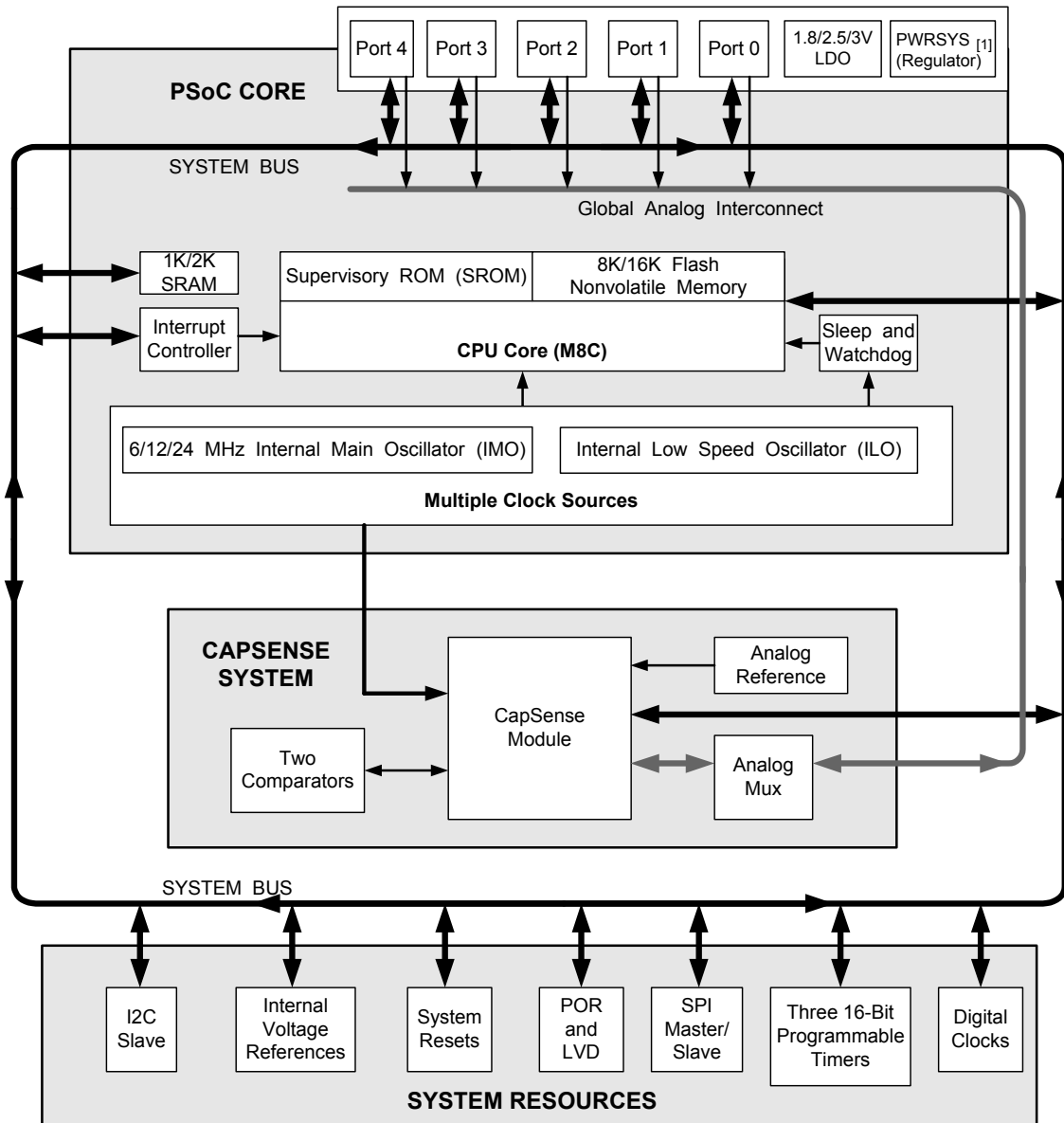
What Are [Embedded - Microcontrollers - Application Specific](#)?

Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (8kB)
Controller Series	CY8C20xx6A
RAM Size	1K x 8
Interface	I ² C, SPI
Number of I/O	36
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20536a-24pvxit

Logic Block Diagram



Note

1. Internal voltage regulator for internal circuitry

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Additional System Resources

System resources provide additional capability, such as configurable USB and I²C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I²C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I²C enhanced slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note [I2C Enhanced Slave Operation - AN56007](#).
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

For in depth information, along with detailed programming details, see the PSoC® [Technical Reference Manual](#).

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

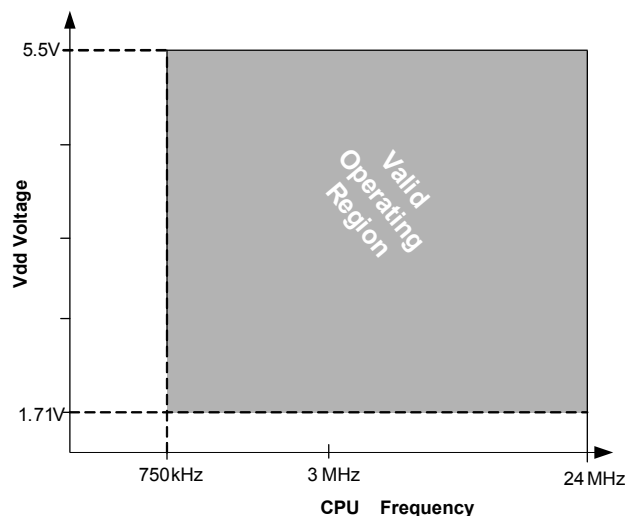
A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36H/46H PSoC devices. For the latest electrical specifications, confirm that you have the most recent data sheet by visiting the web at <http://www.cypress.com/psoc>.

Figure 5. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	+25	+125	°C
V _{DD}	Supply voltage relative to V _{SS}		-0.5	-	+6.0	V
V _{IO}	DC input voltage		V _{SS} - 0.5	-	V _{DD} + 0.5	V
V _{IOZ}	DC voltage applied to tristate		V _{SS} - 0.5	-	V _{DD} + 0.5	V
I _{MIO}	Maximum current into any port pin		-25	-	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	-	-	V
LU	Latch up current	In accordance with JESD78 standard	-	-	200	mA

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T _A	Ambient temperature		-40	-	+85	°C
T _C	Commercial temperature range		0	-	70	°C
T _J	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 28 . The user must limit the power consumption to comply with this requirement.	-40	-	+100	°C

DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 7. 3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.60	8	$k\Omega$
V_{OH1}	High output voltage port 2 or 3 pins	$I_{OH} \leq 10 \mu\text{A}$, maximum of 10 mA source current in all I/Os	$V_{DD} - 0.20$	–	–	V
V_{OH2}	High output voltage port 2 or 3 pins	$I_{OH} = 1 \text{ mA}$, maximum of 20 mA source current in all I/Os	$V_{DD} - 0.90$	–	–	V
V_{OH3}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	$I_{OH} < 10 \mu\text{A}$, maximum of 10 mA source current in all I/Os	$V_{DD} - 0.20$	–	–	V
V_{OH4}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	$I_{OH} = 5 \text{ mA}$, maximum of 20 mA source current in all I/Os	$V_{DD} - 0.90$	–	–	V
V_{OH5}	High output voltage port 1 pins with LDO regulator enabled for 3 V out	$I_{OH} < 10 \mu\text{A}$, $V_{DD} > 3.1 \text{ V}$, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V_{OH6}	High output voltage port 1 pins with LDO regulator enabled for 3 V out	$I_{OH} = 5 \text{ mA}$, $V_{DD} > 3.1 \text{ V}$, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage port 1 pins with LDO enabled for 2.5 V out	$I_{OH} < 10 \mu\text{A}$, $V_{DD} > 2.7 \text{ V}$, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage port 1 pins with LDO enabled for 2.5 V out	$I_{OH} = 2 \text{ mA}$, $V_{DD} > 2.7 \text{ V}$, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage port 1 pins with LDO enabled for 1.8 V out	$I_{OH} < 10 \mu\text{A}$, $V_{DD} > 2.7 \text{ V}$, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V_{OH10}	High output voltage port 1 pins with LDO enabled for 1.8 V out	$I_{OH} = 1 \text{ mA}$, $V_{DD} > 2.7 \text{ V}$, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	$I_{OL} = 25 \text{ mA}$, $V_{DD} > 3.3 \text{ V}$, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.80	V
V_{IH}	Input high voltage		2.00	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	0.001	1	μA
C_{PIN}	Pin capacitance	Package and pin dependent Temp = 25°C	0.50	1.70	7	pF

Table 8. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull-up resistor		4	5.60	8	kΩ
V _{OH1}	High output voltage port 2 or 3 pins	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	–	–	V
V _{OH2}	High output voltage port 2 or 3 pins	I _{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.40	–	–	V
V _{OH3}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	–	–	V
V _{OH4}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.50	–	–	V
V _{OH5A}	High output voltage port 1 pins with LDO enabled for 1.8 V out	I _{OH} < 10 μA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V _{OH6A}	High output voltage port 1 pins with LDO enabled for 1.8 V out	I _{OH} = 1 mA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V _{OL}	Low output voltage	I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V _{IL}	Input low voltage		–	–	0.72	V
V _{IH}	Input high voltage		1.40	–	–	V
V _H	Input hysteresis voltage		–	80	–	mV
I _{IL}	Input leakage (absolute value)		–	1	1000	nA
C _{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

Table 9. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull-up resistor		4	5.60	8	kΩ
V _{OH1}	High output voltage port 2 or 3 pins	I _{OH} = 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	–	–	V
V _{OH2}	High output voltage port 2 or 3 pins	I _{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.50	–	–	V
V _{OH3}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I _{OH} = 100 μA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	–	–	V
V _{OH4}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.50	–	–	V
V _{OL}	Low output voltage	I _{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V _{IL}	Input low voltage		–	–	0.30 × V _{DD}	V
V _{IH}	Input high voltage		0.65 × V _{DD}	–	–	V

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{POR0}	1.66 V selected in PSoC Designer	V _{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V _{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	
V _{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	
V _{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	
V _{LVD0}	2.45 V selected in PSoC Designer		2.40	2.45	2.51	V
V _{LVD1}	2.71 V selected in PSoC Designer		2.64 ^[14]	2.71	2.78	
V _{LVD2}	2.92 V selected in PSoC Designer		2.85 ^[15]	2.92	2.99	
V _{LVD3}	3.02 V selected in PSoC Designer		2.95 ^[16]	3.02	3.09	
V _{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V _{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V _{LVD6}	1.80 V selected in PSoC Designer		1.75 ^[17]	1.80	1.84	
V _{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{DDIWRITE}	Supply voltage for flash write operations		1.71	–	5.25	V
I _{DDP}	Supply current during programming or verify		–	5	25	mA
V _{ILP}	Input low voltage during programming or verify	See the appropriate DC General Purpose I/O Specifications on page 13	–	–	V _{IL}	V
V _{IHP}	Input high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications on page 13 table on pages 15 or 16	V _{IH}	–	–	V
I _{ILP}	Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I _{IHP}	Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V _{OLP}	Output low voltage during programming or verify		–	–	V _{SS} + 0.75	V
V _{OHP}	Output high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications on page 13 table on page 16. For V _{DD} > 3 V use V _{OH4} in Table 5 on page 11 .	V _{OH}	–	V _{DD}	V
Flash _{ENPB}	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
Flash _{DR}	Flash data retention	Following maximum flash write cycles; ambient temperature of 55 °C	10	20	–	Years

Notes

14. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
15. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
16. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
17. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{IMO24}	IMO frequency at 24-MHz setting		22.8	24	25.2	MHz
F _{IMO12}	IMO frequency at 12-MHz setting		11.4	12	12.6	MHz
F _{IMO6}	IMO frequency at 6-MHz setting		5.7	6.0	6.3	MHz
F _{CPU}	CPU frequency		0.75	–	25.20	MHz
F _{32K1}	ILO frequency		19	32	50	kHz
F _{32K_U}	ILO untrimmed frequency		13	32	82	kHz
DC _{IMO}	Duty cycle of IMO		40	50	60	%
DC _{ILO}	ILO duty cycle		40	50	60	%
SR _{POWER_UP}	Power supply slew rate	V _{DD} slew rate during power-up	–	–	250	V/ms
T _{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
T _{XRST2}	External reset pulse width after power-up ^[18]	Applies after part has booted	10	–	–	μs

Note

18. The minimum required XRES pulse length is longer when programming the device (see [Table 23 on page 21](#)).

AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode port 0, 1	0	–	6 MHz for 1.71 V < V_{DD} < 2.40 V 12 MHz for 2.40 V < V_{DD} < 5.50 V	MHz
T_{RISE23}	Rise time, strong mode, Cload = 50 pF ports 2 or 3	V_{DD} = 3.0 to 3.6 V, 10% – 90%	15	–	80	ns
$T_{RISE23L}$	Rise time, strong mode low supply, Clload = 50 pF, ports 2 or 3	V_{DD} = 1.71 to 3.0 V, 10% – 90%	15	–	80	ns
T_{RISE01}	Rise time, strong mode, Clload = 50 pF ports 0 or 1	V_{DD} = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	–	50	ns
$T_{RISE01L}$	Rise time, strong mode low supply, Clload = 50 pF, ports 0 or 1	V_{DD} = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	10	–	80	ns
T_{FALL}	Fall time, strong mode, Clload = 50 pF all ports	V_{DD} = 3.0 to 3.6 V, 10% – 90%	10	–	50	ns
T_{FALLL}	Fall time, strong mode low supply, Clload = 50 pF, all ports	V_{DD} = 1.71 to 3.0 V, 10% – 90%	10	–	70	ns

Figure 6. GPIO Timing Diagram

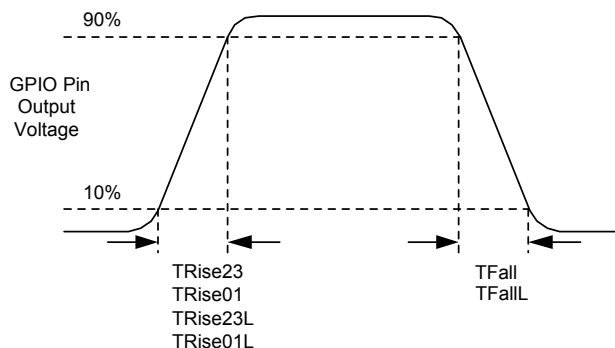


Table 19. AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{DRATE}	Full-speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
T _{JR1}	Receiver jitter tolerance	To next transition	–18.5	–	18.5	ns
T _{JR2}	Receiver jitter tolerance	To pair transition	–9	–	9	ns
T _{DJ1}	FS driver jitter	To next transition	–3.5	–	3.5	ns
T _{DJ2}	FS driver jitter	To pair transition	–4.0	–	4.0	ns
T _{FDEOP}	Source jitter for differential transition	To SE0 transition	–2	–	5	ns
T _{FEOPT}	Source SE0 interval of EOP		160	–	175	ns
T _{FEOPR}	Receiver SE0 interval of EOP		82	–		ns
T _{FST}	Width of SE0 interval during differential transition		–	–	14	ns

Table 20. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{FR}	Transition rise time	50 pF	4	–	20	ns
T _{FF}	Transition fall time	50 pF	4	–	20	ns
T _{FRFM} ^[19]	Rise/fall time matching		90	–	111	%
V _{crs}	Output signal crossover voltage		1.30	–	2.00	V

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 21. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{OSCEXT}	Frequency (external oscillator frequency)		0.75	–	25.20	MHz
	High period		20.60	–	5300	ns
	Low period		20.60	–	–	ns
	Power-up IMO to switch		150	–	–	μs

Note

19. T_{FRFM} is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.

Table 25. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	— —	— —	6 3	MHz
DC	SCLK duty cycle		—	50	—	%
T_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	60 100	— —	— —	ns
T_{HOLD}	SCLK to MISO hold time		40	—	—	ns
T_{OUT_VAL}	SCLK to MOSI valid time		—	—	40	ns
T_{OUT_H}	MOSI high time		40	—	—	ns

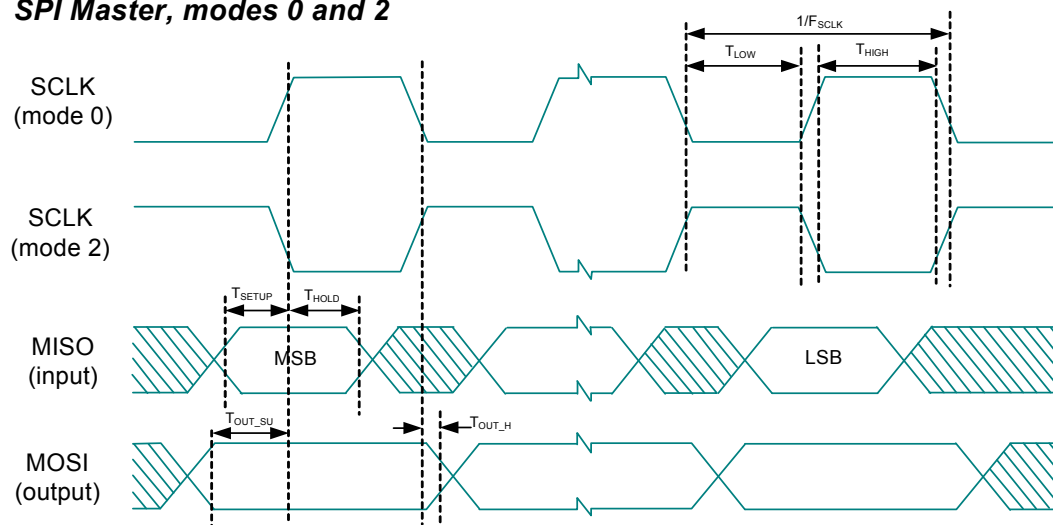
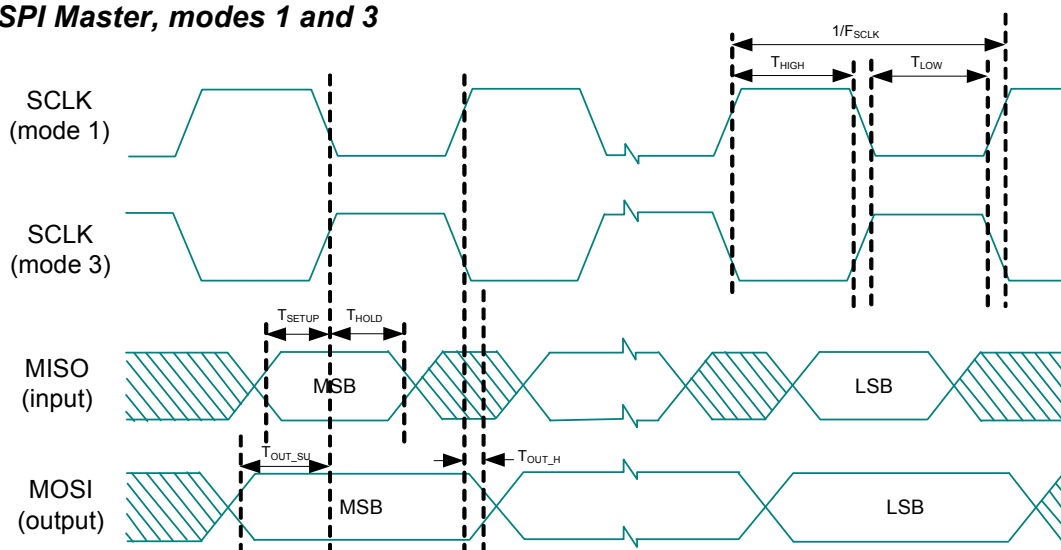
Figure 9. SPI Master Mode 0 and 2
SPI Master, modes 0 and 2


Figure 10. SPI Master Mode 1 and 3
SPI Master, modes 1 and 3

Table 26. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	—	—	—	4	MHz
T_{LOW}	SCLK low time	—	42	—	—	ns
T_{HIGH}	SCLK high time	—	42	—	—	ns
T_{SETUP}	MOSI to SCLK setup time	—	30	—	—	ns
T_{HOLD}	SCLK to MOSI hold time	—	50	—	—	ns
T_{SS_MISO}	SS high to MISO valid	—	—	—	153	ns
T_{SCLK_MISO}	SCLK to MISO valid	—	—	—	125	ns
T_{SS_HIGH}	SS high time	—	50	—	—	ns
T_{SS_CLK}	Time from SS low to first SCLK	—	2/SCLK	—	—	ns
T_{CLK_SS}	Time from last SCLK to SS high	—	2/SCLK	—	—	ns

Thermal Impedances

Table 27. Thermal Impedances per Package

Package	Typical θ_{JA} ^[21]
24-QFN ^[22]	20.90 °C/W
32-QFN ^[22]	19.51 °C/W
48-QFN ^[22]	17.68 °C/W

Capacitance on Crystal Pins

Table 28. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
24-pin QFN	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

Notes

21. $T_J = T_A + \text{Power} \times \theta_{JA}$.

22. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at <http://www.cypress.com>.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at <http://www.cypress.com>.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The **CY3215-DK** is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240-V power supply, Euro-Plug adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466A-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The **CY3210-MiniProg1** kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The **CY3210-PSoCEval1** kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3280-20x66 Universal CapSense Controller

The **CY3280-20X66 CapSense Controller Kit** is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller board
- CY3240-I2USB bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 retractable cable
- CY3280-20x66 Kit CD

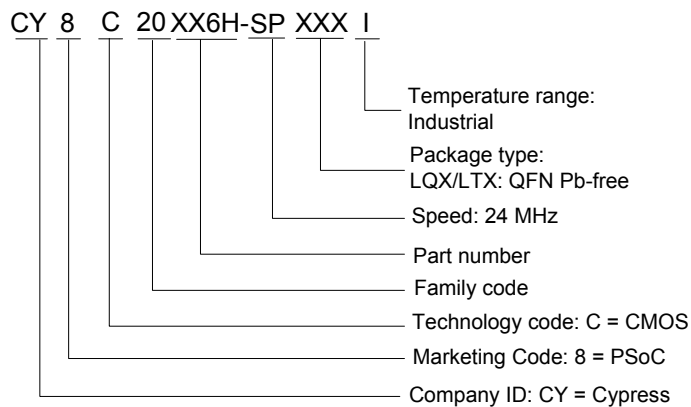
Ordering Information

The following table lists the CY8C20336H/CY8C20446H PSoC devices' key package features and ordering codes.

Table 31. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (KB)	SRAM (KB)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[27]	XRES Pin	USB
24-pin (4 × 4 × 0.6mm) QFN	CY8C20336H-24LQXI	8	1	1	20	20	Yes	No
32 pin (5 × 5 × 0.6 mm) QFN	CY8C20446H-24LQXI	16	2	1	28	28	Yes	No
48 pin (7 × 7 mm) QFN (OCD) ^[28]	CY8C20066A-24LTXI	32	2	1	36	36	Yes	Yes

Ordering Code Definitions



Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
EOP	end of packet
FSR	full scale range
GPIO	general purpose input/output
GUI	graphical user interface
I ² C	inter-integrated circuit
ICE	in-circuit emulator
IDAC	digital analog converter current
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	mega instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debugger
POR	power on reset
PPOR	precision power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC®	Programmable System-on-Chip
SLIMO	slow internal main oscillator
SRAM	static random access memory
SNR	signal to noise ratio
QFN	quad flat no-lead
SCL	serial I ² C clock
SDA	serial I ² C data
SDATA	serial ISSP data
SPI	serial peripheral interface
SS	slave select
SSOP	shrink small outline package
TC	test controller
USB	universal serial bus
USB D+	USB Data +
USB D-	USB Data-
WLCSP	wafer level chip scale package
XTAL	crystal

Units of Measure

Table 32 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Table 32. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
g	gram
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
KHz	kilohertz
Ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
Ω	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
s	sigma: one standard deviation
V	volts
W	watt

Glossary

Crosspoint connection	Connection between any GPIO combination via analog multiplexer bus.
Differential non-linearity	Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.
Hold time	Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.
I²C	It is a serial multi-master bus used to connect low speed peripherals to MCU.
Integral nonlinearity	It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level.
Latch up current	Current at which the latch up test is conducted according to JESD78 standard (at 125 °C)
Power supply rejection ratio (PSRR)	The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device.
Scan	The conversion of all sensor capacitances to digital values.
Setup time	Period required to prepare a device, machine, process, or system for it to be ready to function.
Signal-to-noise ratio	The ratio between a capacitive finger signal and system noise.
SPI	Serial peripheral interface is a synchronous serial data link standard.

Reference Documents

- Technical reference manual for [CY8C20xx6](#) devices
- In-system Serial Programming (ISSP) protocol for 20xx6 – [AN2026C](#)
- Host Sourced Serial Programming for 20xx6 devices – [AN59389](#)

Document History Page

Document Title: CY8C20336H/CY8C20446H Haptics Enabled CapSense® Controller Document Number: 001-56223				
Revision	ECN	Origin of Change	Submission Date	Description of Change
**	2787411	VZD/AESA	10/15/2009	New datasheet.
*A	3016550	KEJO/KPOL	08/26/2010	Added CY8C20346H part. Updated 24-pin QFN and 32-pin QFN package diagrams. Content and format updated to match latest template.
*B	3089844	JPM	11/18/10	In Table 26 , modified T_{LOW} and T_{HIGH} min values to 42. Updated T_{SS_HIGH} min value to 50; removed max value.
*C	3180479	YVA	02/23/11	Removed CY8C20346H part Changed title from CapSense Applications to Haptics Enabled CapSense Controller Updated Table 29 with Time at Maximum Temperature information
*D	3638625	YLIU/BVI	06/06/2012	Updated F_{SCLK} parameter in the SPI Slave AC Specifications table Updated Getting Started and Designing with PSoC Designer sections. Included Development Tools . Updated Software under Development Tool Selection section. Updated F_{SCLK} parameter in the Table 26 , "SPI Slave AC Specifications," on page 24. Changed t_{OUT_HIGH} to t_{OUT_H} in Table 25 , "SPI Master AC Specifications," on page 23 Updated package diagrams: 001-13937 to *D 001-13191 to *F
*E	3822568	DST	11/27/2012	Updated package diagrams: 001-13937 to *E 001-42168 to *E 001-13191 to *G