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What Are <u>Embedded - Microcontrollers -</u> <u>Application Specific</u>?

Application charific microcontrollars are analyzared to

Details

Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (32kB)
Controller Series	CY8C20xx6A
RAM Size	2K x 8
Interface	I ² C, SPI
Number of I/O	36
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20566a-24pvxit

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Logic Block Diagram





CY8C20336H, CY8C20446H

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PSoC[®] Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low-cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The core
- CapSense analog system
- System resources (including a full-speed USB port).

A common, versatile bus allows connection between the I/O and the analog system.

Each CY8C20336H/446H PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1-V or 1.2-V analog reference, which together support capacitive sensing of up to 28 inputs^[2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

SmartSense™

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easyto-use and provides a robust noise immunity. It is the only autotuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.



Figure 1. CapSense System Block Diagram

Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Haptics TS2000 Controller

The CY8C20336H/CY8C20446H family of devices feature an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

Note 2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I^2C + 1 pin for modulator capacitor.





Additional System Resources

System resources provide additional capability, such as configurable USB and I²C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I²C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I²C enhanced slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note I2C Enhanced Slave Operation AN56007.
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced poweron-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

For in depth information, along with detailed programming details, see the $PSoC^{\mathbb{R}}$ Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.



Pinouts

The CY8C20336H/CY8C20446H PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

24-Pin QFN

Table 1. Pin Definitions - CY8C20336H ^[3, 4]

Pin	Ту	pe	Namo	Description
No.	Digital	Analog	Maine	Description
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I ² C SCL, SPI SS
5	IOHR	I	P1[5]	I ² C SDA, SPI MISO
6	IOHR	Ι	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK ^[5] , I ² C SCL, SPI MOSI
8			NC	No connection
9	Po	wer	Vss	Ground connection
10	IOHR	I	P1[0]	ISSP DATA ^[5] , I ² C SDA, SPI CLK
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	In	put	XRES	Active high external reset with internal pull down
15	I/O	Ι	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Po	wer	V _{DD}	Supply voltage
21	IOH	Ι	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V _{SS}	Center pad must be connected to ground

Figure 2. CY8C20336H PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

- During power-up or reset event, device P1[1] and P1[0] may disturb the l²C bus. Use alternate pins if you encounter any issues.
 The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
 These are the ISSP pins, which are not High Z at POR (Power On Reset).



32-Pin QFN

Table 2. Pin Definitions - CY8C20446H PSoC Device [6, 7]

Pin	Pin Type Name Description		Description	
No.	Digital	Analog	Name	Description
1	IOH		P0[1]	Integrating input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I ² C SCL, SPI SS
9	IOHR	I	P1[5]	I ² C SDA, SPI MISO
10	IOHR	l	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK ^[8] , I ² C SCL, SPI MOSI.
12	Po	wer	Vss	Ground connection.
13	IOHR	l	P1[0]	ISSP DATA ^[8] , I ² C SDA., SPI CLK
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	In	put	XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	- 1	P0[0]	
25	IOH	l	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Po	wer	V _{DD}	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input
32	Po	wer	V _{SS}	Ground connection
CP	Power		V_{SS}	Center pad must be connected to ground

Figure 3. CY8C20446H PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

- Buring power-up or reset event, device P1[1] and P1[0] may disturb the l²C bus. Use alternate pins if you encounter any issues.
 The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
 These are the ISSP pins, which are not High Z at POR (Power On Reset).



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36H/46H PSoC devices. For the latest electrical specifications, confirm that you have the most recent data sheet by visiting the web at http://www.cypress.com/psoc.



Figure 5. Voltage versus CPU Frequency

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Тур	Max	Units
T _{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	+25	+125	ů
V _{DD}	Supply voltage relative to V_{SS}		-0.5	-	+6.0	V
V _{IO}	DC input voltage		$V_{SS} - 0.5$	-	V _{DD} + 0.5	V
V _{IOZ}	DC voltage applied to tristate		V _{SS} –0.5	-	V _{DD} + 0.5	V
I _{MIO}	Maximum current into any port pin		-25	-	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	-	-	V
LU	Latch up current	In accordance with JESD78 standard	_	_	200	mA

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Тур	Max	Units
T _A	Ambient temperature		-40	-	+85	°C
T _C	Commercial temperature range		0	-	70	°C
TJ	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 28. The user must limit the power consumption to comply with this requirement.	-40	-	+100	°C





DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
V _{DD} ^[13]	Supply voltage	Refer the table DC POR and LVD Specifications on page 17	1.71	-	5.50	V
I _{DD24}	Supply current, IMO = 24 MHz	Conditions are V _{DD} \leq 3.0 V, T _A = 25 °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	-	3.32	4.00	mA
I _{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \le 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	-	1.86	2.60	mA
I _{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \le 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	-	1.13	1.80	mA
I _{SB0}	Deep sleep current	$V_{DD}{\leq}3.0$ V, T_{A} = 25 °C, I/O regulator turned off	_	0.10	0.50	μA
I _{SB1}	Standby current with POR, LVD, and sleep timer	$V_{DD}{\leq}3.0$ V, T_{A} = 25 °C, I/O regulator turned off	_	1.07	1.50	μA

Note

13. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 usec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.



Table 8. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
R _{PU}	Pull-up resistor		4	5.60	8	kΩ
V _{OH1}	High output voltage port 2 or 3 pins	I_{OH} < 10 μ A, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	_	_	V
V _{OH2}	High output voltage port 2 or 3 pins	I _{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.40	Ι	-	V
V _{OH3}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} < 10 μ A, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	-	-	V
V _{OH4}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.50	_	-	V
V _{OH5A}	High output voltage port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 μ A, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V _{OH6A}	High output voltage port 1 pins with LDO enabled for 1.8 V out	I _{OH} = 1 mA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	_	-	V
V _{OL}	Low output voltage	I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	-	-	0.75	V
V _{IL}	Input low voltage		-	-	0.72	V
V _{IH}	Input high voltage		1.40	_	_	V
V _H	Input hysteresis voltage		_	80	_	mV
IIL	Input leakage (absolute value)		_	1	1000	nA
C _{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

Table 9. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
R _{PU}	Pull-up resistor		4	5.60	8	kΩ
V _{OH1}	High output voltage port 2 or 3 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	_	-	V
V _{OH2}	High output voltage port 2 or 3 pins	I _{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.50	-	-	V
V _{OH3}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I _{OH} = 100 μA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	-	-	V
V _{OH4}	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.50	-	-	V
V _{OL}	Low output voltage	I _{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	_	-	0.40	V
V _{IL}	Input low voltage		-	-	$0.30 \times V_{DD}$	V
V _{IH}	Input high voltage		$0.65 \times V_{DD}$	-	-	V



Table 9. 1.71 V to 2.4 V DC GPIO Specifications (continued)

Symbol	Description	Conditions	Min	Тур	Max	Units
V _H	Input hysteresis voltage		-	80	-	mV
IIL	Input leakage (absolute value)		-	1	1000	nA
C _{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

Table 10.DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Тур	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	900	-	1575	Ω
Rusba	USB D+ pull-up resistance	While receiving traffic	1425	-	3090	Ω
Vohusb	Static output high		2.8	-	3.6	V
Volusb	Static output low		-	-	0.3	V
Vdi	Differential input sensitivity		0.2	-	-	V
Vcm	Differential input common mode range		0.8	-	2.5	V
Vse	Single-ended receiver threshold		0.8	-	2.0	V
Cin	Transceiver capacitance		-	-	50	pF
lio	High-Z state data line leakage	On D+ or D- line	-10	-	+10	μA
Rps2	PS/2 pull-up resistance		3000	5000	7000	Ω
Rext	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
R _{SW}	Switch resistance to common analog bus		-	-	800	Ω
R _{GND}	Resistance of initialization switch to V_{SS}		_	-	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. DC Comparator Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
V _{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V _{DD}	0.0	-	1.8	V
I _{LPC}	LPC supply current		-	10	40	μΑ
V _{OSLPC}	LPC voltage offset		_	2.5	30	mV



Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C \leq TA \leq 85 °C, 1.71 V \leq V_{DD} \leq 5.5 V.

Table 13. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
T _{COMP}	Comparator response time	50-mV overdrive	_	70	100	ns
Offset		Valid from 0.2 V to V_{DD} – 0.2 V	_	2.5	30	mV
Current		Average DC current, 50 mV overdrive	_	20	80	μA
DSDD	Supply voltage > 2 V	Power supply rejection ratio	_	80	-	dB
	Supply voltage < 2 V	Power supply rejection ratio	_	40	-	dB
Input Range			0	-	1.5	V

ADC Electrical Specifications

Table 14.ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
Input						
V _{IN}	Input voltage range		0	-	VREFADC	V
C _{IIN}	Input capacitance		-	-	5	pF
R _{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference	·					
V _{REFADC}	ADC reference voltage		1.14	-	1.26	V
Conversion Rate						
F _{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications on page 18 for accuracy	2.25	-	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data clock)	-	23.43	_	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data clock)	-	5.85	_	ksps
DC Accuracy			1	1		
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	-	10	bits
DNL	Differential nonlinearity		–1	-	+2	LSB
INL	Integral nonlinearity		-2	_	+2	LSB
E _{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E _{GAIN}	Gain error	For any resolution	-5	-	+5	%FSR
Power		·				
I _{ADC}	Operating current		-	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (V _{DD} > 3.0 V)	-	24	-	dB
		PSRR (V _{DD} < 3.0 V)	_	30	_	dB



AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC GPIO Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
F _{GPIO}	GPIO operating frequency	Normal strong mode port 0, 1	0	-	6 MHz for 1.71 V <v<sub>DD < 2.40 V 12 MHz for</v<sub>	MHz
			0	-	2.40 V < V _{DD} < 5.50 V	
T _{RISE23}	Rise time, strong mode, Cload = 50 pF ports 2 or 3	V _{DD} = 3.0 to 3.6 V, 10% – 90%	15	-	80	ns
T _{RISE23L}	Rise time, strong mode low supply, Cload = 50 pF, ports 2 or 3	V _{DD} = 1.71 to 3.0 V, 10% – 90%	15	-	80	ns
T _{RISE01}	Rise time, strong mode, Cload = 50 pF ports 0 or 1	V _{DD} = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	-	50	ns
T _{RISE01L}	Rise time, strong mode low supply, Cload = 50 pF, ports 0 or 1	V _{DD} = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	10	-	80	ns
T _{FALL}	Fall time, strong mode, Cload = 50 pF all ports	V _{DD} = 3.0 to 3.6 V, 10% – 90%	10	-	50	ns
T _{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	V _{DD} = 1.71 to 3.0 V, 10% – 90%	10	_	70	ns

Figure 6. GPIO Timing Diagram





Table 19.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Тур	Max	Units
T _{DRATE}	Full-speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
T _{JR1}	Receiver jitter tolerance	To next transition	-18.5	_	18.5	ns
T _{JR2}	Receiver jitter tolerance	To pair transition	-9	_	9	ns
T _{DJ1}	FS driver jitter	To next transition	-3.5	_	3.5	ns
T _{DJ2}	FS driver jitter	To pair transition	-4.0	-	4.0	ns
T _{FDEOP}	Source jitter for differential transition	To SE0 transition	-2	_	5	ns
T _{FEOPT}	Source SE0 interval of EOP		160	_	175	ns
T _{FEOPR}	Receiver SE0 interval of EOP		82	_		ns
T _{FST}	Width of SE0 interval during differential transition		-	_	14	ns

Table 20. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Тур	Max	Units
T _{FR}	Transition rise time	50 pF	4	_	20	ns
T _{FF}	Transition fall time	50 pF	4	_	20	ns
T _{FRFM} ^[19]	Rise/fall time matching		90	_	111	%
Vcrs	Output signal crossover voltage		1.30	-	2.00	V

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 21. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
T _{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	-	_	100	ns

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. AC External Clock Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
F _{OSCEXT}	Frequency (external oscillator frequency)		0.75	-	25.20	MHz
	High period		20.60	-	5300	ns
	Low period		20.60	-	-	ns
	Power-up IMO to switch		150	-	-	μS

Note

 T_{FRFM} is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.



Table 25. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
F _{SCLK}	SCLK clock frequency	$V_{DD} \ge 2.4 V$	-	-	6	MHz
		V _{DD} < 2.4 V	-	-	3	
DC	SCLK duty cycle		-	50	-	%
T _{SETUP}	MISO to SCLK setup time	$V_{DD} \ge 2.4 \text{ V}$	60	_	_	ns
		V _{DD} < 2.4 V	100	-	-	
T _{HOLD}	SCLK to MISO hold time		40	-	-	ns
T _{OUT_VAL}	SCLK to MOSI valid time		-	-	40	ns
T _{OUT_H}	MOSI high time		40	_	_	ns

Figure 9. SPI Master Mode 0 and 2





BOTTOM VIEW



Figure 14. 32-Pin (5 × 5 × 0.55 mm) QFN

4. DIMENSIONS ARE IN MILLIMETERS

TOP VIEW

Figure 15. 48-Pin (7 × 7 × 1.0 mm) QFN SIDE VIEW



NOTES:

- 1. 🐼 HATCH AREA IS SOLDERABLE EXPOSED METAL.
- 2. REFERENCE JEDEC#: MO-220

3. PACKAGE WEIGHT: 13 \pm 1 mg

4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *G

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.



Thermal Impedances

Table 27. Thermal Impedances per Package

Package	Typical θ _{JA} ^[21]
24-QFN ^[22]	20.90 °C/W
32-QFN ^[22]	19.51 °C/W
48-QFN ^[22]	17.68 °C/W

Capacitance on Crystal Pins

Table 28. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
24-pin QFN	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

Notes

21. T_J = T_A + Power x θ_{JA}.
22. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.
23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.





Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240-V power supply, Euro-Plug adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466A-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3280-20x66 Universal CapSense Controller

The CY3280-20X66 CapSense Controller Kit is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller board
- CY3240-I2USB bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 retractable cable
- CY3280-20x66 Kit CD



Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Accessories (Emulation and Programming)

- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Table 30. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit ^[24]	Foot Kit ^[25]	Adapter ^[26]
CY8C20336H-24LQXI	24-pin QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 24
CY8C20446H-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 26

Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at http://www.cypress.com/?rID2748.

Notes

25. Foot kit includes surface mount feet that can be soldered to the target PCB.

27. Dual-function digital I/O pins also connect to the common analog mux.

^{24.} Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

^{26.} Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

^{28.} This part is available in limited quantities for in-circuit debugging during prototype development. It is not available in production volumes.





Ordering Information

The following table lists the CY8C20336H/CY8C20446H PSoC devices' key package features and ordering codes.

Table 31. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (KB)	SRAM (KB)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[27]	XRES Pin	USB
24-pin (4 × 4 × 0.6mm) QFN	CY8C20336H-24LQXI	8	1	1	20	20	Yes	No
32 pin (5 × 5 × 0.6 mm) QFN	CY8C20446H-24LQXI	16	2	1	28	28	Yes	No
48 pin (7 × 7 mm) QFN (OCD) ^[28]	CY8C20066A-24LTXI	32	2	1	36	36	Yes	Yes

Ordering Code Definitions





Document History Page

Document Title: CY8C20336H/CY8C20446H Haptics Enabled CapSense [®] Controller Document Number: 001-56223				
Revision	ECN	Origin of Change	Submission Date	Description of Change
**	2787411	VZD/AESA	10/15/2009	New datasheet.
*A	3016550	KEJO/KPOL	08/26/2010	Added CY8C20346H part. Updated 24-pin QFN and 32-pin QFN package diagrams. Content and format updated to match latest template.
*В	3089844	JPM	11/18/10	In Table 26, modified T_{LOW} and T_{HIGH} min values to 42. Updated T_{SS_HIGH} min value to 50; removed max value.
*C	3180479	YVA	02/23/11	Removed CY8C20346H part Changed title from CapSense Applications to Haptics Enabled CapSense Controller Updated Table 29 with Time at Maximum Temperature information
*D	3638625	YLIU/BVI	06/06/2012	Updated F_{SCLK} parameter in the SPI Slave AC Specifications table Updated Getting Started and Designing with PSoC Designer sections. Included Development Tools. Updated Software under Development Tool Selection section. Updated F_{SCLK} parameter in the Table 26, "SPI Slave AC Specifications," on page 24. Changed t _{OUT_HIGH} to t _{OUT_H} in Table 25, "SPI Master AC Specifications," on page 23 Updated package diagrams: 001-13937 to *D 001-13191 to *F
*E	3822568	DST	11/27/2012	Updated package diagrams: 001-13937 to *E 001-42168 to *E 001-13191 to *G