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Details

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| Product Status | Active |
|-------------------------|--|
| Applications | Capacitive Sensing |
| Core Processor | M8C |
| Program Memory Type | FLASH (8kB) |
| Controller Series | CY8C20xx6A |
| RAM Size | 1K x 8 |
| Interface | I ² C, SPI |
| Number of I/O | 36 |
| Voltage - Supply | 1.71V ~ 5.5V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 48-VFQFN Exposed Pad |
| Supplier Device Package | 48-QFN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20636a-24ltxi |
| | |

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CY8C20336H, CY8C20446H

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PSoC[®] Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low-cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The core
- CapSense analog system
- System resources (including a full-speed USB port).

A common, versatile bus allows connection between the I/O and the analog system.

Each CY8C20336H/446H PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1-V or 1.2-V analog reference, which together support capacitive sensing of up to 28 inputs^[2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

SmartSense™

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easyto-use and provides a robust noise immunity. It is the only autotuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.



Figure 1. CapSense System Block Diagram

Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Haptics TS2000 Controller

The CY8C20336H/CY8C20446H family of devices feature an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

Note 2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I^2C + 1 pin for modulator capacitor.





Additional System Resources

System resources provide additional capability, such as configurable USB and I²C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I²C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I²C enhanced slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note I2C Enhanced Slave Operation AN56007.
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced poweron-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

For in depth information, along with detailed programming details, see the $PSoC^{\mathbb{R}}$ Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.





Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

- 1. Select user modules.
- 2. Configure user modules.
- 3. Organize and connect.
- 4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.



Pinouts

The CY8C20336H/CY8C20446H PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

24-Pin QFN

Table 1. Pin Definitions - CY8C20336H ^[3, 4]

| Pin | Ту | pe | Namo | Description |
|-----|---------|--------|-----------------|---|
| No. | Digital | Analog | Maine | Description |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | I/O | I | P2[1] | |
| 4 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 5 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 6 | IOHR | Ι | P1[3] | SPI CLK |
| 7 | IOHR | I | P1[1] | ISSP CLK ^[5] , I ² C SCL, SPI MOSI |
| 8 | | | NC | No connection |
| 9 | Po | wer | Vss | Ground connection |
| 10 | IOHR | I | P1[0] | ISSP DATA ^[5] , I ² C SDA, SPI CLK |
| 11 | IOHR | I | P1[2] | |
| 12 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 13 | IOHR | I | P1[6] | |
| 14 | In | put | XRES | Active high external reset with internal pull down |
| 15 | I/O | Ι | P2[0] | |
| 16 | IOH | I | P0[0] | |
| 17 | IOH | I | P0[2] | |
| 18 | IOH | I | P0[4] | |
| 19 | IOH | I | P0[6] | |
| 20 | Po | wer | V _{DD} | Supply voltage |
| 21 | IOH | Ι | P0[7] | |
| 22 | IOH | I | P0[5] | |
| 23 | IOH | I | P0[3] | Integrating input |
| 24 | IOH | Ι | P0[1] | Integrating input |
| CP | Po | wer | V _{SS} | Center pad must be connected to ground |

Figure 2. CY8C20336H PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

- During power-up or reset event, device P1[1] and P1[0] may disturb the l²C bus. Use alternate pins if you encounter any issues.
 The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
 These are the ISSP pins, which are not High Z at POR (Power On Reset).



DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and -40 °C \leq T_A \leq 85 °C, 2.4 V to 3.0 V and -40 °C \leq T_A \leq 85 °C, or 1.71 V to 2.4 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|-------------------|---|---|------------------------|-------|------|-------|
| R _{PU} | Pull-up resistor | | 4 | 5.60 | 8 | kΩ |
| V _{OH1} | High output voltage port 2 or 3 pins | $I_{OH} \le 10 \ \mu$ A, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | _ | - | V |
| V _{OH2} | High output voltage port 2 or 3 pins | I _{OH} = 1 mA, maximum of 20 mA source current in all I/Os | V _{DD} – 0.90 | _ | _ | V |
| V _{OH3} | High output voltage port 0 or 1 pins with LDO regulator disabled for port 1 | I_{OH} < 10 μ A, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | - | _ | V |
| V _{OH4} | High output voltage port 0 or 1 pins with LDO regulator disabled for port 1 | I _{OH} = 5 mA, maximum of 20 mA source current in all I/Os | V _{DD} – 0.90 | - | _ | V |
| V _{OH5} | High output voltage port 1 pins with LDO regulator enabled for 3 V out | I_{OH} < 10 μ A, V _{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA | 2.85 | 3.00 | 3.30 | V |
| V _{OH6} | High output voltage port 1 pins with LDO regulator enabled for 3 V out | I _{OH} = 5 mA, V _{DD} > 3.1 V, maximum of 20 mA source current in all I/Os | 2.20 | - | _ | V |
| V _{OH7} | High output voltage port 1 pins with LDO enabled for 2.5 V out | I_{OH} < 10 μ A, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os | 2.35 | 2.50 | 2.75 | V |
| V _{OH8} | High output voltage port 1 pins with LDO enabled for 2.5 V out | I _{OH} = 2 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os | 1.90 | - | - | V |
| V _{OH9} | High output voltage port 1 pins with LDO enabled for 1.8 V out | I_{OH} < 10 μ A, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os | 1.60 | 1.80 | 2.10 | V |
| V _{OH10} | High output voltage port 1 pins with LDO enabled for 1.8 V out | I _{OH} = 1 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os | 1.20 | _ | _ | V |
| V _{OL} | Low output voltage | I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]) | - | - | 0.75 | V |
| V _{IL} | Input low voltage | | - | _ | 0.80 | V |
| V _{IH} | Input high voltage | | 2.00 | - | - | V |
| V _H | Input hysteresis voltage | | _ | 80 | _ | mV |
| I _{IL} | Input leakage (absolute value) | | _ | 0.001 | 1 | μA |
| C _{PIN} | Pin capacitance | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |



Table 8. 2.4 V to 3.0 V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Тур | Мах | Units |
|-------------------|---|--|------------------------|------|------|-------|
| R _{PU} | Pull-up resistor | | 4 | 5.60 | 8 | kΩ |
| V _{OH1} | High output voltage port 2 or 3 pins | I_{OH} < 10 μ A, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | _ | _ | V |
| V _{OH2} | High output voltage port 2 or 3 pins | I _{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.40 | Ι | - | V |
| V _{OH3} | High output voltage port 0 or 1 pins with LDO regulator disabled for port 1 | I_{OH} < 10 μ A, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | - | - | V |
| V _{OH4} | High output voltage port 0 or 1 pins with LDO regulator disabled for port 1 | I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.50 | _ | - | V |
| V _{OH5A} | High output voltage port 1 pins with LDO enabled for 1.8 V out | I_{OH} < 10 μ A, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os | 1.50 | 1.80 | 2.10 | V |
| V _{OH6A} | High output voltage port 1 pins with LDO enabled for 1.8 V out | I _{OH} = 1 mA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os | 1.20 | _ | - | V |
| V _{OL} | Low output voltage | I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | - | - | 0.75 | V |
| V _{IL} | Input low voltage | | - | - | 0.72 | V |
| V _{IH} | Input high voltage | | 1.40 | _ | _ | V |
| V _H | Input hysteresis voltage | | _ | 80 | _ | mV |
| IIL | Input leakage (absolute value) | | _ | 1 | 1000 | nA |
| C _{PIN} | Capacitive load on pins | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |

Table 9. 1.71 V to 2.4 V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|------------------|---|---|------------------------|------|----------------------|-------|
| R _{PU} | Pull-up resistor | | 4 | 5.60 | 8 | kΩ |
| V _{OH1} | High output voltage port 2 or 3 pins | I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | _ | - | V |
| V _{OH2} | High output voltage port 2 or 3 pins | I _{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.50 | - | - | V |
| V _{OH3} | High output voltage port 0 or 1 pins with LDO regulator disabled for port 1 | I _{OH} = 100 μA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | - | - | V |
| V _{OH4} | High output voltage port 0 or 1 pins with LDO regulator disabled for port 1 | I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.50 | - | - | V |
| V _{OL} | Low output voltage | I _{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | _ | - | 0.40 | V |
| V _{IL} | Input low voltage | | - | - | $0.30 \times V_{DD}$ | V |
| V _{IH} | Input high voltage | | $0.65 \times V_{DD}$ | - | - | V |



Table 9. 1.71 V to 2.4 V DC GPIO Specifications (continued)

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|------------------|--------------------------------|---|------|------|------|-------|
| V _H | Input hysteresis voltage | | - | 80 | - | mV |
| IIL | Input leakage (absolute value) | | - | 1 | 1000 | nA |
| C _{PIN} | Capacitive load on pins | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |

Table 10.DC Characteristics – USB Interface

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|--------|--------------------------------------|-----------------------------|-------|------|-------|-------|
| Rusbi | USB D+ pull-up resistance | With idle bus | 900 | - | 1575 | Ω |
| Rusba | USB D+ pull-up resistance | While receiving traffic | 1425 | - | 3090 | Ω |
| Vohusb | Static output high | | 2.8 | - | 3.6 | V |
| Volusb | Static output low | | - | - | 0.3 | V |
| Vdi | Differential input sensitivity | | 0.2 | - | - | V |
| Vcm | Differential input common mode range | | 0.8 | - | 2.5 | V |
| Vse | Single-ended receiver threshold | | 0.8 | - | 2.0 | V |
| Cin | Transceiver capacitance | | - | - | 50 | pF |
| lio | High-Z state data line leakage | On D+ or D- line | -10 | - | +10 | μA |
| Rps2 | PS/2 pull-up resistance | | 3000 | 5000 | 7000 | Ω |
| Rext | External USB series resistor | In series with each USB pin | 21.78 | 22.0 | 22.22 | Ω |

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC Analog Mux Bus Specifications

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|------------------|---|------------|-----|-----|-----|-------|
| R _{SW} | Switch resistance to common analog bus | | - | - | 800 | Ω |
| R _{GND} | Resistance of initialization switch to V_{SS} | | _ | - | 800 | Ω |

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. DC Comparator Specifications

| Symbol | Description | Conditions | Min | Тур | Мах | Units |
|--------------------|--|--|-----|-----|-----|-------|
| V _{LPC} | Low power comparator (LPC) common mode | Maximum voltage limited to V _{DD} | 0.0 | - | 1.8 | V |
| I _{LPC} | LPC supply current | | - | 10 | 40 | μΑ |
| V _{OSLPC} | LPC voltage offset | | _ | 2.5 | 30 | mV |



DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC POR and LVD Specifications

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|-------------------|----------------------------------|---|----------------------|------|------|-------|
| V _{POR0} | 1.66 V selected in PSoC Designer | V_{DD} must be greater than or equal to 1.71 V | 1.61 | 1.66 | 1.71 | V |
| V _{POR1} | 2.36 V selected in PSoC Designer | during startup, reset from the XRES pin, or reset from watchdog | - | 2.36 | 2.41 | |
| V _{POR2} | 2.60 V selected in PSoC Designer | reset nom waterladg. | - | 2.60 | 2.66 | |
| V _{POR3} | 2.82 V selected in PSoC Designer | | - | 2.82 | 2.95 | |
| V _{LVD0} | 2.45 V selected in PSoC Designer | | 2.40 | 2.45 | 2.51 | V |
| V _{LVD1} | 2.71 V selected in PSoC Designer | | 2.64 ^[14] | 2.71 | 2.78 | |
| V _{LVD2} | 2.92 V selected in PSoC Designer | | 2.85 ^[15] | 2.92 | 2.99 | |
| V _{LVD3} | 3.02 V selected in PSoC Designer | | 2.95 ^[16] | 3.02 | 3.09 | |
| V _{LVD4} | 3.13 V selected in PSoC Designer | | 3.06 | 3.13 | 3.20 | |
| V _{LVD5} | 1.90 V selected in PSoC Designer | | 1.84 | 1.90 | 2.32 | |
| V _{LVD6} | 1.80 V selected in PSoC Designer | | 1.75 ^[17] | 1.80 | 1.84 | |
| V _{LVD7} | 4.73 V selected in PSoC Designer | | 4.62 | 4.73 | 4.83 | |

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. DC Programming Specifications

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|-----------------------|---|---|-----------------|-----|------------------------|-------|
| Vdd _{IWRITE} | Supply voltage for flash write operations | | 1.71 | - | 5.25 | V |
| I _{DDP} | Supply current during programming or verify | | _ | 5 | 25 | mA |
| V _{ILP} | Input low voltage during programming or verify | See the appropriate DC General Purpose I/O Specifications on page 13 | - | _ | V _{IL} | V |
| V _{IHP} | Input high voltage during programming or verify | See appropriate DC General Purpose I/O Specifications on page 13 table on pages 15 or 16 | V _{IH} | - | _ | V |
| I _{ILP} | Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify | Driving internal pull-down resistor | - | - | 0.2 | mA |
| I _{IHP} | Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify | Driving internal pull-down resistor | - | - | 1.5 | mA |
| V _{OLP} | Output low voltage during programming or verify | | _ | - | V _{SS} + 0.75 | V |
| V _{OHP} | Output high voltage during programming or verify | See appropriate DC General Purpose I/O Specifications on page 13 table on page 16. For V_{DD} > 3 V use V_{OH4} in Table 5 on page 11. | V _{OH} | _ | V _{DD} | V |
| Flash _{ENPB} | Flash write endurance | Erase/write cycles per block | 50,000 | - | - | - |
| Flash _{DR} | Flash data retention | Following maximum flash write cycles; ambient temperature of 55 °C | 10 | 20 | - | Years |

Notes

- 14. Always greater than 50 mV above V_{PPOR1} voltage for falling supply. 15. Always greater than 50 mV above V_{PPOR2} voltage for falling supply. 16. Always greater than 50 mV above V_{PPOR3} voltage for falling supply. 17. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.



AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Chip-Level Specifications

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|------------------------|---|---|------|-----|-------|-------|
| F _{IMO24} | IMO frequency at 24-MHz setting | | 22.8 | 24 | 25.2 | MHz |
| F _{IMO12} | IMO frequency at 12-MHz setting | | 11.4 | 12 | 12.6 | MHz |
| F _{IMO6} | IMO frequency at 6-MHz setting | | 5.7 | 6.0 | 6.3 | MHz |
| F _{CPU} | CPU frequency | | 0.75 | - | 25.20 | MHz |
| F _{32K1} | ILO frequency | | 19 | 32 | 50 | kHz |
| F _{32K_U} | ILO untrimmed frequency | | 13 | 32 | 82 | kHz |
| DC _{IMO} | Duty cycle of IMO | | 40 | 50 | 60 | % |
| DC _{ILO} | ILO duty cycle | | 40 | 50 | 60 | % |
| SR _{POWER_UP} | Power supply slew rate | V _{DD} slew rate during power-up | - | - | 250 | V/ms |
| T _{XRST} | External reset pulse width at power-up | After supply voltage is valid | 1 | - | - | ms |
| T _{XRST2} | External reset pulse width after power-up ^[18] | Applies after part has booted | 10 | - | - | μS |



AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC GPIO Specifications

| Symbol | Description | Conditions | Min | Тур | Мах | Units |
|----------------------|---|---|-----|-----|--|-------|
| F _{GPIO} | GPIO operating frequency | Normal strong mode port 0, 1 | 0 | - | 6 MHz for 1.71 V <v<sub>DD < 2.40 V 12 MHz for</v<sub> | MHz |
| | | | 0 | - | 2.40 V < V _{DD} < 5.50 V | |
| T _{RISE23} | Rise time, strong mode, Cload = 50 pF ports 2 or 3 | V _{DD} = 3.0 to 3.6 V, 10% – 90% | 15 | - | 80 | ns |
| T _{RISE23L} | Rise time, strong mode low supply, Cload = 50 pF, ports 2 or 3 | V _{DD} = 1.71 to 3.0 V, 10% – 90% | 15 | - | 80 | ns |
| T _{RISE01} | Rise time, strong mode, Cload = 50 pF ports 0 or 1 | V _{DD} = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled | 10 | - | 50 | ns |
| T _{RISE01L} | Rise time, strong mode low supply, Cload = 50 pF, ports 0 or 1 | V _{DD} = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled | 10 | - | 80 | ns |
| T _{FALL} | Fall time, strong mode, Cload = 50 pF all ports | V _{DD} = 3.0 to 3.6 V, 10% – 90% | 10 | - | 50 | ns |
| T _{FALLL} | Fall time, strong mode low supply, Cload = 50 pF, all ports | V _{DD} = 1.71 to 3.0 V, 10% – 90% | 10 | _ | 70 | ns |

Figure 6. GPIO Timing Diagram





AC Programming Specifications

Figure 7. AC Waveform

The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. AC Programming Specifications

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|----------------------|---|---|-------|-----|-------|-------|
| T _{RSCLK} | Rise time of SCLK | | 1 | — | 20 | ns |
| T _{FSCLK} | Fall time of SCLK | | 1 | - | 20 | ns |
| T _{SSCLK} | Data Setup time to falling edge of SCLK | | 40 | - | - | ns |
| T _{HSCLK} | Data Hold time from falling edge of SCLK | | 40 | _ | - | ns |
| F _{SCLK} | Frequency of SCLK | | 0 | - | 8 | MHz |
| T _{ERASEB} | Flash erase time (Block) | | - | - | 18 | ms |
| T _{WRITE} | Flash block write time | | - | _ | 25 | ms |
| T _{DSCLK} | Data out delay from falling edge of SCLK | 3.6 < V _{DD} | - | - | 60 | ns |
| T _{DSCLK3} | Data out delay from falling edge of SCLK | $3.0 \leq V_{DD} \leq 3.6$ | - | - | 85 | ns |
| T _{DSCLK2} | Data out delay from falling edge of SCLK | $1.71 \le V_{DD} \le 3.0$ | - | - | 130 | ns |
| T _{XRST3} | External reset pulse width after power-up | Required to enter programming mode when coming out of sleep | 300 | - | - | μS |
| T _{XRES} | XRES Pulse Length | | 300 | - | - | μS |
| T _{VDDWAIT} | V _{DD} stable to wait-and-poll hold off | | 0.1 | - | 1 | ms |
| T _{VDDXRES} | V _{DD} stable to XRES assertion delay | | 14.27 | - | - | ms |
| T _{POLL} | SDATA high pulse time | | 0.01 | - | 200 | ms |
| T _{ACQ} | "Key window" time after a V _{DD} ramp acquire event, based on 256 ILO clocks. | | 3.20 | - | 19.60 | ms |
| T _{XRESINI} | "Key window" time after an XRES event, based on eight ILO clocks | | 98 | - | 615 | μS |



Table 25. SPI Master AC Specifications

| Symbol | Description | Conditions | Min | Тур | Мах | Units |
|----------------------|-------------------------|----------------------------|-----|-----|-----|-------|
| F _{SCLK} | SCLK clock frequency | $V_{DD} \ge 2.4 V$ | - | - | 6 | MHz |
| | | V _{DD} < 2.4 V | - | - | 3 | |
| DC | SCLK duty cycle | | - | 50 | - | % |
| T _{SETUP} | MISO to SCLK setup time | $V_{DD} \ge 2.4 \text{ V}$ | 60 | _ | _ | ns |
| | | V _{DD} < 2.4 V | 100 | - | - | |
| T _{HOLD} | SCLK to MISO hold time | | 40 | - | - | ns |
| T _{OUT_VAL} | SCLK to MOSI valid time | | - | - | 40 | ns |
| T _{OUT_H} | MOSI high time | | 40 | _ | _ | ns |

Figure 9. SPI Master Mode 0 and 2









Figure 11. SPI Slave Mode 0 and 2







Packaging Information

This section illustrates the packaging specifications for the CY8C20336H/CY8C20446H PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.



Figure 13. 24-Pin (4 × 4 × 0.55 mm) QFN

<u>NOTES</u> :

- 1. 💥 HATCH IS SOLDERABLE EXPOSED METAL.
- 2. REFERENCE JEDEC # MO-248
- 3. PACKAGE WEIGHT : 29 \pm 3 mg
- 4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *E



Thermal Impedances

Table 27. Thermal Impedances per Package

| Package | Typical θ _{JA} ^[21] |
|------------------------|---|
| 24-QFN ^[22] | 20.90 °C/W |
| 32-QFN ^[22] | 19.51 °C/W |
| 48-QFN ^[22] | 17.68 °C/W |

Capacitance on Crystal Pins

Table 28. Typical Package Capacitance on Crystal Pins

| Package | Package Capacitance |
|------------|---------------------|
| 32-pin QFN | 3.2 pF |
| 48-pin QFN | 3.3 pF |

Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

Table 29. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Time at Maximum Peak Temperature |
|------------|--------------------------|----------------------------------|
| 24-pin QFN | 260 °C | 30 s |
| 32-pin QFN | 260 °C | 30 s |
| 48-pin QFN | 260 °C | 30 s |

Notes

21. T_J = T_A + Power x θ_{JA}.
22. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.
23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.





Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240-V power supply, Euro-Plug adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466A-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3280-20x66 Universal CapSense Controller

The CY3280-20X66 CapSense Controller Kit is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller board
- CY3240-I2USB bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 retractable cable
- CY3280-20x66 Kit CD



Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

| Acronym | Description |
|------------------|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CMOS | complementary metal oxide semiconductor |
| CPU | central processing unit |
| DAC | digital-to-analog converter |
| DC | direct current |
| EOP | end of packet |
| FSR | full scale range |
| GPIO | general purpose input/output |
| GUI | graphical user interface |
| l ² C | inter-integrated circuit |
| ICE | in-circuit emulator |
| IDAC | digital analog converter current |
| ILO | internal low speed oscillator |
| IMO | internal main oscillator |
| I/O | input/output |
| ISSP | in-system serial programming |
| LCD | liquid crystal display |
| LDO | low dropout (regulator) |
| LSB | least-significant bit |
| LVD | low voltage detect |
| MCU | micro-controller unit |
| MIPS | mega instructions per second |
| MISO | master in slave out |
| MOSI | master out slave in |
| MSB | most-significant bit |
| OCD | on-chip debugger |
| POR | power on reset |
| PPOR | precision power on reset |
| PSRR | power supply rejection ratio |
| PWRSYS | power system |
| PSoC® | Programmable System-on-Chip |
| SLIMO | slow internal main oscillator |
| SRAM | static random access memory |
| SNR | signal to noise ratio |
| QFN | quad flat no-lead |
| SCL | serial I ² C clock |
| SDA | serial I ² C data |
| SDATA | serial ISSP data |
| SPI | serial peripheral interface |
| SS | slave select |
| SSOP | shrink small outline package |
| TC | test controller |
| USB | universal serial bus |
| USB D+ | USB Data + |
| USB D- | USB Data- |
| WLCSP | wafer level chip scale package |
| XTAL | crystal |
| | - |

Units of Measure

Table 32 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Table 32. Units of Measure

| Symbol | Unit of Measure |
|--------|-------------------------------|
| °C | degree Celsius |
| dB | decibels |
| fF | femto farad |
| g | gram |
| Hz | hertz |
| KB | 1024 bytes |
| Kbit | 1024 bits |
| KHz | kilohertz |
| Ksps | kilo samples per second |
| kΩ | kilohm |
| MHz | megahertz |
| MΩ | megaohm |
| μA | microampere |
| μF | microfarad |
| μH | microhenry |
| μS | microsecond |
| μW | microwatts |
| mA | milli-ampere |
| ms | milli-second |
| mV | milli-volts |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolts |
| Ω | ohm |
| pА | picoampere |
| pF | picofarad |
| рр | peak-to-peak |
| ppm | parts per million |
| ps | picosecond |
| sps | samples per second |
| S | sigma: one standard deviation |
| V | volts |
| W | watt |



Glossary

| Crosspoint connection | Connection between any GPIO combination via analog multiplexer bus. |
|-------------------------------------|---|
| Differential non-linearity | Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. |
| Hold time | Hold time is the time following a clock event during which the data input to a latch or flip- flop must remain stable in order to guarantee that the latched data is correct. |
| l ² C | It is a serial multi-master bus used to connect low speed peripherals to MCU. |
| Integral nonlinearity | It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level. |
| Latch up current | Current at which the latch up test is conducted according to JESD78 standard (at 125 °C) |
| Power supply rejection ratio (PSRR) | The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device. |
| Scan | The conversion of all sensor capacitances to digital values. |
| Setup time | Period required to prepare a device, machine, process, or system for it to be ready to function. |
| Signal-to-noise ratio | The ratio between a capacitive finger signal and system noise. |
| SPI | Serial peripheral interface is a synchronous serial data link standard. |

Reference Documents

■ Technical reference manual for CY8C20xx6 devices

■ In-system Serial Programming (ISSP) protocol for 20xx6 – AN2026C

Host Sourced Serial Programming for 20xx6 devices – AN59389



Document History Page

| Document Title: CY8C20336H/CY8C20446H Haptics Enabled CapSense [®] Controller Document Number: 001-56223 | | | | |
|--|---------|---------------------|--------------------|--|
| Revision | ECN | Origin of Change | Submission Date | Description of Change |
| ** | 2787411 | VZD/AESA | 10/15/2009 | New datasheet. |
| *A | 3016550 | KEJO/KPOL | 08/26/2010 | Added CY8C20346H part. Updated 24-pin QFN and 32-pin QFN package diagrams. Content and format updated to match latest template. |
| *В | 3089844 | JPM | 11/18/10 | In Table 26, modified T_{LOW} and T_{HIGH} min values to 42. Updated T_{SS_HIGH} min value to 50; removed max value. |
| *C | 3180479 | YVA | 02/23/11 | Removed CY8C20346H part Changed title from CapSense Applications to Haptics Enabled CapSense Controller Updated Table 29 with Time at Maximum Temperature information |
| *D | 3638625 | YLIU/BVI | 06/06/2012 | Updated F_{SCLK} parameter in the SPI Slave AC Specifications table Updated Getting Started and Designing with PSoC Designer sections. Included Development Tools. Updated Software under Development Tool Selection section. Updated F_{SCLK} parameter in the Table 26, "SPI Slave AC Specifications," on page 24. Changed t _{OUT_HIGH} to t _{OUT_H} in Table 25, "SPI Master AC Specifications," on page 23 Updated package diagrams: 001-13937 to *D 001-13191 to *F |
| *E | 3822568 | DST | 11/27/2012 | Updated package diagrams: 001-13937 to *E 001-42168 to *E 001-13191 to *G |