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**[Embedded - Microcontrollers - Application Specific](#): Tailored Solutions for Precision and Performance**

**[Embedded - Microcontrollers - Application Specific](#)** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

**What Are [Embedded - Microcontrollers - Application Specific](#)?**

Application specific microcontrollers are engineered to

#### Details

Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (32kB)
Controller Series	CY8C20xx6A
RAM Size	2K x 8
Interface	I <sup>2</sup> C, SPI, USB
Number of I/O	36
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-QFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20666as-24lqxi">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20666as-24lqxi</a>

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## Additional System Resources

System resources provide additional capability, such as configurable USB and I<sup>2</sup>C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I<sup>2</sup>C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I<sup>2</sup>C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I<sup>2</sup>C enhanced slave interface appears as a 32-byte RAM buffer to the external I<sup>2</sup>C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note [I2C Enhanced Slave Operation - AN56007](#).
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

## Getting Started

For in depth information, along with detailed programming details, see the PSoC® [Technical Reference Manual](#).

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

## Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

## Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

## Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via [www.cypress.com](http://www.cypress.com), covers a wide variety of topics and skill levels to assist you in your designs.

## CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

## Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

## Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I<sup>2</sup>C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

### PSoC Designer Software Subsystems

#### *Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

#### *Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers.** The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

#### *Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

#### *Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

#### *In-Circuit Emulator*

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

## Pinouts

The CY8C20336H/CY8C20446H PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V<sub>SS</sub>, V<sub>DD</sub>, and XRES are not capable of digital I/O.

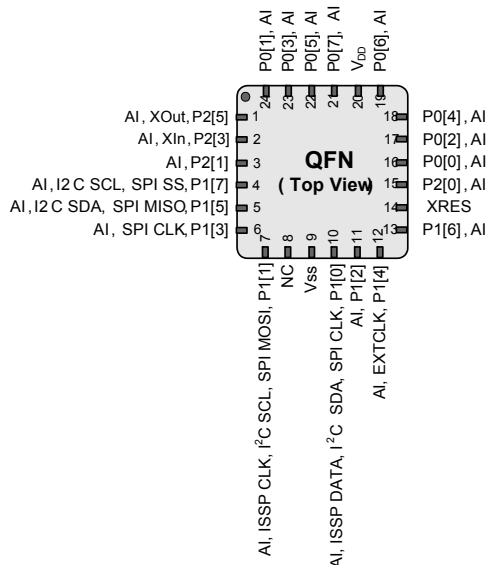
### 24-Pin QFN

**Table 1. Pin Definitions - CY8C20336H** [3, 4]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS
5	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK <sup>[5]</sup> , I <sup>2</sup> C SCL, SPI MOSI
8			NC	No connection
9	Power		V <sub>SS</sub>	Ground connection
10	IOHR	I	P1[0]	ISSP DATA <sup>[5]</sup> , I <sup>2</sup> C SDA, SPI CLK
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down
15	I/O	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		V <sub>DD</sub>	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 2. CY8C20336H PSoC Device**



#### Notes

- During power-up or reset event, device P1[1] and P1[0] may disturb the I<sup>2</sup>C bus. Use alternate pins if you encounter any issues.
- The center pad (CP) on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- These are the ISSP pins, which are not High Z at POR (Power On Reset).



## DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 6. DC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DD}^{[13]}$	Supply voltage	Refer the table <a href="#">DC POR and LVD Specifications on page 17</a>	1.71	–	5.50	V
$I_{DD24}$	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	3.32	4.00	mA
$I_{DD12}$	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.86	2.60	mA
$I_{DD6}$	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.13	1.80	mA
$I_{SB0}$	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	0.50	μA
$I_{SB1}$	Standby current with POR, LVD, and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	μA

### Note

13. When  $V_{DD}$  remains in the range from 1.71 V to 1.9 V for more than 50 μsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the  $SR_{POWER\_UP}$  parameter.

### Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range:  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ .

**Table 13. Comparator User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{\text{COMP}}$	Comparator response time	50-mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to $V_{DD} - 0.2\text{ V}$	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	$\mu\text{A}$
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input Range			0	–	1.5	V

### ADC Electrical Specifications

**Table 14. ADC User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>Input</b>						
$V_{\text{IN}}$	Input voltage range		0	–	$V_{\text{REFADC}}$	V
$C_{\text{IIN}}$	Input capacitance		–	–	5	pF
$R_{\text{IN}}$	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500\text{fF} \times \text{data clock})$	$1/(400\text{fF} \times \text{data clock})$	$1/(300\text{fF} \times \text{data clock})$	$\Omega$
<b>Reference</b>						
$V_{\text{REFADC}}$	ADC reference voltage		1.14	–	1.26	V
<b>Conversion Rate</b>						
$F_{\text{CLK}}$	Data clock	Source is chip's internal main oscillator. See <a href="#">AC Chip-Level Specifications on page 18</a> for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. Sample Rate = $0.001/(2^{\text{Resolution}}/\text{Data clock})$	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. Sample Rate = $0.001/(2^{\text{Resolution}}/\text{Data clock})$	–	5.85	–	ksps
<b>DC Accuracy</b>						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity		–1	–	+2	LSB
INL	<a href="#">Integral nonlinearity</a>		–2	–	+2	LSB
$E_{\text{OFFSET}}$	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
$E_{\text{GAIN}}$	Gain error	For any resolution	–5	–	+5	%FSR
<b>Power</b>						
$I_{\text{ADC}}$	Operating current		–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR ( $V_{DD} > 3.0\text{ V}$ )	–	24	–	dB
		PSRR ( $V_{DD} < 3.0\text{ V}$ )	–	30	–	dB



## DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 15. DC POR and LVD Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>POR0</sub>	1.66 V selected in PSoC Designer	V <sub>DD</sub> must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V <sub>POR1</sub>	2.36 V selected in PSoC Designer		–	2.36	2.41	
V <sub>POR2</sub>	2.60 V selected in PSoC Designer		–	2.60	2.66	
V <sub>POR3</sub>	2.82 V selected in PSoC Designer		–	2.82	2.95	
V <sub>LVD0</sub>	2.45 V selected in PSoC Designer		2.40	2.45	2.51	V
V <sub>LVD1</sub>	2.71 V selected in PSoC Designer		2.64 <sup>[14]</sup>	2.71	2.78	
V <sub>LVD2</sub>	2.92 V selected in PSoC Designer		2.85 <sup>[15]</sup>	2.92	2.99	
V <sub>LVD3</sub>	3.02 V selected in PSoC Designer		2.95 <sup>[16]</sup>	3.02	3.09	
V <sub>LVD4</sub>	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V <sub>LVD5</sub>	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V <sub>LVD6</sub>	1.80 V selected in PSoC Designer		1.75 <sup>[17]</sup>	1.80	1.84	
V <sub>LVD7</sub>	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

## DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 16. DC Programming Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>DDIWRITE</sub>	Supply voltage for flash write operations		1.71	–	5.25	V
I <sub>DDP</sub>	Supply current during programming or verify		–	5	25	mA
V <sub>ILP</sub>	Input low voltage during programming or verify	See the appropriate <a href="#">DC General Purpose I/O Specifications on page 13</a>	–	–	V <sub>IL</sub>	V
V <sub>IHP</sub>	Input high voltage during programming or verify	See appropriate <a href="#">DC General Purpose I/O Specifications on page 13</a> table on pages 15 or 16	V <sub>IH</sub>	–	–	V
I <sub>ILP</sub>	Input current when applying V <sub>ILP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I <sub>IHP</sub>	Input current when applying V <sub>IHP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V <sub>OLP</sub>	Output low voltage during programming or verify		–	–	V <sub>SS</sub> + 0.75	V
V <sub>OHP</sub>	Output high voltage during programming or verify	See appropriate <a href="#">DC General Purpose I/O Specifications on page 13</a> table on page 16. For V <sub>DD</sub> > 3 V use V <sub>OH4</sub> in <a href="#">Table 5 on page 11</a> .	V <sub>OH</sub>	–	V <sub>DD</sub>	V
Flash <sub>ENPB</sub>	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
Flash <sub>DR</sub>	Flash data retention	Following maximum flash write cycles; ambient temperature of 55 °C	10	20	–	Years

### Notes

14. Always greater than 50 mV above V<sub>PPOR1</sub> voltage for falling supply.
15. Always greater than 50 mV above V<sub>PPOR2</sub> voltage for falling supply.
16. Always greater than 50 mV above V<sub>PPOR3</sub> voltage for falling supply.
17. Always greater than 50 mV above V<sub>PPOR0</sub> voltage for falling supply.

## AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 17. AC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>IMO24</sub>	IMO frequency at 24-MHz setting		22.8	24	25.2	MHz
F <sub>IMO12</sub>	IMO frequency at 12-MHz setting		11.4	12	12.6	MHz
F <sub>IMO6</sub>	IMO frequency at 6-MHz setting		5.7	6.0	6.3	MHz
F <sub>CPU</sub>	CPU frequency		0.75	–	25.20	MHz
F <sub>32K1</sub>	ILO frequency		19	32	50	kHz
F <sub>32K_U</sub>	ILO untrimmed frequency		13	32	82	kHz
DC <sub>IMO</sub>	Duty cycle of IMO		40	50	60	%
DC <sub>ILO</sub>	ILO duty cycle		40	50	60	%
SR <sub>POWER_UP</sub>	Power supply slew rate	V <sub>DD</sub> slew rate during power-up	–	–	250	V/ms
T <sub>XRST</sub>	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
T <sub>XRST2</sub>	External reset pulse width after power-up <sup>[18]</sup>	Applies after part has booted	10	–	–	μs

### Note

18. The minimum required XRES pulse length is longer when programming the device (see [Table 23 on page 21](#)).

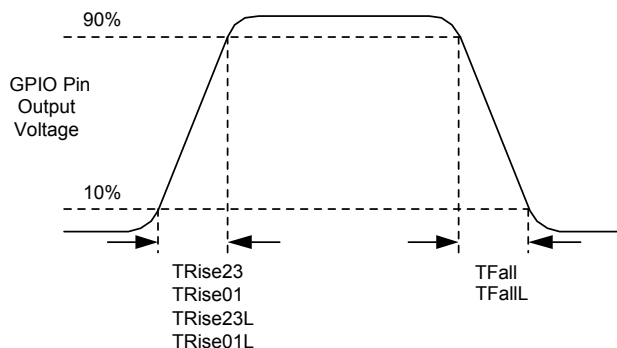
## AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 18. AC GPIO Specifications**

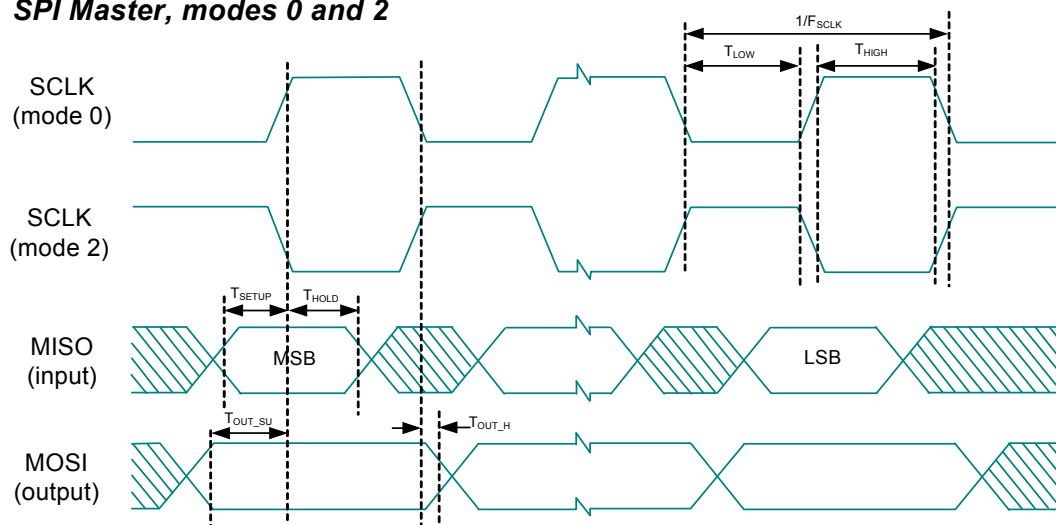
Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{GPIO}$	GPIO operating frequency	Normal strong mode port 0, 1	0	–	6 MHz for 1.71 V < $V_{DD}$ < 2.40 V 12 MHz for 2.40 V < $V_{DD}$ < 5.50 V	MHz
$T_{RISE23}$	Rise time, strong mode, Cload = 50 pF ports 2 or 3	$V_{DD}$ = 3.0 to 3.6 V, 10% – 90%	15	–	80	ns
$T_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, ports 2 or 3	$V_{DD}$ = 1.71 to 3.0 V, 10% – 90%	15	–	80	ns
$T_{RISE01}$	Rise time, strong mode, Cload = 50 pF ports 0 or 1	$V_{DD}$ = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	–	50	ns
$T_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, ports 0 or 1	$V_{DD}$ = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	10	–	80	ns
$T_{FALL}$	Fall time, strong mode, Cload = 50 pF all ports	$V_{DD}$ = 3.0 to 3.6 V, 10% – 90%	10	–	50	ns
$T_{FALLL}$	Fall time, strong mode low supply, Cload = 50 pF, all ports	$V_{DD}$ = 1.71 to 3.0 V, 10% – 90%	10	–	70	ns

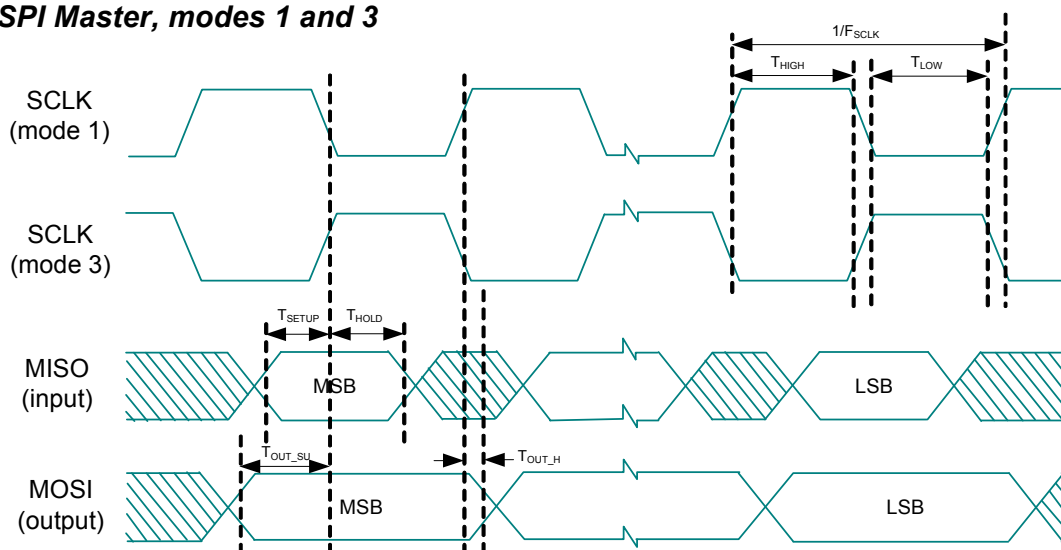
**Figure 6. GPIO Timing Diagram**



**Table 25. SPI Master AC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	$V_{DD} \geq 2.4 \text{ V}$ $V_{DD} < 2.4 \text{ V}$	— —	— —	6 3	MHz
DC	SCLK duty cycle		—	50	—	%
$T_{SETUP}$	MISO to SCLK setup time	$V_{DD} \geq 2.4 \text{ V}$ $V_{DD} < 2.4 \text{ V}$	60 100	— —	— —	ns
$T_{HOLD}$	SCLK to MISO hold time		40	—	—	ns
$T_{OUT\_VAL}$	SCLK to MOSI valid time		—	—	40	ns
$T_{OUT\_H}$	MOSI high time		40	—	—	ns

**Figure 9. SPI Master Mode 0 and 2**
**SPI Master, modes 0 and 2**


**Figure 10. SPI Master Mode 1 and 3**
**SPI Master, modes 1 and 3**

**Table 26. SPI Slave AC Specifications**

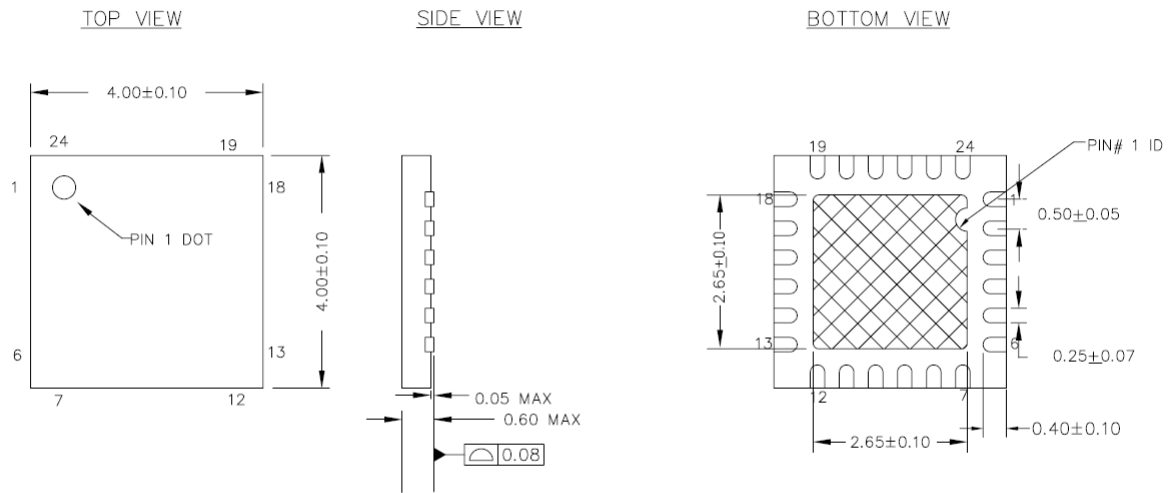
Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	—	—	—	4	MHz
$T_{LOW}$	SCLK low time	—	42	—	—	ns
$T_{HIGH}$	SCLK high time	—	42	—	—	ns
$T_{SETUP}$	MOSI to SCLK setup time	—	30	—	—	ns
$T_{HOLD}$	SCLK to MOSI hold time	—	50	—	—	ns
$T_{SS\_MISO}$	SS high to MISO valid	—	—	—	153	ns
$T_{SCLK\_MISO}$	SCLK to MISO valid	—	—	—	125	ns
$T_{SS\_HIGH}$	SS high time	—	50	—	—	ns
$T_{SS\_CLK}$	Time from SS low to first SCLK	—	2/SCLK	—	—	ns
$T_{CLK\_SS}$	Time from last SCLK to SS high	—	2/SCLK	—	—	ns

## Packaging Information


This section illustrates the packaging specifications for the CY8C20336H/CY8C20446H PSoC device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

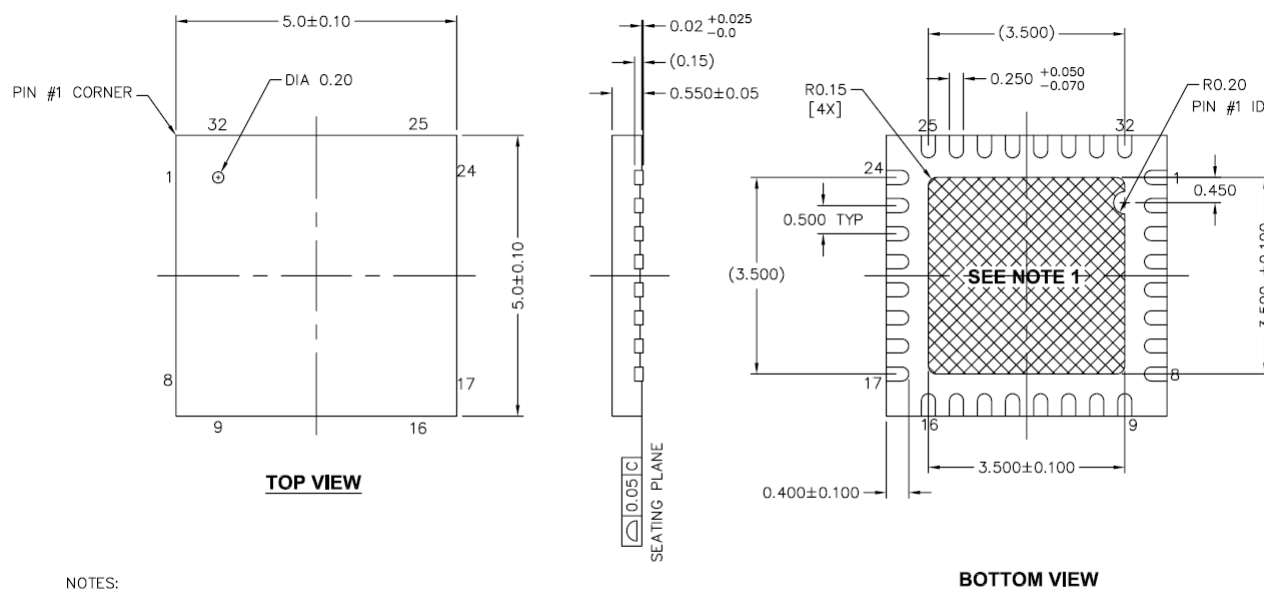
**Figure 13. 24-Pin ( $4 \times 4 \times 0.55$  mm) QFN**




### NOTES :

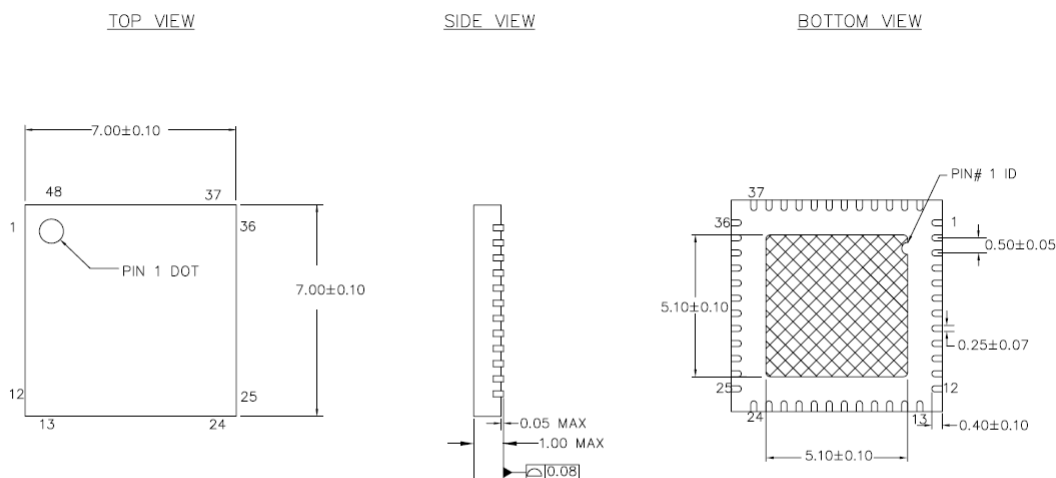
1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT :  $29 \pm 3$  mg
4. ALL DIMENSIONS ARE IN MILLIMETERS


001-13937 \*E

**Figure 14. 32-Pin (5 × 5 × 0.55 mm) QFN**

**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 \*E

**Figure 15. 48-Pin (7 × 7 × 1.0 mm) QFN**

**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 \*G

**Important Notes**

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at [http://www.amkor.com/products/notes\\_papers/MLFAppNote.pdf](http://www.amkor.com/products/notes_papers/MLFAppNote.pdf).
- Pinned vias for thermal conduction are not required for the low power PSoC device.

## Thermal Impedances

**Table 27. Thermal Impedances per Package**

Package	Typical $\theta_{JA}$ <sup>[21]</sup>
24-QFN <sup>[22]</sup>	20.90 °C/W
32-QFN <sup>[22]</sup>	19.51 °C/W
48-QFN <sup>[22]</sup>	17.68 °C/W

## Capacitance on Crystal Pins

**Table 28. Typical Package Capacitance on Crystal Pins**

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

## Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

**Table 29. Solder Reflow Peak Temperature**

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
24-pin QFN	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

### Notes

21.  $T_J = T_A + \text{Power} \times \theta_{JA}$ .

22. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are  $220 \pm 5$  °C with Sn-Pb or  $245 \pm 5$  °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.



## Development Tool Selection

### Software

#### *PSoC Designer*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at <http://www.cypress.com>.

#### *PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at <http://www.cypress.com>.

### Development Kits

All development kits are sold at the Cypress Online Store.

#### *CY3215-DK Basic Development Kit*

The **CY3215-DK** is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240-V power supply, Euro-Plug adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466A-24PXI 28-PDIP chip samples

### Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

#### *CY3210-MiniProg1*

The **CY3210-MiniProg1** kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

#### *CY3210-PSoCEval1*

The **CY3210-PSoCEval1** kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

#### *CY3280-20x66 Universal CapSense Controller*

The **CY3280-20X66 CapSense Controller Kit** is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller board
- CY3240-I2USB bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 retractable cable
- CY3280-20x66 Kit CD

## Device Programmers

All device programmers are purchased from the Cypress Online Store.

### CY3216 Modular Programmer

The **CY3216 Modular Programmer kit** features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD

- Getting Started Guide

- USB 2.0 Cable

### CY3207ISSP In-System Serial Programmer (ISSP)

The **CY3207ISSP** is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

## Accessories (Emulation and Programming)

**Table 30. Emulation and Programming Accessories**

Part Number	Pin Package	Flex-Pod Kit <sup>[24]</sup>	Foot Kit <sup>[25]</sup>	Adapter <sup>[26]</sup>
CY8C20336H-24LQXI	24-pin QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 24
CY8C20446H-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 26

## Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under Documentation > Evaluation Boards.

## Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at <http://www.cypress.com/?rID2748>.

## Notes

24. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

25. Foot kit includes surface mount feet that can be soldered to the target PCB.

26. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

27. Dual-function digital I/O pins also connect to the common analog mux.

28. This part is available in limited quantities for in-circuit debugging during prototype development. It is not available in production volumes.

## Document Conventions

### Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
EOP	end of packet
FSR	full scale range
GPIO	general purpose input/output
GUI	graphical user interface
I <sup>2</sup> C	inter-integrated circuit
ICE	in-circuit emulator
IDAC	digital analog converter current
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	mega instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debugger
POR	power on reset
PPOR	precision power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC®	Programmable System-on-Chip
SLIMO	slow internal main oscillator
SRAM	static random access memory
SNR	signal to noise ratio
QFN	quad flat no-lead
SCL	serial I <sup>2</sup> C clock
SDA	serial I <sup>2</sup> C data
SDATA	serial ISSP data
SPI	serial peripheral interface
SS	slave select
SSOP	shrink small outline package
TC	test controller
USB	universal serial bus
USB D+	USB Data +
USB D-	USB Data-
WLCSP	wafer level chip scale package
XTAL	crystal

### Units of Measure

Table 32 lists all the abbreviations used to measure the PSoC devices.

### Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

**Table 32. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
g	gram
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
KHz	kilohertz
Ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
Ω	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
s	sigma: one standard deviation
V	volts
W	watt

## Glossary

<b>Crosspoint connection</b>	Connection between any GPIO combination via analog multiplexer bus.
<b>Differential non-linearity</b>	Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.
<b>Hold time</b>	Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.
<b>I<sup>2</sup>C</b>	It is a serial multi-master bus used to connect low speed peripherals to MCU.
<b>Integral nonlinearity</b>	It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level.
<b>Latch up current</b>	Current at which the latch up test is conducted according to JESD78 standard (at 125 °C)
<b>Power supply rejection ratio (PSRR)</b>	The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device.
<b>Scan</b>	The conversion of all sensor capacitances to digital values.
<b>Setup time</b>	Period required to prepare a device, machine, process, or system for it to be ready to function.
<b>Signal-to-noise ratio</b>	The ratio between a capacitive finger signal and system noise.
<b>SPI</b>	Serial peripheral interface is a synchronous serial data link standard.

## Reference Documents

- Technical reference manual for [CY8C20xx6](#) devices
- In-system Serial Programming (ISSP) protocol for 20xx6 – [AN2026C](#)
- Host Sourced Serial Programming for 20xx6 devices – [AN59389](#)

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