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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atuc128d3-a2ur

- One Master and One Slave Two-Wire Interfaces (TWI), 400 kbit/s I^2C-compatible
- One 8-channel Analog-To-Digital Converter (ADC)
- One Inter-IC Sound Controller (IISC) with Stereo Capabilities
- Autonomous Capacitive Touch Button (QTouch®) Capture
  - Up to 25 Touch Buttons
  - QWheel® and QSlide® Compatible
- QTouch® Library Support
  - Capacitive Touch Buttons, Sliders, and Wheels
  - QTouch® and QMatrix® Acquisition
  - Hardware assisted QTouch® Acquisition
- One Programmable Glue Logic Controller(GLOC) for General Purpose PCB Design
- On-Chip Non-Intrusive Debug System
  - Nexus Class 2+, Runtime Control
  - aWire™ Single-Pin Programming and Debug Interface Muxed with Reset Pin
  - 64-pin and 48-pin TQFP/QFN (51 and 35 GPIO Pins)
- Four High-Drive I/O Pins
- Single 3.3V Power Supply or Dual 1.8V-3.3V Power Supply

Table 4-1. Signal Descriptions List

EXTTRIG	ADCIFD EXTTRIG	Input		
AD7 - AD0	ADC Inputs	Analog		
Power				
VDDIO	Digital I/O Power Supply	Power Input		3.0 V to 3.6V.
VDDANA	Analog Power Supply	Power Input		3.0 V to 3.6V
ADVREF	Analog Reference Voltage	Power Input		2.6 V to 3.6 V
VDDCORE	Core Power Supply	Power Input		1.65 V to 1.95 V
VDDIN	Voltage Regulator Input	Power Input		3.0 V to 3.6V
VDDOUT	Voltage Regulator Output	Power Output		1.65 V to 1.95V
GNDANA	Analog Ground	Ground		
GND	Ground	Ground		
General Purpose I/O pin - GPIOA, GPIOB				
PA31 - PA00	General Purpose I/O Controller GPIO A	I/O		
PB18 - PB00	General Purpose I/O Controller GPIO B	I/O		

4.1 I/O Line Considerations

4.1.1 JTAG Pins

The JTAG is enabled if TCK is low while the RESET_N pin is released. The TCK, TMS, and TDI pins have pull-up resistors when JTAG is enabled. TDO pin is an output, driven at VDDIO, and has no pull-up resistor. These JTAG pins can be used as GPIO pins and muxed with peripherals when the JTAG is disabled.

4.1.2 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a programmable pull-up resistor to VDDIO. As the product integrates a power-on reset detector, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

The RESET_N pin is also used for the aWire debug protocol. When the pin is used for debugging, it must not be driven by the application.

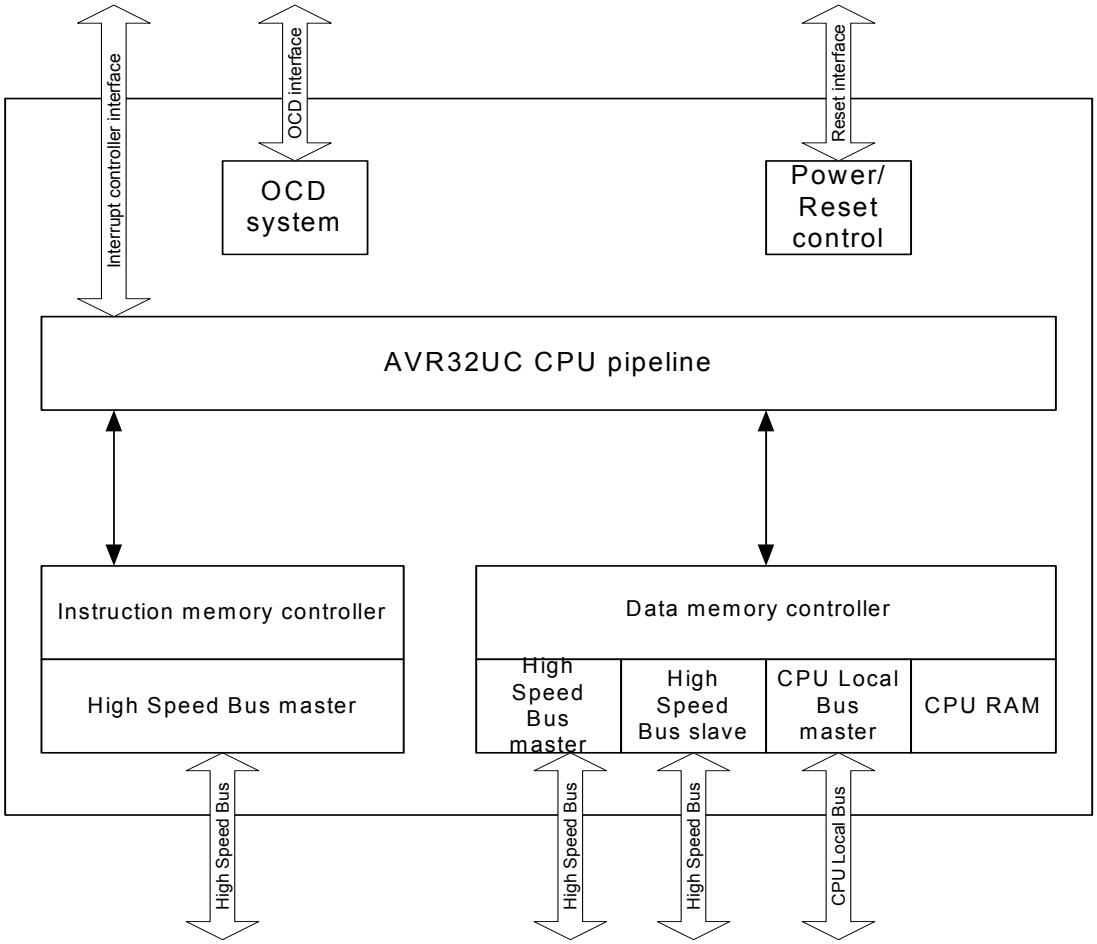
4.1.3 TWI Pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO pins or used for other peripherals, the pins have the same characteristics as GPIO pins.

4.1.4 GPIO Pins

All the I/O lines integrate a pull-up resistor. Programming of this pull-up resistor is performed

Figure 5-1. Overview of the AVR32UC CPU



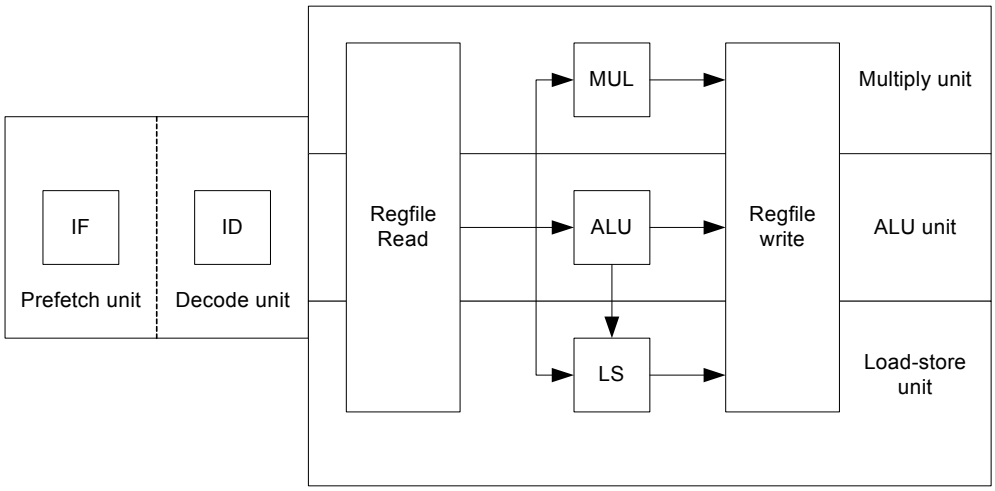
5.3.1 Pipeline Overview

AVR32UC has three pipeline stages, Instruction Fetch (IF), Instruction Decode (ID), and Instruction Execute (EX). The EX stage is split into three parallel subsections, one arithmetic/logic (ALU) section, one multiply (MUL) section, and one load/store (LS) section.

Instructions are issued and complete in order. Certain operations require several clock cycles to complete, and in this case, the instruction resides in the ID and EX stages for the required number of clock cycles. Since there is only three pipeline stages, no internal data forwarding is required, and no data dependencies can arise in the pipeline.

Figure 5-2 on page 23 shows an overview of the AVR32UC pipeline stages.

Figure 5-2. The AVR32UC Pipeline



5.3.2 AVR32A Microarchitecture Compliance

AVR32UC implements an AVR32A microarchitecture. The AVR32A microarchitecture is targeted at cost-sensitive, lower-end applications like smaller microcontrollers. This microarchitecture does not provide dedicated hardware registers for shadowing of register file registers in interrupt contexts. Additionally, it does not provide hardware registers for the return address registers and return status registers. Instead, all this information is stored on the system stack. This saves chip area at the expense of slower interrupt handling.

5.3.2.1 Interrupt Handling

Upon interrupt initiation, registers R8-R12 are automatically pushed to the system stack. These registers are pushed regardless of the priority level of the pending interrupt. The return address and status register are also automatically pushed to stack. The interrupt handler can therefore use R8-R12 freely. Upon interrupt completion, the old R8-R12 registers and status register are restored, and execution continues at the return address stored popped from stack.

The stack is also used to store the status register and return address for exceptions and *scall*. Executing the *rete* or *rets* instruction at the completion of an exception or system call will pop this status register and continue execution at the popped return address.

5.3.2.2 Java Support

AVR32UC does not provide Java hardware acceleration.

5.3.2.3 Unaligned Reference Handling

AVR32UC does not support unaligned accesses, except for doubleword accesses. AVR32UC is able to perform word-aligned *st.d* and *ld.d*. Any other unaligned memory access will cause an address exception. Doubleword-sized accesses with word-aligned pointers will automatically be performed as two word-sized accesses.

Debug state can be entered as described in the *AVR32UC Technical Reference Manual*.

Debug state is exited by the *retd* instruction.

5.4.4 System Registers

The system registers are placed outside of the virtual memory space, and are only accessible using the privileged *mfsr* and *mtsr* instructions. The table below lists the system registers specified in the AVR32 architecture, some of which are unused in AVR32UC. The programmer is responsible for maintaining correct sequencing of any instructions following a *mtsr* instruction. For detail on the system registers, refer to the *AVR32UC Technical Reference Manual*.

Table 5-3. System Registers

Reg #	Address	Name	Function
0	0	SR	Status Register
1	4	EVBA	Exception Vector Base Address
2	8	ACBA	Application Call Base Address
3	12	CPUCR	CPU Control Register
4	16	ECR	Exception Cause Register
5	20	RSR_SUP	Unused in AVR32UC
6	24	RSR_INT0	Unused in AVR32UC
7	28	RSR_INT1	Unused in AVR32UC
8	32	RSR_INT2	Unused in AVR32UC
9	36	RSR_INT3	Unused in AVR32UC
10	40	RSR_EX	Unused in AVR32UC
11	44	RSR_NMI	Unused in AVR32UC
12	48	RSR_DBG	Return Status Register for Debug mode
13	52	RAR_SUP	Unused in AVR32UC
14	56	RAR_INT0	Unused in AVR32UC
15	60	RAR_INT1	Unused in AVR32UC
16	64	RAR_INT2	Unused in AVR32UC
17	68	RAR_INT3	Unused in AVR32UC
18	72	RAR_EX	Unused in AVR32UC
19	76	RAR_NMI	Unused in AVR32UC
20	80	RAR_DBG	Return Address Register for Debug mode
21	84	JECR	Unused in AVR32UC
22	88	JOSP	Unused in AVR32UC
23	92	JAVA_LV0	Unused in AVR32UC
24	96	JAVA_LV1	Unused in AVR32UC
25	100	JAVA_LV2	Unused in AVR32UC
26	104	JAVA_LV3	Unused in AVR32UC
27	108	JAVA_LV4	Unused in AVR32UC

Table 5-4. Priority and Handler Addresses for Events

Priority	Handler Address	Name	Event source	Stored Return Address
1	0x80000000	Reset	External input	Undefined
2	Provided by OCD system	OCD Stop CPU	OCD system	First non-completed instruction
3	EVBA+0x00	Unrecoverable exception	Internal	PC of offending instruction
4	EVBA+0x04			
5	EVBA+0x08	Bus error data fetch	Data bus	First non-completed instruction
6	EVBA+0x0C	Bus error instruction fetch	Data bus	First non-completed instruction
7	EVBA+0x10	NMI	External input	First non-completed instruction
8	Autovectored	Interrupt 3 request	External input	First non-completed instruction
9	Autovectored	Interrupt 2 request	External input	First non-completed instruction
10	Autovectored	Interrupt 1 request	External input	First non-completed instruction
11	Autovectored	Interrupt 0 request	External input	First non-completed instruction
12	EVBA+0x14	Instruction Address	CPU	PC of offending instruction
13	EVBA+0x50			
14	EVBA+0x18			
15	EVBA+0x1C	Breakpoint	OCD system	First non-completed instruction
16	EVBA+0x20	Illegal Opcode	Instruction	PC of offending instruction
17	EVBA+0x24	Unimplemented instruction	Instruction	PC of offending instruction
18	EVBA+0x28	Privilege violation	Instruction	PC of offending instruction
19	EVBA+0x2C	Floating-point	UNUSED	
20	EVBA+0x30	Coprocessor absent	Instruction	PC of offending instruction
21	EVBA+0x100	Supervisor call	Instruction	PC(Supervisor Call) +2
22	EVBA+0x34	Data Address (Read)	CPU	PC of offending instruction
23	EVBA+0x38	Data Address (Write)	CPU	PC of offending instruction
24	EVBA+0x60			
25	EVBA+0x70			
26	EVBA+0x3C			
27	EVBA+0x40			
28	EVBA+0x44			

7. Boot Sequence

This chapter summarizes the boot sequence of the UC3D. The behavior after power-up is controlled by the Power Manager. For specific details, refer to the Power Manager chapter.

7.1 Starting of Clocks

After power-up, the device will be held in a reset state by the Power-On Reset circuitry for a short time to allow the power to stabilize throughout the device. After reset, the device will use the System RC Oscillator (RCSYS) as clock source.

On system start-up, all clocks to all modules are running. No clocks have a divided frequency; all parts of the system receive a clock with the same frequency as the System RC Oscillator.

7.2 Fetching of Initial Instructions

After reset has been released, the AVR32UC CPU starts fetching instructions from the reset address, which is 0x80000000. This address points to the first address in the internal Flash.

The code read from the internal Flash is free to configure the system to divide the frequency of the clock routed to some of the peripherals, and to gate the clocks to unused peripherals.

8. Electrical Characteristics

8.1 Disclaimer

All values in this chapter are preliminary and subject to change without further notice.

8.2 Absolute Maximum Ratings*

Table 8-1. Absolute Maximum Ratings

Operating temperature ..... -40°C to +85°C
Storage temperature ..... -60°C to +150°C
Voltage on input pins (except for 5V pins) with respect to ground .....-0.3V to V_{VDD}[2]+0.3V
Voltage on 5V tolerant[1] pins with respect to ground .....-0.3V to 5.5V
Total DC output current on all I/O pins - VDDIO 152mA
Total DC output current on all I/O pins - VDDANA..... 152mA
Maximum operating voltage VDDCORE..... 1.95V
Maximum operating voltage VDDIO, VDDIN 3.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. 5V tolerant pins, see Section 3.2 "Peripheral Multiplexing on I/O lines" on page 8

2. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3.2 on page 8 for details.

8.3 Supply Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified and are certified for a junction temperature up to T_J = 100°C.

Table 8-2. Supply Characteristics

Symbol	Parameter	Voltage		
		Min	Max	Unit
V_{VDDIO}	DC supply peripheral I/Os	3.0	3.6	V
V_{VDDIN}	DC supply internal regulator, 3.3V single supply mode	3.0	3.6	V
$V_{VDDCORE}$	DC supply core	1.65	1.95	V
V_{VDDANA}	Analog supply voltage	3.0	3.6	V
$V_{ADVREFP}$	Analog reference voltage	2.6	V_{VDDANA}	V

8.4 Maximum Clock Frequencies

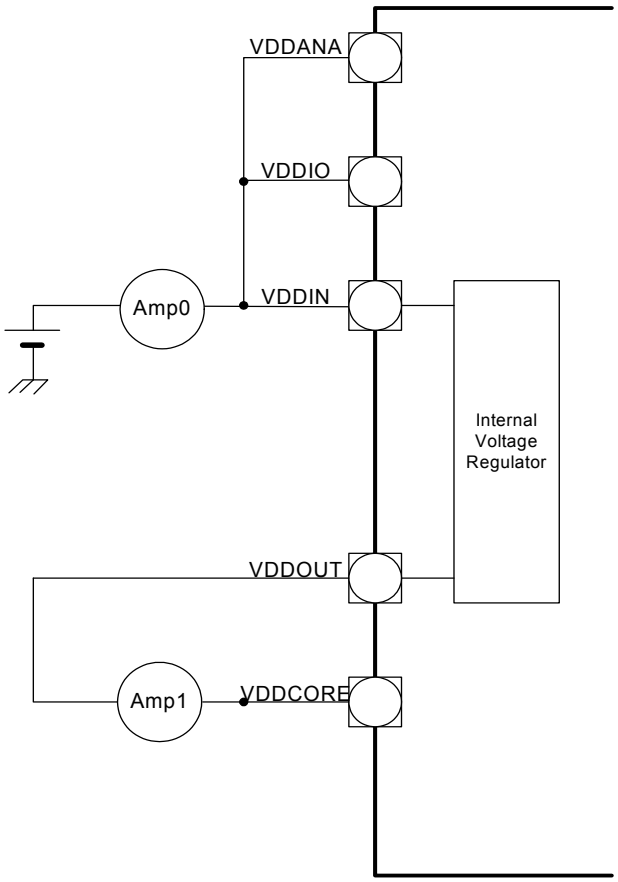
These parameters are given in the following conditions:

- $V_{VDDCORE}$ = 1.65 to 1.95V

Table 8-4. Power Consumption for Different Operating Modes

Mode	Conditions		Consumption Typ	Unit
Active	- CPU running a recursive Fibonacci Algorithm from flash and clocked from PLL0 at f MHz. - Voltage regulator is on. - XIN0: external clock. - All peripheral clocks activated with a division by 4. - GPIOs are inactive with internal pull-up, JTAG unconnected with external pull-up and Input pins are connected to GND		0.3105xf(MHz) + 0.2707	mA/MHz
	Same conditions at 48MHz		15.17	mA
Idle	See Active mode conditions		0.1165xf(MHz) + 0.1457	mA/MHz
	Same conditions at 48MHz		5.74	mA
Frozen	See Active mode conditions		0.0718xf(MHz) + 0.0903	mA/MHz
	Same conditions at 48MHz		3.54	mA
Standby	See Active mode conditions		0.0409xf(MHz) + 0.0935	mA/MHz
	Same conditions at 48MHz		2.06	mA
Stop	- CPU running in sleep mode - XIN0, Xin1 and XIN32 are stopped. - All peripheral clocks are desactived. - GPIOs are inactive with internal pull-up, JTAG unconnected with external pull-up and Input pins are connected to GND.	Voltage Regulator On	60	µA
		Voltage Regulator Off	51	µA
Deepstop	See Stop mode conditions	Voltage Regulator On	26	µA
		Voltage Regulator Off	17	µA
Static	See Stop mode conditions	Voltage Regulator On	13	µA
		Voltage Regulator Off	3.5	µA

Figure 8-1. Measurement Schematic, External Core Supply



8.5.1 Peripheral Power Consumption

The values in Table 8-5 are measured values of power consumption under the following conditions.

- Operating conditions external core supply (Figure 8-1)
  - V_{VDDIN} = 3.3V
  - $V_{VDDCORE}$ = 1.8V, supplied by the internal regulator
  - Corresponds to the 3.3V + 1.8V dual supply mode , please refer to the Supply and Startup Considerations section for more details
- T_A = 25°C
- Oscillators
  - OSC0 on external clock running
  - PLL running at 48MHz with OSC0 as reference
- Clocks
  - OSC0 external clock used as main clock source
  - CPU, HSB, and PB clocks undivided

- I/Os are inactive with internal pull-up

Consumption idle is the added current consumption when turning the module clock on and the module is uninitialized. Consumption active is the added current consumption when the module clock is turned on and when the module is doing a typical set of operations.

Table 8-5. Typical Current Consumption by Peripheral

Peripheral	Typ Consumption Active	Unit
ADCIFD[1]	3.6	µA/MHz
AST	4.5	
AW USART	9.8	
CAT	14	
EIC	2.3	
FREQM	1.1	
GLOC	1.3	
GPIO	10.6	
IISC	4.7	
PWMA	5.6	
SPI	6.3	
TC	7.3	
TWIM	4.5	
TWIS	2.8	
USART	3.9	
WDT	1.8	

Notes: 1. Includes the current consumption on VDDANA and ADVREFP.

8.6 I/O Pin Characteristics

Table 8-6. Normal I/O Pin Characteristics[1]

Symbol	Parameter	Condition		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance			9	15	25	kOhm
V_{IL}	Input low-level voltage	V_{VDD} = 3.0V	[3]	-0.3		+0.8	V
			[4]	-0.3		+0.4	V
V_{IH}	Input high-level voltage	V_{VDD} = 3.6V	[3]	+2		V_{VDD} + 0.3	V
			[4]	+1.6		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage	V_{VDD} = 3.0V, I_{OL} = 4mA				0.4	V
V_{OH}	Output high-level voltage	V_{VDD} = 3.0V, I_{OH} = 4mA		V_{VDD} - 0.4			V

Table 8-6. Normal I/O Pin Characteristics[1]

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{OL}	Output low-level current	V_{VDD} = 3.0V	[5]			4	mA
			[6]			8	mA
I_{OH}	Output high-level current	V_{VDD} = 3.0V	[5]			4	mA
			[6]			8	mA
F_{MAX}	Output frequency[2]	V_{VDD} = 3.0V, load = 10 pF	[5]			195	MHz
			[6]			348	MHz
		V_{VDD} = 3.0V, load = 30 pF	[5]			78	MHz
			[6]			149	MHz
t_{RISE}	Rise time[2]	V_{VDD} = 3.0V, load = 10 pF	[5]			2.21	ns
			[6]			1.26	ns
		V_{VDD} = 3.0V, load = 30 pF	[5]			5.45	ns
			[6]			2.88	ns
t_{FALL}	Fall time[2]	V_{VDD} = 3.0V, load = 10 pF	[5]			2.57	ns
			[6]			1.44	ns
		V_{VDD} = 3.0V, load = 30 pF	[5]			6.41	ns
			[6]			3.35	ns
I_{LEAK}	Input leakage current	Pull-up resistors disabled				1	µA
C_{IN}	Input capacitance,	[7]			2		pF
		PA09, PA10			16.5		pF
		PA11, PA12, PA18, PA19			18.5		pF
		PB14, PB15			5		pF

Notes:
1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3.2 on page 8 for details.
2. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.
3. This applies to all normal drive pads except PB13, PB17 and PB18.
4. This applies to PB13, PB17 and PB18 pads only.
5. This applies to all normal drive pad except PA00, PA01, PA02, PA03, PA04, PA05, PA06, PA07, PA08, PA09, PA10, PA11, PA12, PA13, PA18, PA19, PA27, PA30, PA31, PB13, PB16 and RESET_N.
6. This applies to PA00, PA01, PA02, PA03, PA04, PA05, PA06, PA07, PA08, PA09, PA10, PA11, PA12, PA13, PA18, PA19, PA27, PA30, PA31, PB13, PB16 and RESET_N pads only.
7. This applies to all normal drive pads except PA09, PA10, PA11, PA12, PA18, PA19, PB14, PB15.

Table 8-7. High-drive I/O Pin Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance		9	15	25	kOhm
V_{IL}	Input low-level voltage	V_{VDD} = 3.0V	-0.3		+0.8	V
V_{IH}	Input high-level voltage	V_{VDD} = 3.6V	+2		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage	V_{VDD} = 3.0V, I_{OL} = 6mA			0.4	V

8.7 Oscillator Characteristics

8.7.1 Oscillator 0 (OSC0) Characteristics

8.7.1.1 Digital Clock Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN.

Table 8-10. Digital Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CPXIN}	XIN clock frequency				50	MHz
t_{CPXIN}	XIN clock duty cycle		40		60	%

8.7.1.2 Crystal Oscillator Characteristics

The following table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT as shown in Figure 8-2. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can be found in the crystal datasheet. The capacitance of the external capacitors (C_{LEXT}) can then be computed as follows:

$$C_{LEXT} = 2(C_L - C_i) - C_{PCB}$$

where C_{PCB} is the capacitance of the PCB.

Table 8-11. Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal oscillator frequency		0.4		20	MHz
C_L	Crystal load capacitance		6		18	pF
C_i	Internal equivalent load capacitance			1.7		pF
$t_{STARTUP}$	Startup time	400 KHz Resonator SCIF.OSCCTRL.GAIN = 0[1]		198		µs
		2 MHz Quartz SCIF.OSCCTRL.GAIN = 0[1]		4666		
		8 MHz Quartz SCIF.OSCCTRL.GAIN = 1[1]		975		
		12 MHz Quartz SCIF.OSCCTRL.GAIN = 2[1]		615		
		16 MHz Quartz SCIF.OSCCTRL.GAIN = 2[1]		1106		
		20 MHz Quartz SCIF.OSCCTRL.GAIN = 3[1]		1109		

Notes: 1. Please refer to the SCIF chapter for details.

Table 8-18. Flash Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{FPP}	Page programming time	f_{CLK_HSB}= 48MHz		5		ms
T_{FPE}	Page erase time			5		
T_{FFP}	Fuse programming time			1		
T_{FEA}	Full chip erase time (EA)			6		
T_{FCE}	JTAG chip erase time (CHIP_ERASE)	f_{CLK_HSB}= 115kHz		310		

Table 8-19. Flash Endurance and Data Retention

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{FARRAY}	Array endurance (write/page)		100k			cycles
N_{FFUSE}	General Purpose fuses endurance (write/bit)		10k			cycles
t_{RET}	Data retention		15			years

8.9 Analog Characteristics

8.9.1 Voltage Regulator Characteristics

8.9.1.1 Electrical Characteristics

Table 8-20. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{VDDIN}	Input voltage range		3	3.3	3.6	V
$V_{VDDCORE}$	Output voltage	V_{VDDIN} >= 3V	1.75	1.8	1.85	V
	Output voltage accuracy	I_{OUT} = 0.1mA to 100mA, V_{VDDIN}>3V		2		%
I_{OUT}	DC output current	V_{VDDIN}=3.3V			100	mA
I_{VREG}	Static current of internal regulator	Low power mode		10		µA

8.9.1.2 Decoupling Requirements

Table 8-21. Decoupling Requirements

Symbol	Parameter	Condition	Typ	Techno.	Units
C_{IN1}	Input regulator capacitor 1		1	NPO	nF

Figure 8-4. MCU Cold Start-Up RESET_N Externally Driven

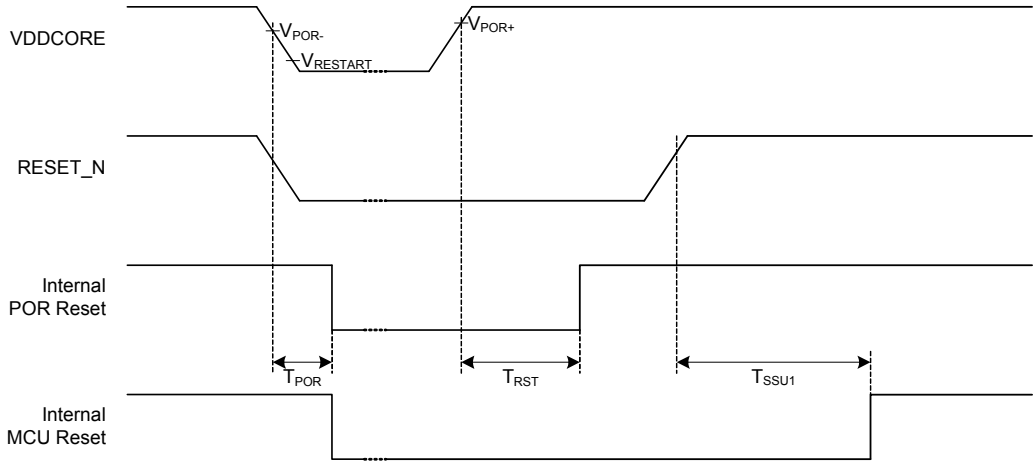
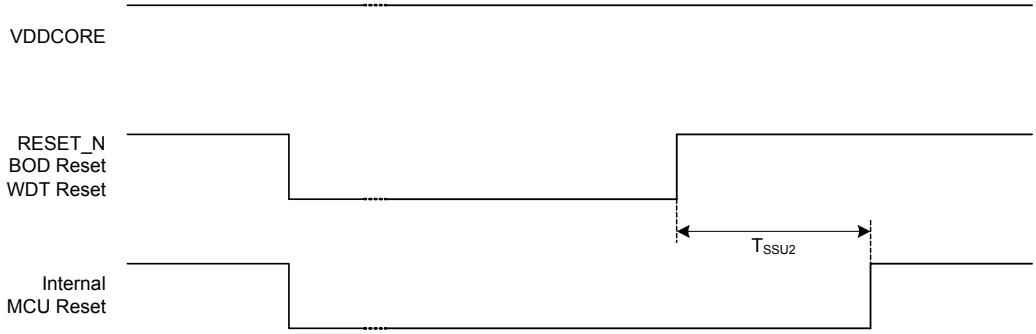


Figure 8-5. MCU Hot Start-Up

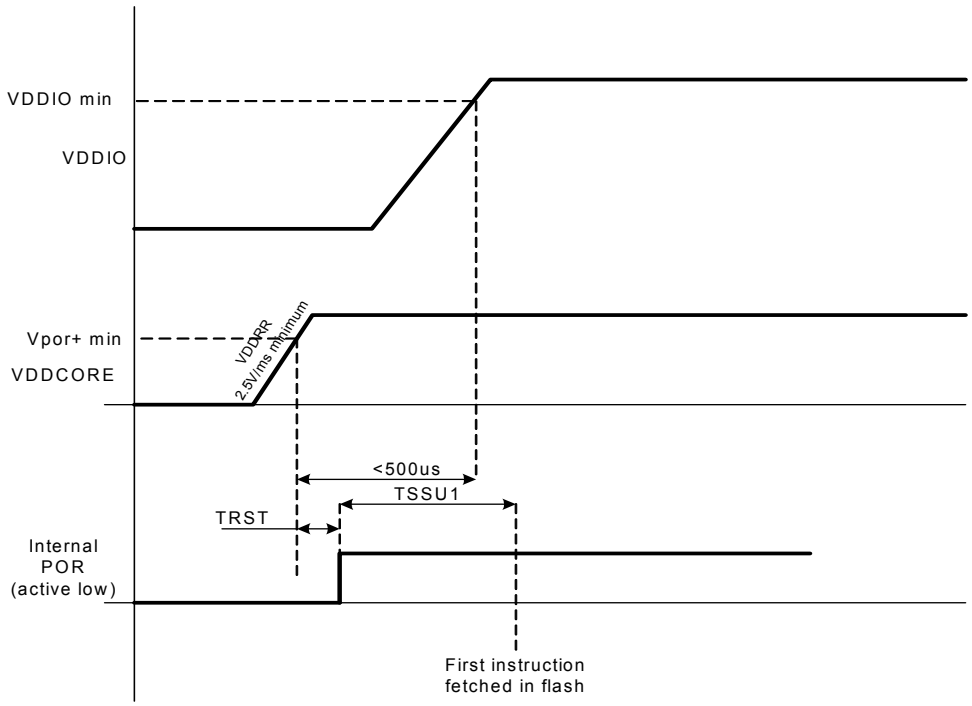


In dual supply configuration, the power up sequence must be carefully managed to ensure a safe startup of the device in all conditions.

The power up sequence must ensure that the internal logic is safely powered when the internal reset (Power On Reset) is released and that the internal Flash logic is safely powered when the CPU fetch the first instructions.

Therefore VDDCORE rise rate (VDDRR) must be equal or superior to 2.5V/ms and VDDIO must reach VDDIO mini value before 500 us (< TRST + TSSU1) after VDDCORE has reached V_{POR+} min value.

Figure 8-6. Dual Supply Configuration



8.9.5 RESET_N Characteristics

Table 8-30. RESET_N Waveform Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{RESET}	RESET_N minimum pulse width		10			ns

8.10 USB Transceiver Characteristics

8.10.1 Electrical Characteristics

Electrical Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{EXT}	Recommended External USB Series Resistor	In series with each USB pin with ±5%		39		Ω

The USB on-chip buffers comply with the Universal Serial Bus (USB) v2.0 standard. All AC parameters related to these buffers can be found within the USB 2.0 electrical specifications.

Figure 9-3. QFN-48 Package Drawing

Table 9-8. Device and Package Maximum Weight

Weight	100 mg

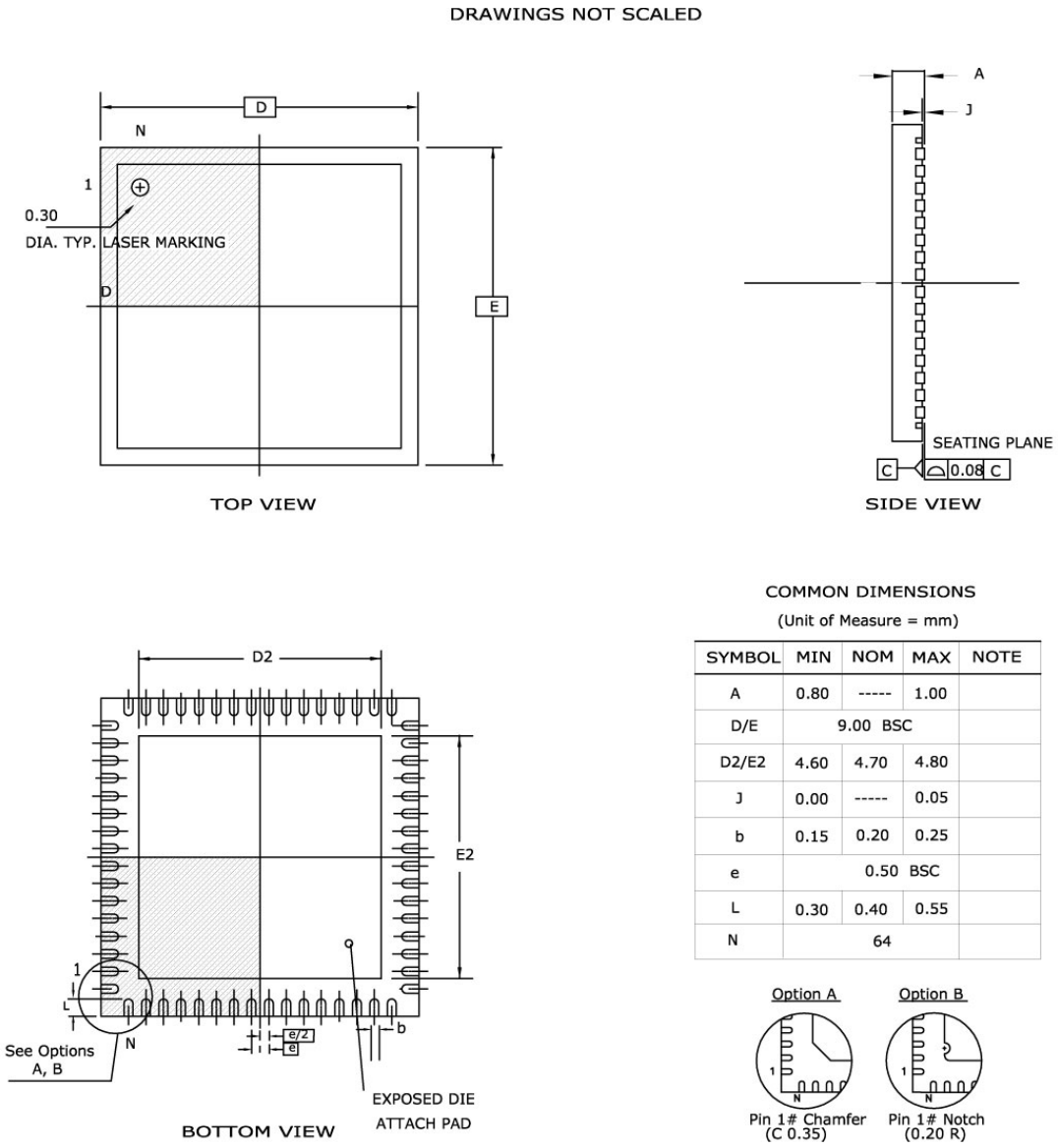
Table 9-9. Package Characteristics

Moisture Sensitivity Level	Jedec J-STD-20D-MSL3

Table 9-10. Package Reference

JEDEC Drawing Reference	M0-220
JESD97 Classification	e3

Figure 9-4. QFN-64 package drawing



SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
D/E		9.00 BSC		
D2/E2	4.60	4.70	4.80	
J	0.00	-----	0.05	
b	0.15	0.20	0.25	
e		0.50 BSC		
L	0.30	0.40	0.55	
N		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Table 9-11. Device and Package Maximum Weight

Weight	200 mg

Table 9-12. Package Characteristics

Moisture Sensitivity Level	Jedec J-STD-20D-MSL3

Table 9-13. Package Reference

JEDEC Drawing Reference	M0-220
JESD97 Classification	e3

11.1.2 TWIS

1. **Clearing the NAK bit before the BTF bit is set locks up the TWI bus**
   When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.
   Fix/Workaround
   Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

11.1.3 PWMA

1. **The SR.READY bit cannot be cleared by writing to SCR.READY**
   The Ready bit in the Status Register will not be cleared when writing a one to the corresponding bit in the Status Clear register. The Ready bit will be cleared when the Busy bit is set.
   Fix/Workaround
   Disable the Ready interrupt in the interrupt handler when receiving the interrupt. When an operation that triggers the Busy/Ready bit is started, wait until the ready bit is low in the Status Register before enabling the interrupt.

11.2 Rev. B

11.2.1 Power Manager

1. **TWIS may not wake the device from sleep mode**
   If the CPU is put to a sleep mode (except Idle and Frozen) directly after a TWI Start condition, the CPU may not wake upon a TWIS address match. The request is NACKed.
   Fix/Workaround
   When using the TWI address match to wake the device from sleep, do not switch to sleep modes deeper than Frozen. Another solution is to enable asynchronous EIC wake on the TWIS clock (TWCK) or TWIS data (TWD) pins, in order to wake the system up on bus events.

11.2.2 SPI

1. **SPI disable does not work in SLAVE mode**
   SPI disable does not work in SLAVE mode.
   Fix/Workaround
   Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

2. **PCS field in receive data register is inaccurate**
   The PCS field in the SPI_RDR register does not accurately indicate from which slave the received data is read.
   Fix/Workaround
   None.

3. **SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0**
   When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
   Fix/Workaround
   Disable mode fault detection by writing a one to MR.MODFDIS.

Fix/Workaround
Disable the PDCA, add two NOPs, and disable the SPI. To continue the transfer, enable the SPI and PDCA.

8. **SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0**
When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
Fix/Workaround
When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

9. **I/O Pins**

10. **Current leakage through pads PA09, PA10 and PB16**
Pads PA09 (TWI), PA10 (TWI) and PB16 (USB VBUS) are not fully 5V tolerant. A leakage current can be observed when a 5V voltage is applied onto those pads inputs. Their behavior is normal at 3.3V
Fix/Workaround
None for pads PA09 and PA10. A voltage divider can be used for PB16 (VBUS) to bring the input voltage down into the 3.3V range.

11. **Current leakage through pads PB13, PB17 and PB18**
For applications in which UC3D is considered as a drop in replacement solution to UC3B, pads PB13, PB17 and PB18 can no longer be used as VDDCORE supply pins.Maintaining a 1.8V voltage on those inputs will however lead to a current over consumption through the pins.
Fix/Workaround
Do not connect PB13, PB17 and PB18 when using UC3D as a drop in replacement for a UC3B specific application.

12. **IO drive strength mismatch with UC3B specification for pads PA11, PA12, PA18 and PA19**
For applications in which UC3D is considered as a drop in replacement solution to UC3B, GPIOs PA11, PA12, PA18 and PA19 are not completely compatible in terms of drive strength. Those pads have a 8 mA current capability on UC3B, while this is limited to 4 mA in UC3D.
Fix/Workaround
None.

13. **WDT**

14. **Clearing the Watchdog Timer (WDT) counter in second half of timeout period will issue a Watchdog reset**
If the WDT counter is cleared in the second half of the timeout period, the WDT will immediately issue a Watchdog reset.
Fix/Workaround
Use twice as long timeout period as needed and clear the WDT counter within the first half of the timeout period. If the WDT counter is cleared after the first half of the timeout period, you will get a Watchdog reset immediately. If the WDT counter is not cleared at all, the time before the reset will be twice as long as needed.