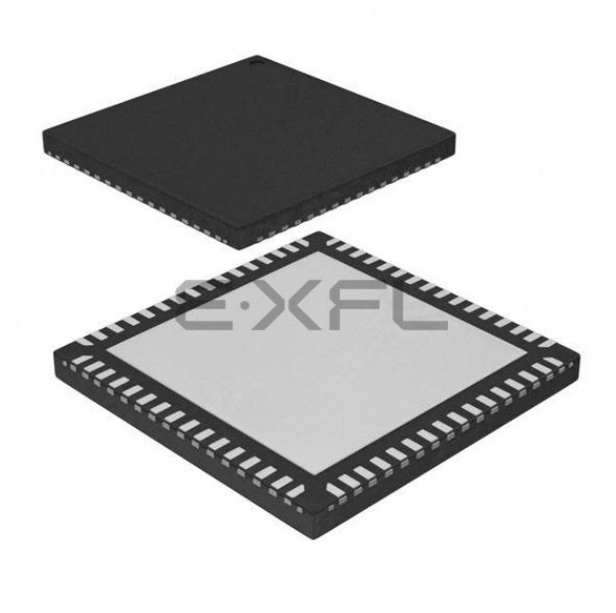

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atuc128d3-z2ut

1. Description

The UC3D is a complete System-On-Chip microcontroller based on the AVR32UC RISC processor running at frequencies up to 48MHz. AVR32UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density, and high performance.

The processor implements a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems.

Higher computation capability is achieved using a rich set of DSP instructions.

The Peripheral Direct Memory Access (DMA) controller enables data transfers between peripherals and memories without processor involvement. The Peripheral DMA controller drastically reduces processing overhead when transferring continuous and large data streams.

The Power Manager improves design flexibility and security. Power monitoring is supported by on-chip Power-On Reset (POR), and Brown-Out Detector (BOD). The device features several oscillators, such as Oscillator 0 (OSC0), 32 KHz Oscillator and system RC oscillator (RCSYS), and two Phase Lock Loop (PLL). Either of these oscillators/PLLs can be used as source for the system clock.

The Watchdog Timer (WDT) will reset the device unless it is periodically serviced by the software. This allows the device to recover from a condition that has caused the system to be unstable.

The Asynchronous Timer (AST) combined with the 32KHz crystal oscillator supports powerful real-time clock capabilities, with a maximum timeout of up to 136 years. The AST can operate in counter mode or calendar mode. The 32KHz crystal oscillator can operate in a 1- or 2-pin mode, trading pin usage and accuracy.

The Frequency Meter (FREQM) allows accurate measuring of a clock frequency by comparing it to a known reference clock.

The Full-Speed USB 2.0 Device interface supports several USB Classes at the same time thanks to the rich End-Point configuration.

The device includes three identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing, and pulse width modulation.

The Pulse Width Modulation controller (PWMA) provides 12-bit PWM channels which can be synchronized and controlled from a common timer. Seven PWM channels are available, enabling applications that require multiple PWM outputs, such as LCD backlight control. The PWM channels can operate independently, with duty cycles set independently from each other, or in interlinked mode, with multiple channels changed at the same time.

The UC3D also features many communication interfaces for communication intensive applications. In addition to standard serial interfaces like USART, SPI or TWI, USB is available. The USART supports different communication modes, like SPI mode.

A general purpose 8-channel ADC is provided; It features a fully configurable sequencer that handles many conversions. Window Mode allows each ADC channel to be used like a simple Analog Comparator.

The Inter-IC Sound controller (IISC) provides easy access to digital audio interfaces following I2S stereo standard.

Table 3-1. Multiplexed Signals on I/O Pins

48-pin Package	64-pin Package	PIN	GPIO	Supply	Pad Type	GPIO Function				Other Functions
						A	B	C	D	
2	2	PB12	44	VDDIO	Normal I/O	SPI - NPCS[0]	IISC - IMCK	GLOC - OUT[0]		JTAG-TCK
6	8	PB13	45	VDDIO	Normal I/O	CAT - SYNC	SCIF - GCLK[2]	GLOC - IN[4]	CAT - CSA[2]	
38	50	PB14	46	VDDIO	Normal I/O	USBC - DP	USART0 - RXD	GLOC - OUT[2]	CAT - CSA[13]	
39	51	PB15	47	VDDIO	Normal I/O	USBC - DM	USART0 - TXD	GLOC - IN[12]	CAT - CSB[13]	
40	52	PB16	48	VDDIO	Input only, 5V tolerant	USBC - VBUS		GLOC - IN[10]		USB-VBUS
41	53	PB17	49	VDDIO	Normal I/O	IISC - ISDO	USART0 - RTS	GLOC - IN[13]		
42	56	PB18	50	VDDIO	Normal I/O	IISC - ISDI	CAT - SYNC	GLOC - OUT[3]	CAT - CSA[15]	

See Section 4. for a description of the various peripheral signals.

Refer to "Electrical Characteristics" on page 37 for a description of the electrical properties of the pad types used.

3.2.2 Peripheral Functions

Each GPIO line can be assigned to one of several peripheral functions. The following table describes how the various peripheral functions are selected. The last listed function has priority in case multiple functions are enabled.

Table 3-2. Peripheral Functions

Function	Description
A	GPIO peripheral selection A
B	GPIO peripheral selection B
C	GPIO peripheral selection C
D	GPIO peripheral selection D

3.2.3 JTAG Port Connections

If the JTAG is enabled, the JTAG will take control over a number of pins, irrespective of the I/O Controller configuration.

Table 3-3. JTAG Pinout

48-pin or 64-pin Package	Pin Name	JTAG Pin
2	PB12	TCK
5	PA02	TMS
4	PA01	TDO
3	PA00	TDI

3.2.4 Oscillator Pinout

The oscillators are not mapped to the normal GPIO functions and their muxings are controlled by registers in the System Control Interface (SCIF). Please refer to the SCIF chapter for more information about this.

Table 3-4. Oscillator Pinout

48-pin Package	64-pin Package	Pin	Oscillator Function
30	39	PA18	XIN0
31	40	PA19	XOUT0
22	30	PA11	XIN32
23	31	PA12	XOUT32

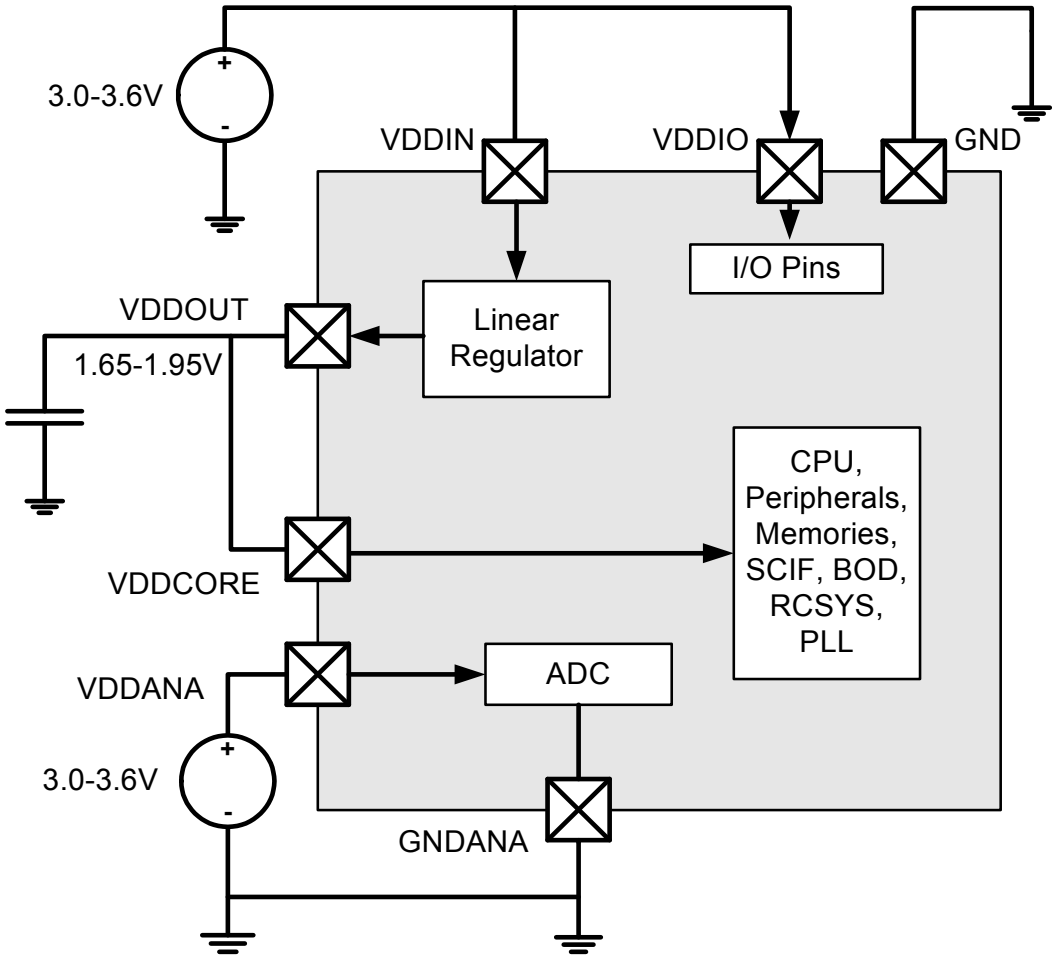
3.2.5 Other Functions

The functions listed in Table 3-5 are not mapped to the normal GPIO functions.The aWire DATA pin will only be active after the aWire is enabled. The aWire DATAOUT pin will only be active after the aWire is enabled and the 2-pin mode command has been sent.

Table 3-5. Other Functions

48-Pin Package	64-Pin Package	Pin	Function
47	63	RESET_N	aWire DATA
2	2	PB12	aWire DATAOUT

Figure 4-2. 3.3V Single Power Supply mode



The following table shows the instructions with support for unaligned addresses. All other instructions require aligned addresses.

Table 5-1. Instructions with Unaligned Reference Support

Instruction	Supported Alignment
ld.d	Word
st.d	Word

5.3.2.4 *Unimplemented Instructions*

The following instructions are unimplemented in AVR32UC, and will cause an Unimplemented Instruction Exception if executed:

- All SIMD instructions
- All coprocessor instructions if no coprocessors are present
- retj, incjosp, popjc, pushjc
- tlbr, tlbs, tlbw
- cache

5.3.2.5 *CPU and Architecture Revision*

Three major revisions of the AVR32UC CPU currently exist. The device described in this datasheet uses CPU revision 3.

The Architecture Revision field in the CONFIG0 system register identifies which architecture revision is implemented in a specific device.

AVR32UC CPU revision 3 is fully backward-compatible with revisions 1 and 2, ie. code compiled for revision 1 or 2 is binary-compatible with revision 3 CPUs.

Debug state can be entered as described in the *AVR32UC Technical Reference Manual*.

Debug state is exited by the *retd* instruction.

5.4.4 System Registers

The system registers are placed outside of the virtual memory space, and are only accessible using the privileged *mfsr* and *mtsr* instructions. The table below lists the system registers specified in the AVR32 architecture, some of which are unused in AVR32UC. The programmer is responsible for maintaining correct sequencing of any instructions following a *mtsr* instruction. For detail on the system registers, refer to the *AVR32UC Technical Reference Manual*.

Table 5-3. System Registers

Reg #	Address	Name	Function
0	0	SR	Status Register
1	4	EVBA	Exception Vector Base Address
2	8	ACBA	Application Call Base Address
3	12	CPUCR	CPU Control Register
4	16	ECR	Exception Cause Register
5	20	RSR_SUP	Unused in AVR32UC
6	24	RSR_INT0	Unused in AVR32UC
7	28	RSR_INT1	Unused in AVR32UC
8	32	RSR_INT2	Unused in AVR32UC
9	36	RSR_INT3	Unused in AVR32UC
10	40	RSR_EX	Unused in AVR32UC
11	44	RSR_NMI	Unused in AVR32UC
12	48	RSR_DBG	Return Status Register for Debug mode
13	52	RAR_SUP	Unused in AVR32UC
14	56	RAR_INT0	Unused in AVR32UC
15	60	RAR_INT1	Unused in AVR32UC
16	64	RAR_INT2	Unused in AVR32UC
17	68	RAR_INT3	Unused in AVR32UC
18	72	RAR_EX	Unused in AVR32UC
19	76	RAR_NMI	Unused in AVR32UC
20	80	RAR_DBG	Return Address Register for Debug mode
21	84	JECR	Unused in AVR32UC
22	88	JOSP	Unused in AVR32UC
23	92	JAVA_LV0	Unused in AVR32UC
24	96	JAVA_LV1	Unused in AVR32UC
25	100	JAVA_LV2	Unused in AVR32UC
26	104	JAVA_LV3	Unused in AVR32UC
27	108	JAVA_LV4	Unused in AVR32UC

The addresses and priority of simultaneous events are shown in Table 5-4 on page 32. Some of the exceptions are unused in AVR32UC since it has no MMU, coprocessor interface, or floating-point unit.

Table 5-4. Priority and Handler Addresses for Events

Priority	Handler Address	Name	Event source	Stored Return Address
1	0x80000000	Reset	External input	Undefined
2	Provided by OCD system	OCD Stop CPU	OCD system	First non-completed instruction
3	EVBA+0x00	Unrecoverable exception	Internal	PC of offending instruction
4	EVBA+0x04			
5	EVBA+0x08	Bus error data fetch	Data bus	First non-completed instruction
6	EVBA+0x0C	Bus error instruction fetch	Data bus	First non-completed instruction
7	EVBA+0x10	NMI	External input	First non-completed instruction
8	Autovectored	Interrupt 3 request	External input	First non-completed instruction
9	Autovectored	Interrupt 2 request	External input	First non-completed instruction
10	Autovectored	Interrupt 1 request	External input	First non-completed instruction
11	Autovectored	Interrupt 0 request	External input	First non-completed instruction
12	EVBA+0x14	Instruction Address	CPU	PC of offending instruction
13	EVBA+0x50			
14	EVBA+0x18			
15	EVBA+0x1C	Breakpoint	OCD system	First non-completed instruction
16	EVBA+0x20	Illegal Opcode	Instruction	PC of offending instruction
17	EVBA+0x24	Unimplemented instruction	Instruction	PC of offending instruction
18	EVBA+0x28	Privilege violation	Instruction	PC of offending instruction
19	EVBA+0x2C	Floating-point	UNUSED	
20	EVBA+0x30	Coprocessor absent	Instruction	PC of offending instruction
21	EVBA+0x100	Supervisor call	Instruction	PC(Supervisor Call) +2
22	EVBA+0x34	Data Address (Read)	CPU	PC of offending instruction
23	EVBA+0x38	Data Address (Write)	CPU	PC of offending instruction
24	EVBA+0x60			
25	EVBA+0x70			
26	EVBA+0x3C			
27	EVBA+0x40			
28	EVBA+0x44			

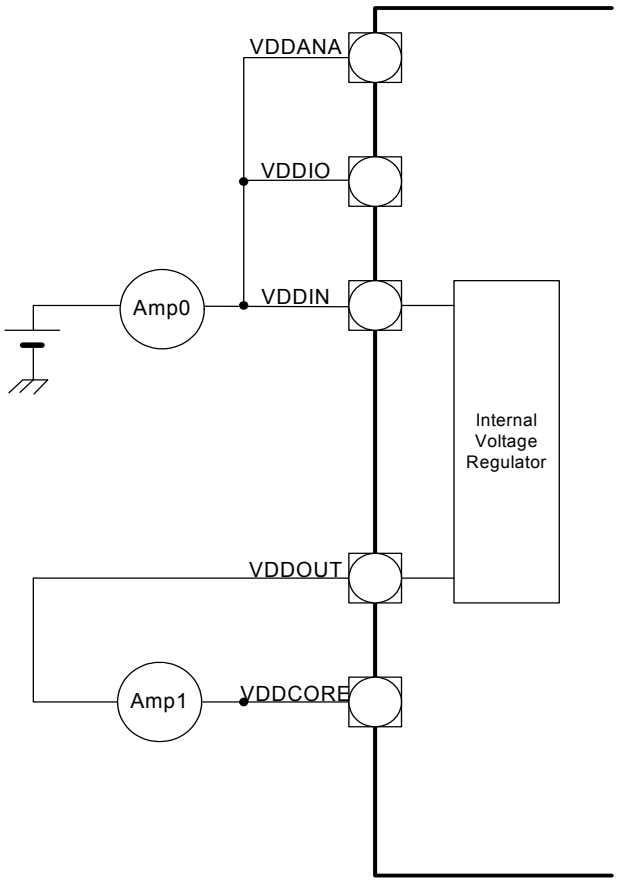
Table 6-2. Peripheral Address Mapping

0xFFFF1400	PM	Power Manager - PM
0xFFFF1800	AST	Asynchronous Timer - AST
0xFFFF1C00	WDT	Watchdog Timer - WDT
0xFFFF2000	EIC	External Interrupt Controller - EIC
0xFFFF2800	GPIO	General Purpose Input/Output Controller - GPIO
0xFFFF3000	USART0	Universal Synchronous/Asynchronous Receiver/Transmitter - USART0
0xFFFF3400	USART1	Universal Synchronous/Asynchronous Receiver/Transmitter - USART1
0xFFFF3800	USART2	Universal Synchronous/Asynchronous Receiver/Transmitter - USART2
0xFFFF3C00	SPI	Serial Peripheral Interface - SPI
0xFFFF4000	TWIM	Two-wire Master Interface - TWIM
0xFFFF4400	TWIS	Two-wire Slave Interface - TWIS
0xFFFF4800	PWMA	Pulse Width Modulation Controller - PWMA
0xFFFF4C00	IISC	Inter-IC Sound (I2S) Controller - IISC
0xFFFF5000	TC	Timer/Counter - TC
0xFFFF5400	ADCIFD	ADC controller interface - ADCIFD
0xFFFF5800	SCIF	System Control Interface - SCIF
0xFFFF5C00	FREQM	Frequency Meter - FREQM
0xFFFF6000	CAT	Capacitive Touch Module - CAT

Table 8-4. Power Consumption for Different Operating Modes

Mode	Conditions		Consumption Typ	Unit
Active	- CPU running a recursive Fibonacci Algorithm from flash and clocked from PLL0 at f MHz. - Voltage regulator is on. - XIN0: external clock. - All peripheral clocks activated with a division by 4. - GPIOs are inactive with internal pull-up, JTAG unconnected with external pull-up and Input pins are connected to GND		0.3105xf(MHz) + 0.2707	mA/MHz
	Same conditions at 48MHz		15.17	mA
Idle	See Active mode conditions		0.1165xf(MHz) + 0.1457	mA/MHz
	Same conditions at 48MHz		5.74	mA
Frozen	See Active mode conditions		0.0718xf(MHz) + 0.0903	mA/MHz
	Same conditions at 48MHz		3.54	mA
Standby	See Active mode conditions		0.0409xf(MHz) + 0.0935	mA/MHz
	Same conditions at 48MHz		2.06	mA
Stop	- CPU running in sleep mode - XIN0, Xin1 and XIN32 are stopped. - All peripheral clocks are desactived. - GPIOs are inactive with internal pull-up, JTAG unconnected with external pull-up and Input pins are connected to GND.	Voltage Regulator On	60	µA
		Voltage Regulator Off	51	µA
Deepstop	See Stop mode conditions	Voltage Regulator On	26	µA
		Voltage Regulator Off	17	µA
Static	See Stop mode conditions	Voltage Regulator On	13	µA
		Voltage Regulator Off	3.5	µA

Figure 8-1. Measurement Schematic, External Core Supply



8.5.1 Peripheral Power Consumption

The values in Table 8-5 are measured values of power consumption under the following conditions.

- Operating conditions external core supply (Figure 8-1)
  - V_{VDDIN} = 3.3V
  - $V_{VDDCORE}$ = 1.8V, supplied by the internal regulator
  - Corresponds to the 3.3V + 1.8V dual supply mode , please refer to the Supply and Startup Considerations section for more details
- T_A = 25°C
- Oscillators
  - OSC0 on external clock running
  - PLL running at 48MHz with OSC0 as reference
- Clocks
  - OSC0 external clock used as main clock source
  - CPU, HSB, and PB clocks undivided

Table 8-21. Decoupling Requirements

Symbol	Parameter	Condition	Typ	Techno.	Units
C_{IN2}	Input regulator capacitor 2		4.7	X7R	nF
C_{OUT1}	Output regulator capacitor 1		470	NPO	nF
C_{OUT2}	Output regulator capacitor 2		2.2	X7R	µF

8.9.2 ADC Characteristics

Table 8-22. Channel Conversion Time and ADC Clock

Parameter	Conditions	Min.	Typ.	Max.	Unit
ADC Clock Frequency	10-bit resolution mode			5	MHz
	8-bit resolution mode			8	MHz
Startup Time	Return from Idle Mode			20	µs
Track and Hold Acquisition Time		600			ns
Conversion Time	ADC Clock = 5 MHz			2	µs
	ADC Clock = 8 MHz			1.25	µs
Throughput Rate	ADC Clock = 5 MHz			384 (1)	kSPS
	ADC Clock = 8 MHz			533 (2)	kSPS

1. Corresponds to 13 clock cycles: 3 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.
2. Corresponds to 15 clock cycles: 5 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.

Table 8-23. ADC Power Consumption

Parameter	Conditions	Min.	Typ.	Max.	Unit
Current Consumption on VDDANA (1)	On 13 samples with ADC clock = 5 MHz			1.25	mA

1. Including internal reference input current

Table 8-24. Analog Inputs

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range		0		VDDANA	V
Input Leakage Current				1	µA
Input Capacitance			7		pF
Input Resistance			370	810	Ohm

Table 8-25. Transfer Characteristics in 8-bit mode

Parameter	Conditions	Min.	Typ.	Max.	Unit
Resolution			8		Bit
Absolute Accuracy	ADC Clock = 5 MHz			0.8	LSB
	ADC Clock = 8 MHz			1.5	LSB
Integral Non-linearity	ADC Clock = 5 MHz		0.35	0.5	LSB
	ADC Clock = 8 MHz		0.5	1.0	LSB

8.9.4 Reset Sequence

Table 8-29. Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDRR}	VDDCORE rise rate to ensure power-on-reset		2.5			V/ms
V_{DDFR}	VDDCORE fall rate to ensure power-on-reset		0.01		400	V/ms
V_{POR+}	Rising threshold voltage: voltage up to which device is kept under reset by POR on rising VDDCORE	Rising VDDCORE: $V_{RESTART}$ -> V_{POR+}	1.4	1.55	1.65	V
V_{POR-}	Falling threshold voltage: voltage when POR resets device on falling VDDCORE	Falling VDDCORE: 1.8V -> V_{POR+}	1.2	1.3	1.4	V
$V_{RESTART}$	On falling VDDCORE, voltage must go down to this value before supply can rise again to ensure reset signal is released at V_{POR+}	Falling VDDCORE: 1.8V -> $V_{RESTART}$	-0.1		0.5	V
T_{POR}	Minimum time with VDDCORE < V_{POR-}	Falling VDDCORE: 1.8V -> 1.1V		15		µs
T_{RST}	Time for reset signal to be propagated to system			200	400	µs
T_{SSU1}	Time for Cold System Startup: Time for CPU to fetch its first instruction (RCosc not calibrated)		480		960	µs
T_{SSU2}	Time for Hot System Startup: Time for CPU to fetch its first instruction (RCosc calibrated)			420		µs

Figure 8-3. MCU Cold Start-Up RESET_N tied to VDDIN

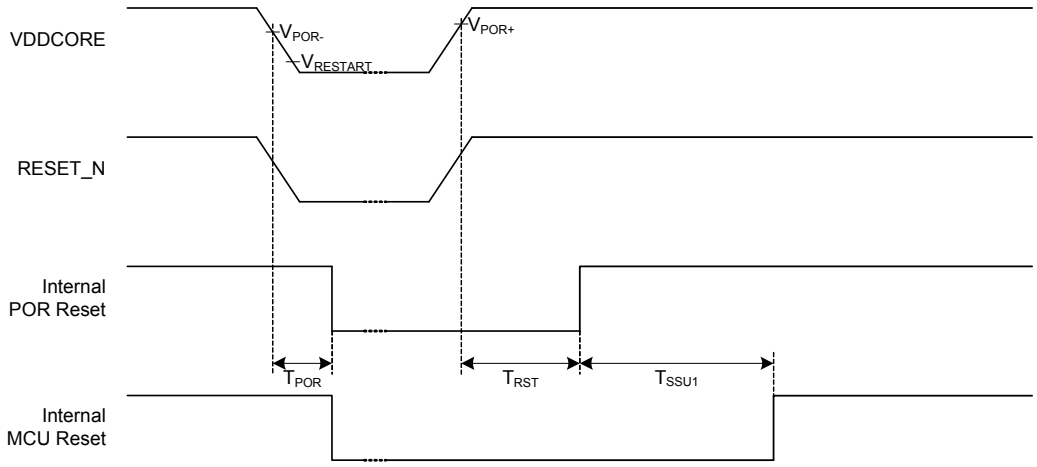


Figure 8-4. MCU Cold Start-Up RESET_N Externally Driven

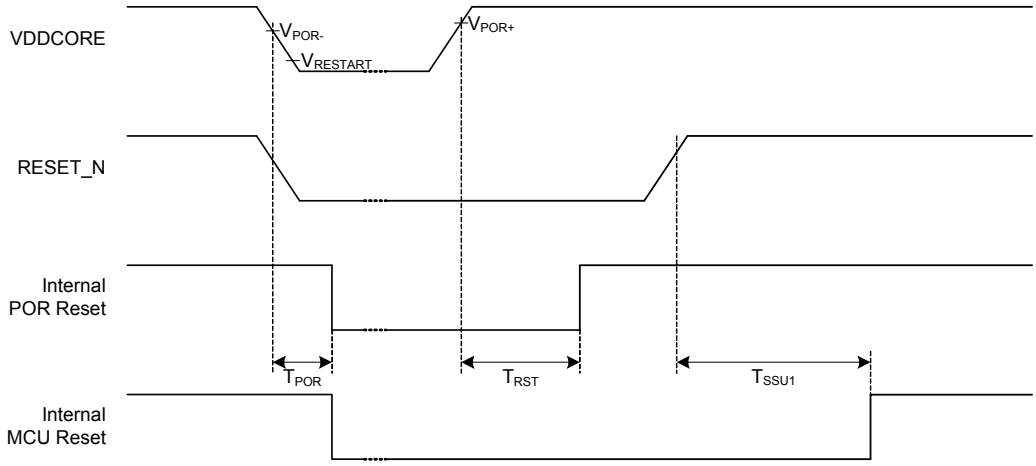
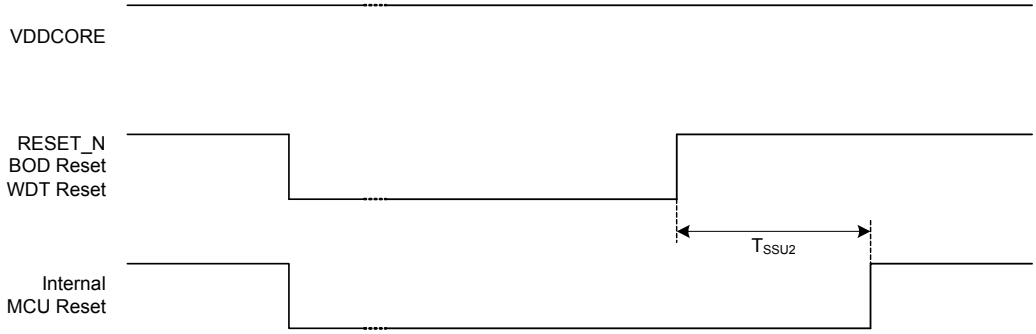


Figure 8-5. MCU Hot Start-Up



In dual supply configuration, the power up sequence must be carefully managed to ensure a safe startup of the device in all conditions.

The power up sequence must ensure that the internal logic is safely powered when the internal reset (Power On Reset) is released and that the internal Flash logic is safely powered when the CPU fetch the first instructions.

Therefore VDDCORE rise rate (VDDRR) must be equal or superior to 2.5V/ms and VDDIO must reach VDDIO mini value before 500 us (< TRST + TSSU1) after VDDCORE has reached V_{POR+} min value.

9. Mechanical Characteristics

9.1 Thermal Considerations

9.1.1 Thermal Data

Table 9-1 summarizes the thermal resistance data depending on the package.

Table 9-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP48	65.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP48	23.4	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN48	29.2	°C/W
θ_{JC}	Junction-to-case thermal resistance		QFN48	2.7	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP64	63.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP64	23.0	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN64	26.9	°C/W
θ_{JC}	Junction-to-case thermal resistance		QFN64	2.7	

9.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 9-1.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 9-1.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the Section 8.5 on page 38.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

9.3 Soldering Profile

Table 9-14 gives the recommended soldering profile from J-STD-20.

Table 9-14. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150°C min, 200°C max
Temperature Maintained Above 217°C	60-150 s
Time within 5·C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25·C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

11.3 Rev. A

11.3.1 GPIO

1. **Clearing Interrupt flags can mask other interrupts**
   When clearing interrupt flags in a GPIO port, interrupts on other pins of that port, happening in the same clock cycle will not be registered.
   Fix/Workaround
   Read the PVR register of the port before and after clearing the interrupt to see if any pin change has happened while clearing the interrupt. If any change occurred in the PVR between the reads, they must be treated as an interrupt.

11.3.2 Power Manager

1. **Clock Failure Detector (CFD) can be issued while turning off the CFD**
   While turning off the CFD, the CFD bit in the Status Register (SR) can be set. This will change the main clock source to RCSYS.
   Fix/Workaround
   Solution 1: Enable CFD interrupt. If CFD interrupt is issues after turning off the CFD, switch back to original main clock source.
   Solution 2: Only turn off the CFD while running the main clock on RCSYS.

2. **Requesting clocks in idle sleep modes will mask all other PB clocks than the requested**
   In idle or frozen sleep mode, all the PB clocks will be frozen if the TWIS or the AST needs to wake the CPU up.
   Fix/Workaround
   Disable the TWIS or the AST before entering idle or frozen sleep mode.

3. **SPI**

4. **SPI disable does not work in SLAVE mode**
   SPI disable does not work in SLAVE mode.
   Fix/Workaround
   Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

5. **PCS field in receive data register is inaccurate**
   The PCS field in the SPI_RDR register does not accurately indicate from which slave the received data is read.
   Fix/Workaround
   None.

6. **SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0**
   When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
   Fix/Workaround
   Disable mode fault detection by writing a one to MR.MODFDIS.

7. **Disabling SPI has no effect on the SR.TDRE bit**
   Disabling SPI has no effect on the SR.TDRE bit whereas the write data command is filtered when SPI is disabled. Writing to TDR when SPI is disabled will not clear SR.TDRE. If SPI is disabled during a PDCA transfer, the PDCA will continue to write data to TDR until its buffer is empty, and this data will be lost.

12. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

12.1 Rev. A – 11/2009

1. Initial revision.

12.2 Rev. B – 04/2011

1. Minor.

12.3 Rev. C – 07/2011

1. Final revision.

12.4 Rev. D – 11/2011

1. Adding errata for silicon Revision C .
2. Fixed PLLOPT field description in SCIF chapter

Table of Contents