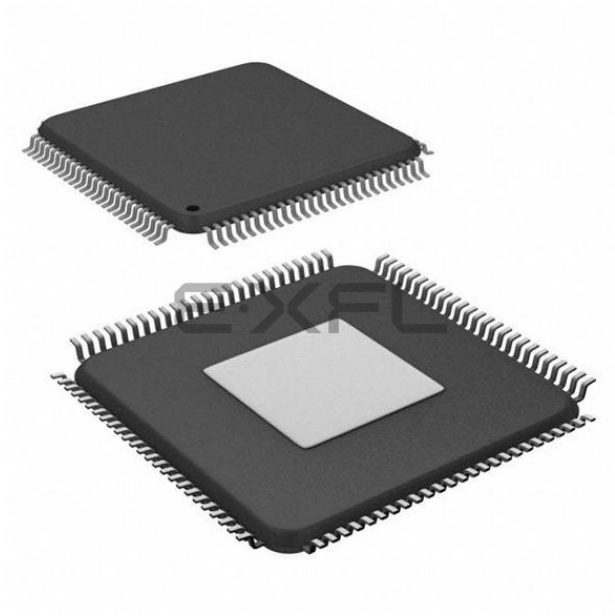
Infineon Technologies - XC2269I136F128LRAAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	128MHz
Connectivity	CANbus, EBI/EMI, FlexRay, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	90K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2269i136f128lraakxuma1

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC2269I Special Device Types

Derivative[1]	Flash Memory[2]	PSRAM DSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
XC2269I-72FxxL	576 Kbytes	64 Kbytes 24 Kbytes	CC2 CCU60/1/2/3	11 + 8	6 CAN Nodes 10 Serial Chan. 2 FlexRay Nodes
XC2269I-104FxxL	832 Kbytes	64 Kbytes 24 Kbytes	CC2 CCU60/1/2/3	11 + 8	6 CAN Nodes 10 Serial Chan. 2 FlexRay Nodes
XC2269I-136FxxL	1 088 Kbytes	64 Kbytes 24 Kbytes	CC2 CCU60/1/2/3	11 + 8	6 CAN Nodes 10 Serial Chan. 2 FlexRay Nodes

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in **Table 3**.

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

1.3 Definition of Feature Variants

The XC2269I types are offered with several Flash memory sizes. **Table 3** describes the location of the available memory areas for each Flash memory size.

Table 3 Flash Memory Allocation

Total Flash Size	Flash Area A[1)]	Flash Area B	Flash Area C
1 088 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $D0'FFFF_H$	n.a.
832 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $CB'FFFF_H$	$D0'0000_H$ … $D0'FFFF_H$
576 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C7'FFFF_H$	$D0'0000_H$ … $D0'FFFF_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1	Flash 2	Flash 3	Flash 4
1 088 Kbytes	256	256	256	256	64
832 Kbytes	256	256	256	---	64
576 Kbytes	256	256	---	---	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XC2269I types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels
11 ADC0 channels	CH0, CH2 … CH5, CH8 … CH11, CH13, CH15
8 ADC1 channels	CH0, CH2, CH4, CH5, CH6 (overlay: CH8 … CH11), CH12, CH13, CH14
6 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4, CAN5 256 message objects
10 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1, U3C0, U3C1, U4C0, U4C1
2 FlexRay nodes	FR0, FR1

2.1 Pin Configuration and Definition

The pins of the XC2269I are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

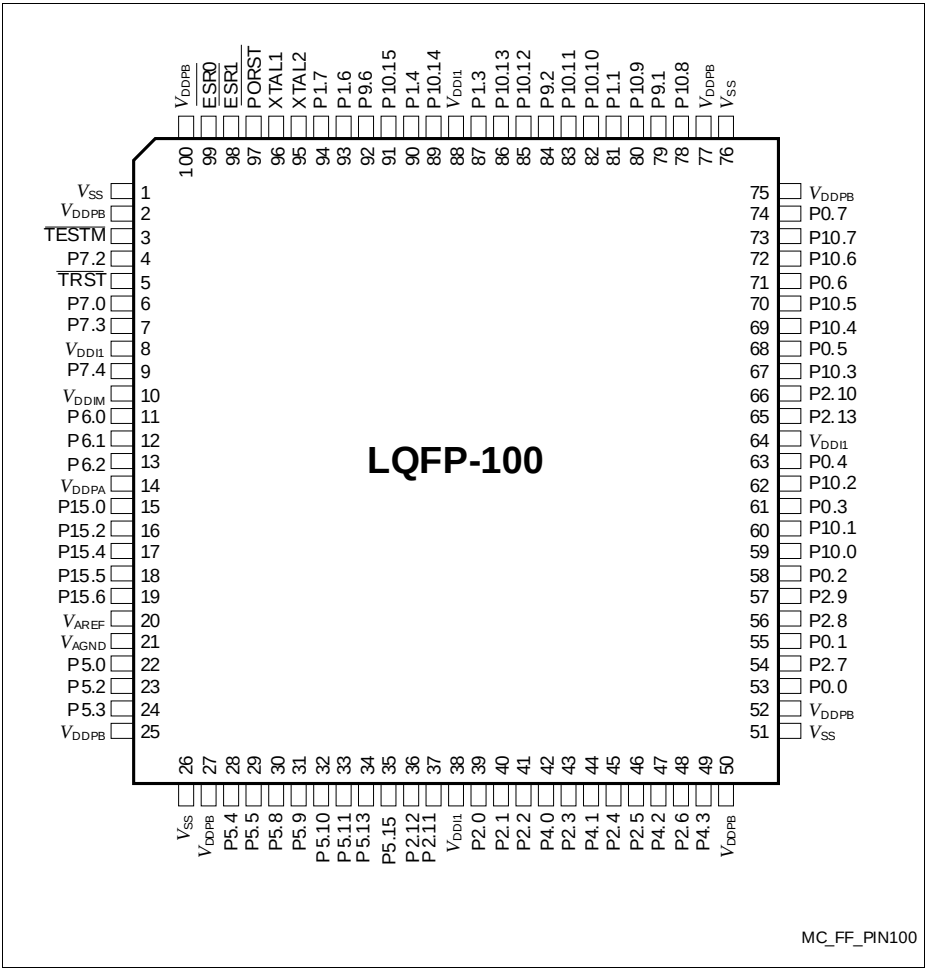

Figure 2 XC2269I Pin Configuration (top view)

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT12E Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT12E Timer T6 Toggle Latch Output**
	TDO_A	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
	RxDC4B	I	St/B	**CAN Node 4 Receive Data Input**
	U4C1_DX0C	I	St/B	**USIC4 Channel 0 Receive Data Input**
7	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
66	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_SELO 3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_CC23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	A23	OH	St/B	**External Bus Interface Address Line 23**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPINA	I	St/B	**GPT12E Register CAPREL Capture Input**
	U3C1_DX0A	I	St/B	**USIC3 Channel 1 Shift Data Input**
67	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COU T60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / IH	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
	U3C0_DX0A	I	St/B	**USIC3 Channel 0 Shift Data Input**
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLK OUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO 2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COU T62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	RXDC3E	I	St/B	**CAN Node 3 Receive Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
94	P1.7	O0 / I	St/B	**Bit 7 of Port 1, General Purpose Input/Output**
	CCU62_CC60	O1	St/B	**CCU62 Channel 0 Output**
	U1C1_MCLKOUT	O2	St/B	**USIC1 Channel 1 Master Clock Output**
	U2C0_SCLKOUT	O3	St/B	**USIC2 Channel 0 Shift Clock Output**
	A15	OH	St/B	**External Bus Interface Address Line 15**
	U2C0_DX1C	I	St/B	**USIC2 Channel 0 Shift Clock Input**
	CCU62_CC60INA	I	St/B	**CCU62 Channel 0 Input**
	RxDC4E	I	St/B	**CAN Node 4 Receive Data Input**
95	XTAL2	O	Sp/M	**Crystal Oscillator Amplifier Output**
96	XTAL1	I	Sp/M	**Crystal Oscillator Amplifier Input** To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM}.
	ESR2_9	I	St/B	**ESR2 Trigger Input 9**
97	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XC2269I completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.

2.2 Identification Registers

The identification registers describe the current version of the XC2269I and of its modules.

Table 7 XC2269I Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820_H	$00'F07E_H$	
SCU_IDCHIP	4801_H	$00'F07C_H$	Step AA
SCU_IDMEM	$310F_H$	$00'F07A_H$	
SCU_IDPROG	1313_H	$00'F078_H$	
JTAG_ID	$101B'F083_H$	---	

3 Functional Description

The architecture of the XC2269I combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources. This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC2269I.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC2269I.

3.1 Memory Subsystem and Organization

The memory space of the XC2269I is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC2269I **Memory Map** [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	$FF'FF00_H$	$FF'FFFF_H$	256 Bytes	
Reserved	$F0'0000_H$	$FF'FEFF_H$	< 1 Mbyte	Minus IMB registers
Reserved for EPSRAM	$E9'0000_H$	$EF'FFFF_H$	448 Kbytes	Mirrors EPSRAM
Emulated PSRAM	$E8'0000_H$	$E8'FFFF_H$	up to 64 Kbytes	With Flash timing
Reserved for PSRAM	$E1'0000_H$	$E7'FFFF_H$	448 Kbytes	Mirrors PSRAM
PSRAM	$E0'0000_H$	$E0'FFFF_H$	up to 64 Kbytes	Program SRAM
Reserved for Flash	$D1'0000_H$	$DF'FFFF_H$	448 Kbytes	
Flash 4	$D0'0000_H$	$D0'FFFF_H$	64 Kbytes	
Flash 3	$CC'0000_H$	$CF'FFFF_H$	256 Kbytes	
Flash 2	$C8'0000_H$	$CB'FFFF_H$	256 Kbytes	
Flash 1	$C4'0000_H$	$C7'FFFF_H$	256 Kbytes	
Flash 0	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes[3)]	Minus res. seg.
External memory area	$40'0000_H$	$BF'FFFF_H$	8 Mbytes	
External IO area[4)]	$21'0000_H$	$3F'FFFF_H$	1 984 Kbytes	

Table 9 Compare Modes (cont'd)

Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

3.9 Capture/Compare Units CCU6x

The XC2269I types feature the CCU60, CCU61, CCU62 and CCU63 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

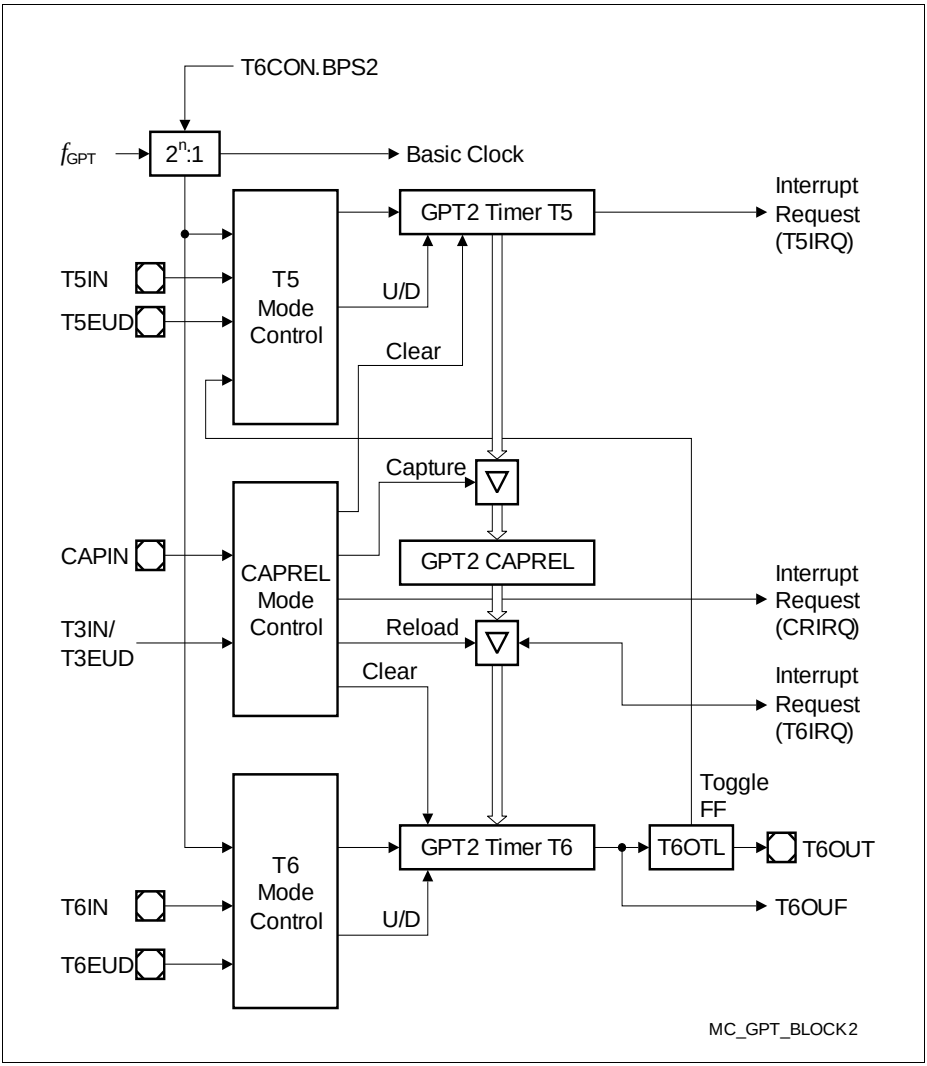

Figure 6 Block Diagram of GPT2

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XC2269I are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in **Section 4.6.4**.

Supply Voltage Restrictions

The XC2269I can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

During power-on sequences, the supply voltages may only change with a maximum speed of dV/dt < 5 V/µs, i.e. the target supply voltage may be reached earliest after approx. 1 µs.

Note: To limit the speed of supply voltage changes, the employment of external buffer capacitors at pins V_{DDPA}/V_{DDPB} is recommended.

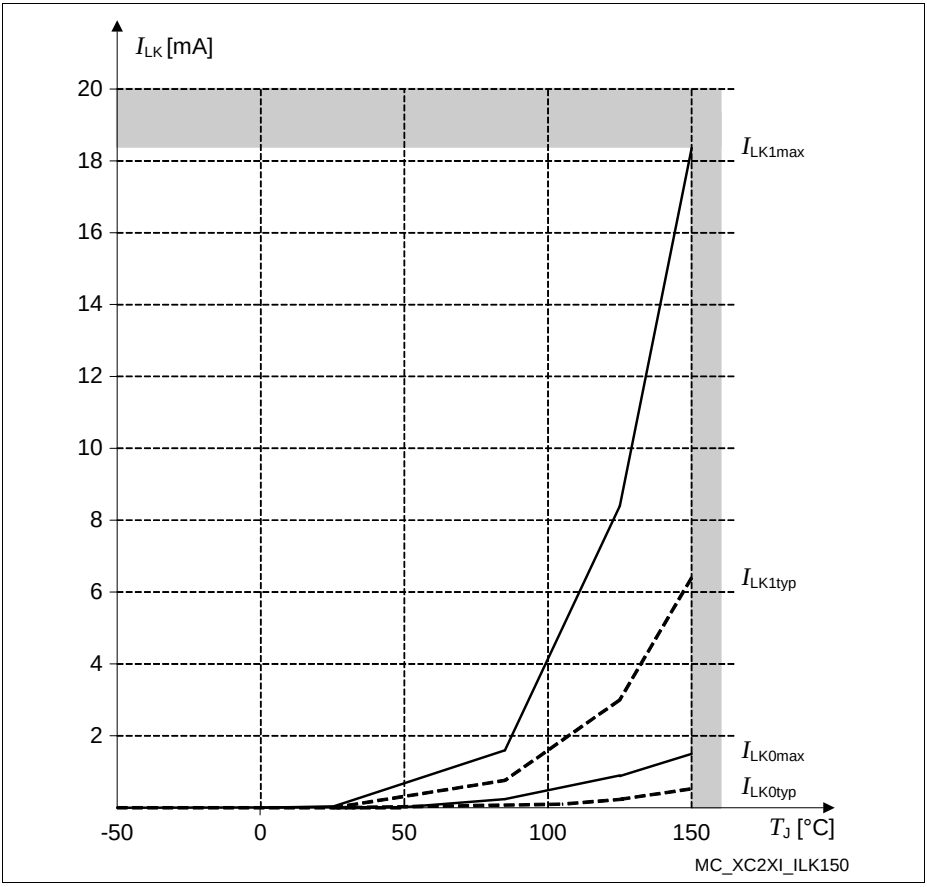

Figure 12 Leakage Supply Current as a Function of Temperature

Sample time and conversion time of the XC2269I's A/D converters are programmable. The timing above can be calculated using **Table 23**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 23 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}		INPCRx.7-0 (STC)	Sample Time[1] t_S
000000_B	f_{SYS}		00_H	$t_{ADCI} \times 2$
000001_B	f_{SYS} / 2		01_H	$t_{ADCI} \times 3$
000010_B	f_{SYS} / 3		02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)		:	$t_{ADCI} \times$ (STC+2)
111110_B	f_{SYS} / 63		FE_H	$t_{ADCI} \times 256$
111111_B	f_{SYS} / 64		FF_H	$t_{ADCI} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: f_{SYS} = 128 MHz (i.e. t_{SYS} = 7.8 ns), DIVA = 06_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 7 = 18.3 MHz, i.e. t_{ADCI} = 54.7 ns
Sample time t_S = $t_{ADCI} \times 2$ = 109.4 ns

Conversion 12-bit:

t_{C10} = $16 \times t_{ADCI} + 2 \times t_{SYS}$ = 16×54.7 ns + 2×7.8 ns = 0.891 µs

Conversion 10-bit:

t_{C8} = $12 \times t_{ADCI} + 2 \times t_{SYS}$ = 12×54.7 ns + 2×7.8 ns = 0.672 µs

Converter Timing Example B:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02_H, STC = 03_H
Analog clock f_{ADCI} = f_{SYS} / 3 = 13.3 MHz, i.e. t_{ADCI} = 75 ns
Sample time t_S = $t_{ADCI} \times 5$ = 375 ns

Conversion 12-bit:

t_{C10} = $19 \times t_{ADCI} + 2 \times t_{SYS}$ = 19×75 ns + 2×25 ns = 1.475 µs

Conversion 10-bit:

t_{C8} = $15 \times t_{ADCI} + 2 \times t_{SYS}$ = 15×75 ns + 2×25 ns = 1.175 µs

4.6.4 Pad Properties

The output pad drivers of the XC2269I can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP}. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

4.6.5.1 Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.

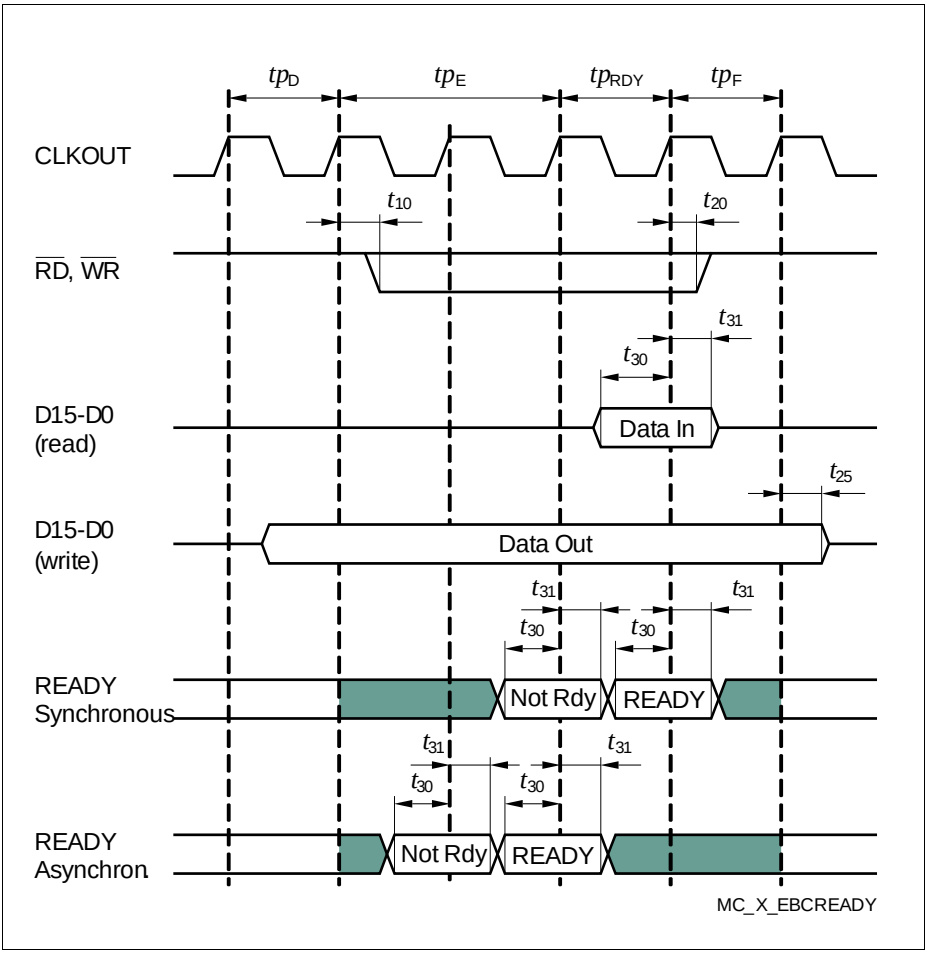

Figure 22 READY Timing

Note: If the READY input is sampled inactive at the indicated sampling point (“Not Rdy”) a READY-controlled waitstate is inserted (tpRDY),
sampling the READY input active at the indicated sampling point (“Ready”) terminates the currently running bus cycle.
Note the different sampling points for synchronous and asynchronous READY.
This example uses one mandatory waitstate (see tpE) before the READY input value is used.

Table 38 USIC SSC Master Mode Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 39 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	7	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	7	–	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

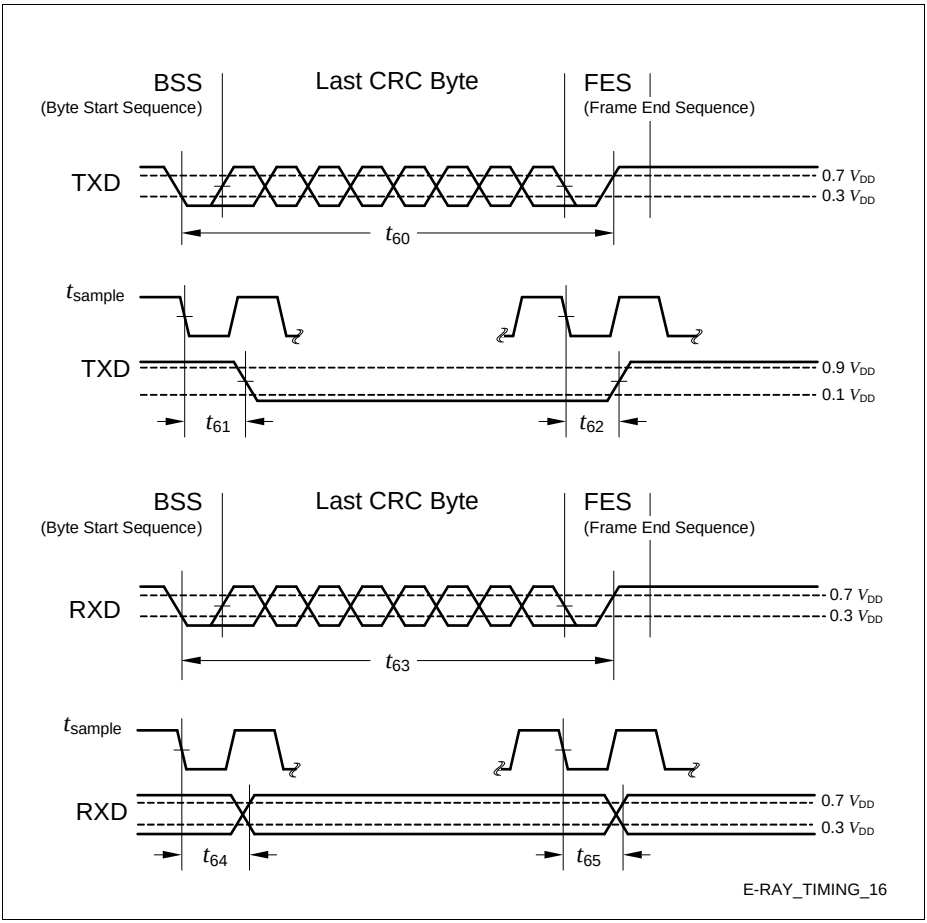

Figure 24 FlexRay Timing