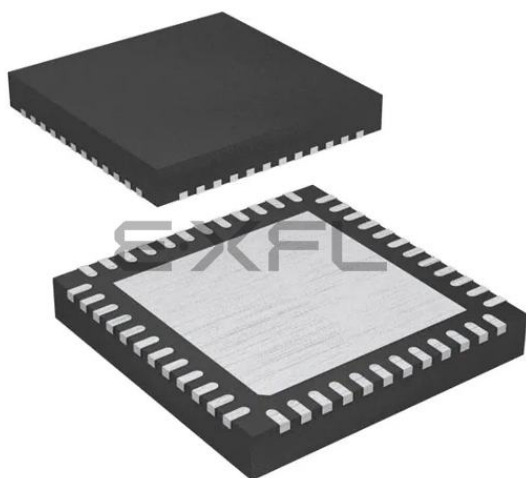




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk20dn64vft5

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

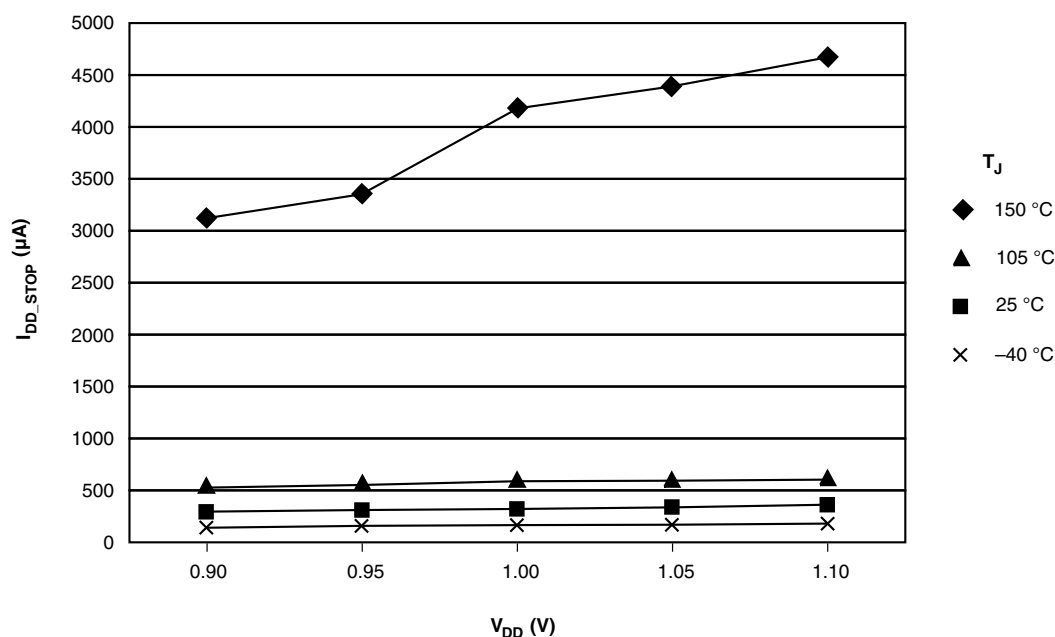
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	–55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	–100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	–0.3	3.8	V

Table continues on the next page...

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V _{LVW1H} V _{LVW2H} V _{LVW3H} V _{LVW4H}	Low-voltage warning thresholds — high range - Level 1 falling (LVWV=00) - Level 2 falling (LVWV=01) - Level 3 falling (LVWV=10) - Level 4 falling (LVWV=11)	2.62 2.72 2.82 2.92	2.70 2.80 2.90 3.00	2.78 2.88 2.98 3.08	V V V V	1
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V _{LVW1L} V _{LVW2L} V _{LVW3L} V _{LVW4L}	Low-voltage warning thresholds — low range - Level 1 falling (LVWV=00) - Level 2 falling (LVWV=01) - Level 3 falling (LVWV=10) - Level 4 falling (LVWV=11)	1.74 1.84 1.94 2.04	1.80 1.90 2.00 2.10	1.86 1.96 2.06 2.16	V V V V	1
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	• VLLS0 → RUN	—	130	μs	
	• VLLS1 → RUN	—	130	μs	
	• VLLS2 → RUN	—	70	μs	
	• VLLS3 → RUN	—	70	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	—	5.2	μs	
	• STOP → RUN	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash	—	13.7	15.1	mA	2
		—	13.9	15.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash	—	16.1	18.2	mA	3, 4
		—	16.3	17.7	mA	
		—	16.7	18.4	mA	
		—	16.7	18.4	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.5	8.4	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.6	6.4	mA	5

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	867	—	μA	6
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	509	—	μA	8
I _{DD_STOP}	Stop mode current at 3.0 V • @ -40 to 25°C • @ 70°C • @ 105°C	—	310	426	μA	
		—	384	458	μA	
		—	629	1100	μA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V • @ -40 to 25°C • @ 70°C • @ 105°C	—	3.5	22.6	μA	
		—	20.7	52.9	μA	
		—	85	220	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V • @ -40 to 25°C • @ 70°C • @ 105°C	—	2.1	3.7	μA	
		—	7.7	43.1	μA	
		—	32.2	68	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ -40 to 25°C • @ 70°C • @ 105°C	—	1.5	2.9	μA	
		—	4.8	22.5	μA	
		—	20	37.8	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ -40 to 25°C • @ 70°C • @ 105°C	—	1.4	2.8	μA	
		—	4.1	19.2	μA	
		—	17.3	32.4	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ -40 to 25°C • @ 70°C • @ 105°C	—	0.678	1.3	μA	
		—	2.8	13.6	μA	
		—	13.6	24.5	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • @ -40 to 25°C • @ 70°C • @ 105°C	—	0.367	1.0	μA	
		—	2.4	13.3	μA	
		—	13.2	24.1	μA	

Table continues on the next page...

- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

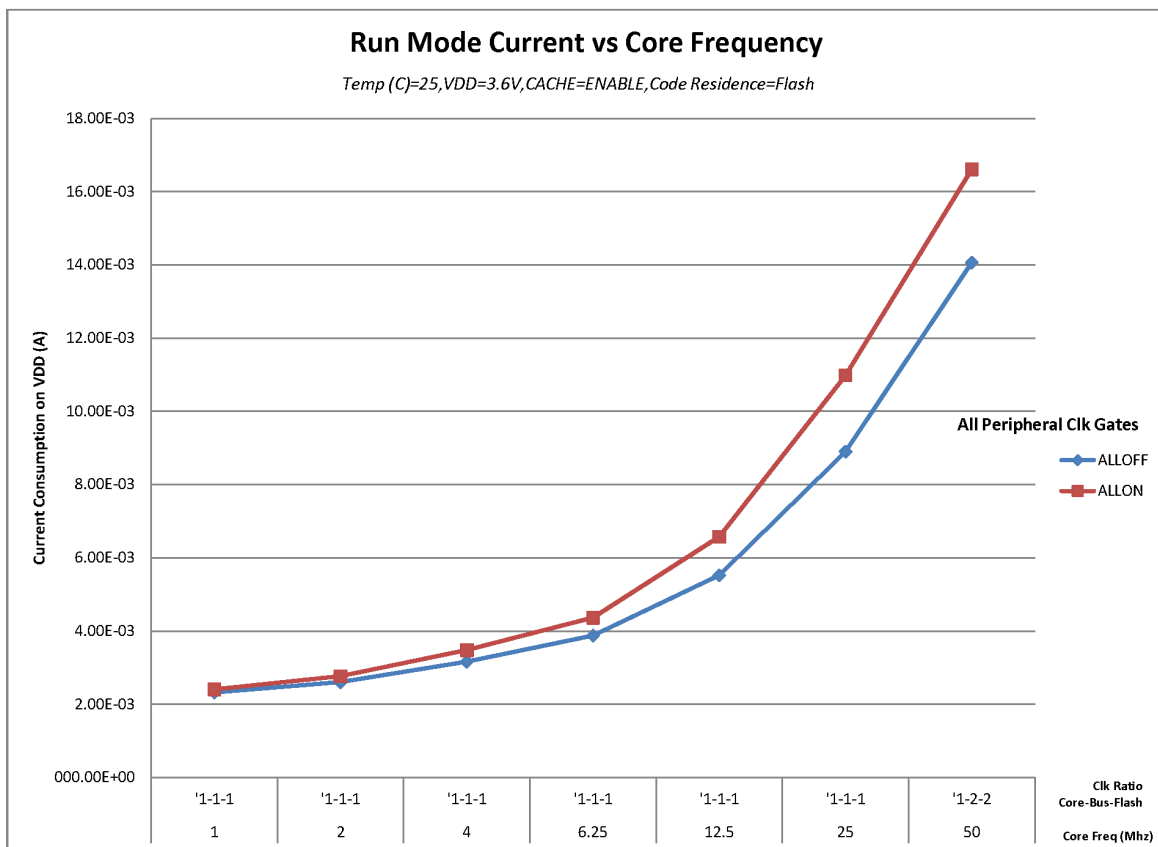


Figure 2. Run mode supply current vs. core frequency

emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{OSC} = 12\text{ MHz}$ (crystal), $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to <http://www.freescale.com>.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	

Table continues on the next page...

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	- Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	—	12	ns	
		—	6	ns	
		—	36	ns	
		—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	48 LQFP	48 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	70	81	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	47	28	°C/W	1, 3

Table continues on the next page...

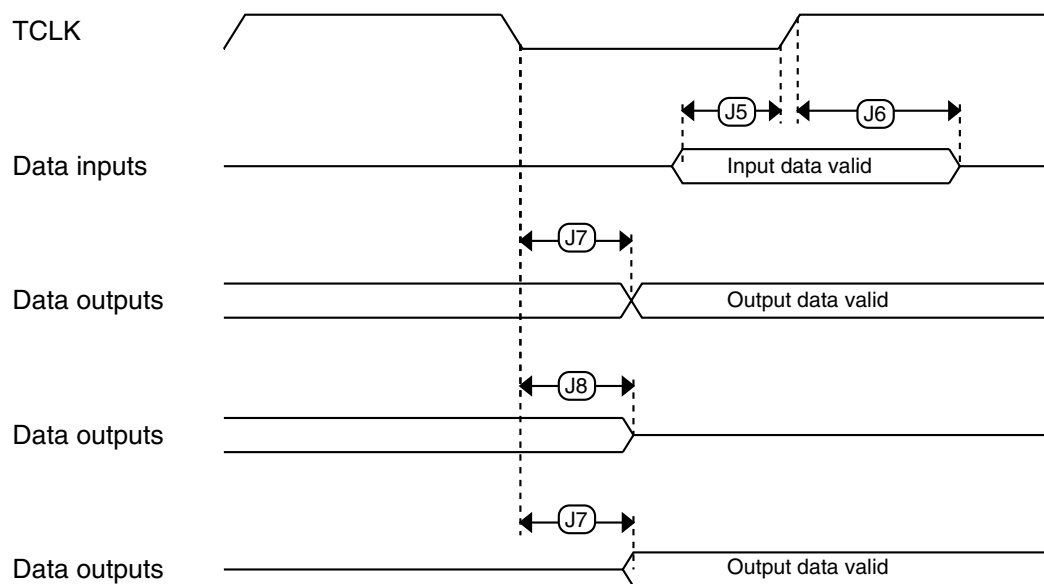


Figure 5. Boundary scan (JTAG) timing

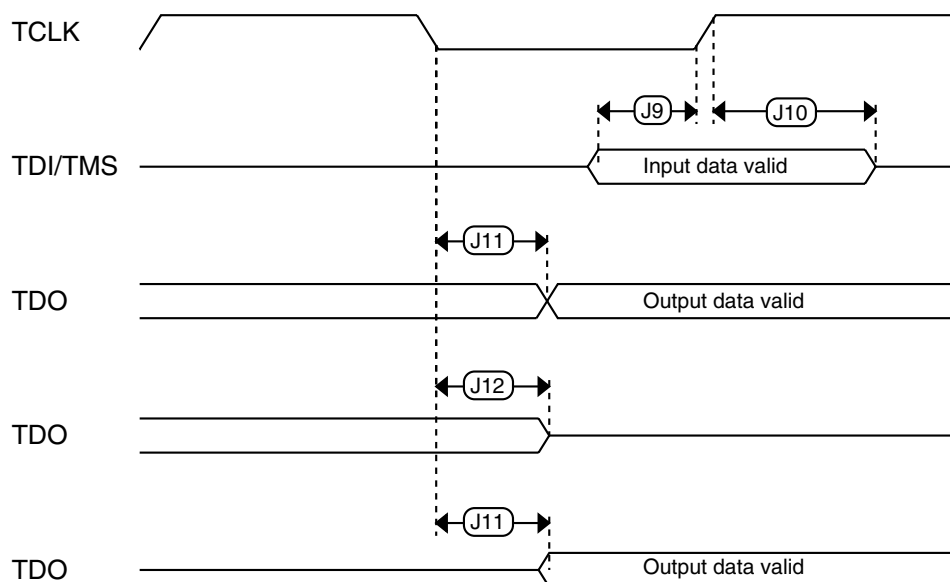
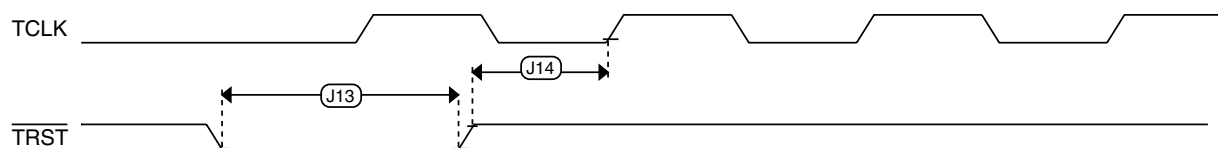


Figure 6. Test Access Port timing

Figure 7. $\overline{\text{TRST}}$ timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 13. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 3	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	—	$\%f_{\text{dco}}$	1
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$f_{\text{loc_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints_t}}$	—	—	kHz	
$f_{\text{loc_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints_t}}$	—	—	kHz	
FLL						

Table continues on the next page...

Table 13. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{fill_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fill_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fill_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fill_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fill_ref}	80	83.89	100	MHz	
f _{dco_t_DMx3} 2	DCO output frequency	Low range (DRS=00) 732 × f _{fill_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fill_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fill_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fill_ref}	—	95.98	—	MHz	
J _{cyc_fill}	FLL period jitter - f_{VCO} = 48 MHz - f_{VCO} = 98 MHz		— —	180 150	— —	ps	
t _{fill_acquire}	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f _{vco}	VCO operating frequency		48.0	—	100	MHz	
I _{pll}	PLL operating current PLL @ 96 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	μA	7
I _{pll}	PLL operating current PLL @ 48 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	μA	7
f _{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS)						8
	- f_{vco} = 48 MHz - f_{vco} = 100 MHz		— —	120 50	— —	ps ps	

Table continues on the next page...

Table 19. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Word-write to FlexRAM for EEPROM operation						
$t_{\text{eewr16bers}}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
$t_{\text{eewr16b8k}}$	Word-write to FlexRAM execution time: • 8 KB EEPROM backup	—	340	1700	μs	
$t_{\text{eewr16b16k}}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr16b32k}}$	• 32 KB EEPROM backup	—	475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{\text{eewr32bers}}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
$t_{\text{eewr32b8k}}$	Longword-write to FlexRAM execution time: • 8 KB EEPROM backup	—	545	1950	μs	
$t_{\text{eewr32b16k}}$	• 16 KB EEPROM backup	—	630	2050	μs	
$t_{\text{eewr32b32k}}$	• 32 KB EEPROM backup	—	810	2250	μs	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash high voltage current behaviors

Table 20. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{\text{DD_PGM}}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{\text{DD_ERS}}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 21. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
$t_{\text{nvmretp10k}}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{\text{nvmretp1k}}$	Data retention after up to 1 K cycles	20	100	—	years	
n_{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{\text{nvmretd10k}}$	Data retention after up to 10 K cycles	5	50	—	years	

Table continues on the next page...

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	- ADLPC=1, ADHSC=0 - ADLPC=1, ADHSC=1 - ADLPC=0, ADHSC=0 - ADLPC=0, ADHSC=1	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12 bit modes <12 bit modes	— —	± 4 ± 1.4	± 6.8 ± 2.1	LSB ⁴	5
DNL	Differential non-linearity	12 bit modes <12 bit modes	— —	± 0.7 ± 0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12 bit modes <12 bit modes	— —	± 1.0 ± 0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12 bit modes <12 bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	16 bit modes ≤ 13 bit modes	— —	-1 to 0 —	— ± 0.5	LSB ⁴	
ENOB	Effective number of bits	16 bit differential mode - Avg=32 - Avg=4 16 bit single-ended mode - Avg=32 - Avg=4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16 bit differential mode - Avg=32 16 bit single-ended mode - Avg=32	— —	-94 -85	— —	dB dB	7

Table continues on the next page...

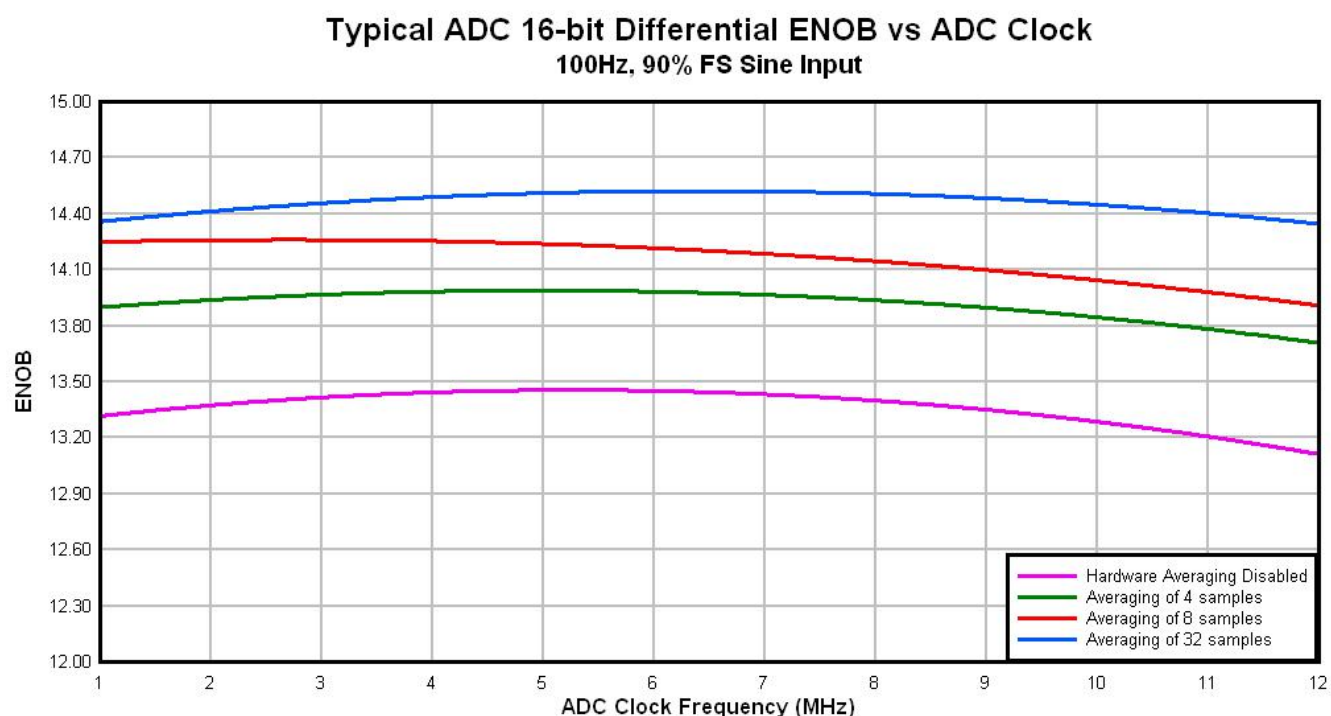


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit differential mode

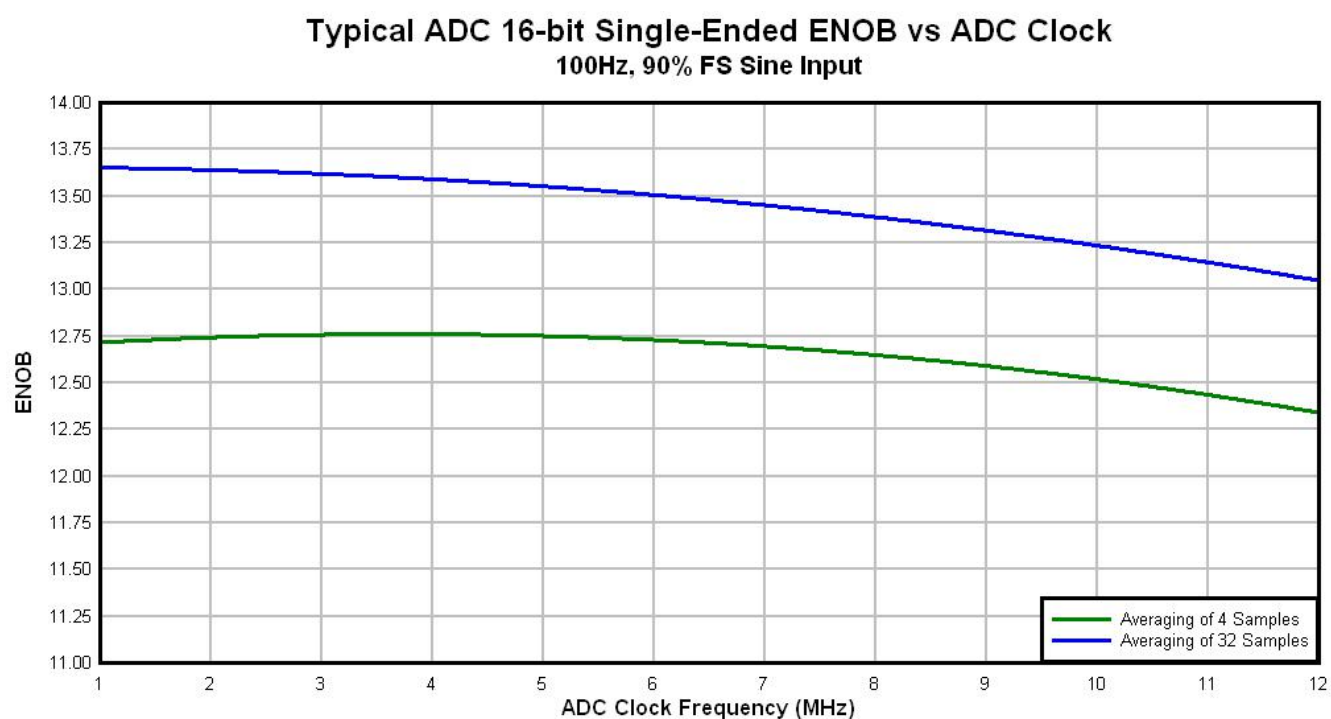


Figure 12. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

6.8.2 USB DCD electrical specifications

Table 30. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 μ A)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μ A
I _{DM_SINK}	USB_DM sink current	50	100	150	μ A
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	k Ω
V _{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 USB VREG electrical specifications

Table 31. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V _{REGIN}	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (V _{REGIN}) > 3.6 V	—	120	186	μ A	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	1.54	μ A	
I _{DDoff}	Quiescent current — Shutdown mode - V_{REGIN} = 5.0 V and temperature=25C - Across operating voltage and temperature	—	650	—	nA	
		—	—	4	μ A	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) > 3.6 V - Run mode - Standby mode	3	3.3	3.6	V	
		2.1	2.8	3.6	V	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) < 3.6 V, pass-through mode	2.1	—	3.6	V	2

Table continues on the next page...

**Table 31. USB VREG electrical specifications
(continued)**

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
C _{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I _{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 32. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t _{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCS _n valid to DSPI_SCK delay	(t _{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS _n invalid delay	(t _{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	14	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

6.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 34. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

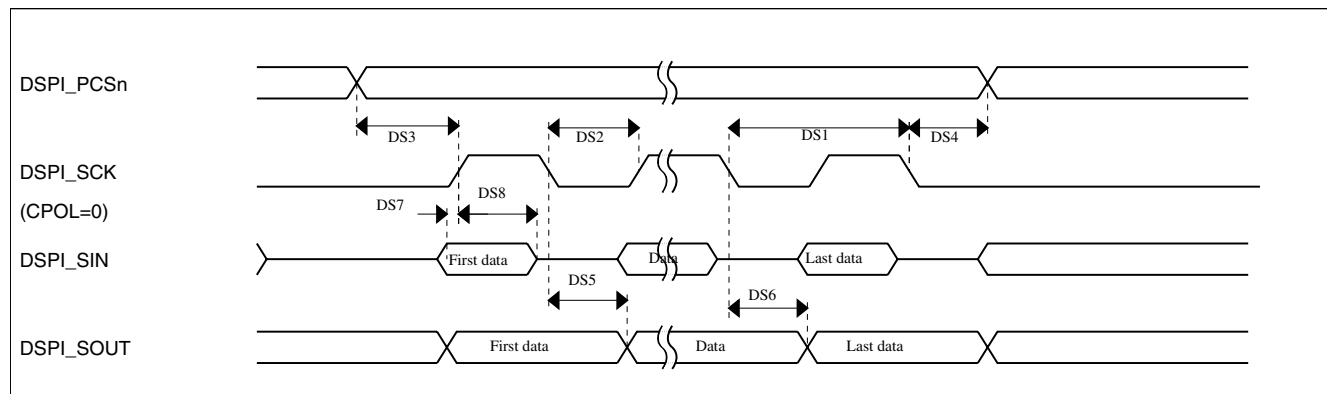


Figure 17. DSPI classic SPI timing — master mode

6.8.8 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.8.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 36. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

8 Pinout

8.1 K20 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

48 LQFP -QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	VDD	VDD	VDD								
2	VSS	VSS	VSS								
3	USB0_DP	USB0_DP	USB0_DP								
4	USB0_DM	USB0_DM	USB0_DM								
5	VOUT33	VOUT33	VOUT33								
6	VREGIN	VREGIN	VREGIN								
7	ADC0_DP0	ADC0_DP0	ADC0_DP0								
8	ADC0_DM0	ADC0_DM0	ADC0_DM0								
9	VDDA	VDDA	VDDA								
10	VREFH	VREFH	VREFH								
11	VREFL	VREFL	VREFL								
12	VSSA	VSSA	VSSA								
13	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5								
14	XTAL32	XTAL32	XTAL32								
15	EXTAL32	EXTAL32	EXTAL32								
16	VBAT	VBAT	VBAT								
17	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSIO_CH1	PTA0	UART0_CTS_b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
18	PTA1	JTAG_TDI/ EZP_DI	TSIO_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
19	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSIO_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
20	PTA3	JTAG_TMS/ SWD_DIO	TSIO_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
21	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSIO_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
22	VDD	VDD	VDD								
23	VSS	VSS	VSS								