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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I <sup>2</sup> S, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk20dx128vft5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	<ul> <li>32 = 32 KB</li> <li>64 = 64 KB</li> <li>128 = 128 KB</li> <li>256 = 256 KB</li> <li>512 = 512 KB</li> <li>1M0 = 1 MB</li> </ul>
R	Silicon revision	<ul> <li>Z = Initial</li> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>
Т	Temperature range (°C)	<ul> <li>V = -40 to 105</li> <li>C = -40 to 85</li> </ul>
PP	Package identifier	<ul> <li>FM = 32 QFN (5 mm x 5 mm)</li> <li>FT = 48 QFN (7 mm x 7 mm)</li> <li>LF = 48 LQFP (7 mm x 7 mm)</li> <li>LH = 64 LQFP (10 mm x 10 mm)</li> <li>MP = 64 MAPBGA (5 mm x 5 mm)</li> <li>LK = 80 LQFP (12 mm x 12 mm)</li> <li>MB = 81 MAPBGA (8 mm x 8 mm)</li> <li>LL = 100 LQFP (14 mm x 14 mm)</li> <li>ML = 104 MAPBGA (8 mm x 8 mm)</li> <li>LQ = 121 MAPBGA (8 mm x 8 mm)</li> <li>LQ = 144 LQFP (20 mm x 20 mm)</li> <li>MD = 144 MAPBGA (13 mm x 13 mm)</li> <li>MJ = 256 MAPBGA (17 mm x 17 mm)</li> </ul>
СС	Maximum CPU frequency (MHz)	<ul> <li>5 = 50 MHz</li> <li>7 = 72 MHz</li> <li>10 = 100 MHz</li> <li>12 = 120 MHz</li> <li>15 = 150 MHz</li> </ul>
N	Packaging type	<ul> <li>R = Tape and reel</li> <li>(Blank) = Trays</li> </ul>

## 2.4 Example

This is an example part number:

MK20DN32VLF5

# 3 Terminology and guidelines

Terminology and guidelines



# 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

# 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

#### General

# 5.2.2 LVD and POR operating requirements

 Table 2.
 V<sub>DD</sub> supply LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V <sub>LVW1H</sub>	Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V <sub>LVW2H</sub>	Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V <sub>LVW3H</sub>	Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V <sub>LVW4H</sub>	Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	_	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V <sub>LVW1L</sub>	Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V <sub>LVW2L</sub>	Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V <sub>LVW3L</sub>	Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V <sub>LVW4L</sub>	Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	_	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

### Table 3. VBAT power operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	867	_	μA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	_	mA	7
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V	_	509	_	μA	8
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V					
	• @ -40 to 25°C	—	310	426	μA	
	• @ 70°C	—	384	458	μA	
	• @ 105°C	—	629	1100	μA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V					
	● @ -40 to 25°C	—	3.5	22.6	μA	
	• @ 70°C	—	20.7	52.9	μA	
	• @ 105°C	—	85	220	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V					
	● @ -40 to 25°C	—	2.1	3.7	μA	
	• @ 70°C	—	7.7	43.1	μA	
	• @ 105°C	—	32.2	68	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V					
	● @ -40 to 25°C	_	1.5	2.9	μA	
	• @ 70°C	_	4.8	22.5	μA	
	• @ 105°C	—	20	37.8	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V					
	• @ -40 to 25°C	_	1.4	2.8	μA	
	• @ 70°C	_	4.1	19.2	μA	
	• @ 105°C	—	17.3	32.4	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V					
	• @ -40 to 25°C	_	0.678	1.3	μA	
	• @ 70°C	_	2.8	13.6	μA	
	• @ 105°C	_	13.6	24.5	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POB detect circuit enabled					
	• @ -40 to 25°C	_	0.367	1.0	μA	
	• @ 70°C	_	2.4	13.3	μA	
	• @ 105°C	_	13.2	24.1	μA	

 Table 6. Power consumption operating behaviors (continued)

Table continues on the next page...





Figure 3. VLPR mode supply current vs. core frequency

### 5.2.6 EMC radiated emissions operating behaviors Table 7. EMC radiated emissions operating behaviors for 64LQFP

Symbol	Description	Frequency band (MHz)	Тур.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	19	dBµV	1,2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	21	dBµV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	19	dBµV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	11	dBµV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	L	—	2, 3

 Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported

emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

- 2.  $V_{DD} = 3.3 \text{ V}$ ,  $T_A = 25 \text{ °C}$ ,  $f_{OSC} = 12 \text{ MHz}$  (crystal),  $f_{SYS} = 48 \text{ MHz}$ ,  $f_{BUS} = 48 \text{ MHz}$
- 3. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions TEM Cell and Wideband TEM Cell Method

### 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to http://www.freescale.com.
- 2. Perform a keyword search for "EMC design."

### 5.2.8 Capacitance attributes

#### Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C <sub>IN_A</sub>	Input capacitance: analog pins	_	7	pF
C <sub>IN_D</sub>	Input capacitance: digital pins	—	7	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
	Normal run mode	9			
f <sub>SYS</sub>	System and core clock		50	MHz	
f <sub>SYS_USB</sub>	System and core clock when Full Speed USB in operation	20	_	MHz	
f <sub>BUS</sub>	Bus clock		50	MHz	
f <sub>FLASH</sub>	Flash clock		25	MHz	
f <sub>LPTMR</sub>	LPTMR clock		25	MHz	
VLPR mode <sup>1</sup>					
f <sub>SYS</sub>	System and core clock	_	4	MHz	
f <sub>BUS</sub>	Bus clock		4	MHz	

Table continues on the next page ...

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	_	6	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	_	24	ns	
		1			

#### Table 10. General switching specifications (continued)

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater synchronous and asynchronous timing must be met.
- 3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
- 4. 75pF load
- 5. 15pF load

# 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

#### Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T <sub>A</sub>	Ambient temperature	-40	105	°C

### 5.4.2 Thermal attributes

Board type	Symbol	Description	48 LQFP	48 QFN	Unit	Notes
Single-layer (1s)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	70	81	°C/W	1, 2
Four-layer (2s2p)	R <sub>eja</sub>	Thermal resistance, junction to ambient (natural convection)	47	28	°C/W	1, 3

Table continues on the next page...

Board type	Symbol	Description	48 LQFP	48 QFN	Unit	Notes
Single-layer (1s)	R <sub>ejma</sub>	Thermal resistance, junction to ambient (200 ft./ min. air speed)	58	66	°C/W	1,3
Four-layer (2s2p)	R <sub>ejma</sub>	Thermal resistance, junction to ambient (200 ft./ min. air speed)	40	23	°C/W	,
	R <sub>0JB</sub>	Thermal resistance, junction to board	24	11	°C/W	5
_	R <sub>θJC</sub>	Thermal resistance, junction to case	18	1.4	°C/W	6
	Ψ <sub>JT</sub>	Thermal characterization parameter, junction to package top outside center (natural convection)	3	4	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air) with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.

3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)* with the board horizontal.

5. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.

- 6. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- 7. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).

# 6 Peripheral operating requirements and behaviors

## 6.1 Core modules





## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

## 6.3.1 MCG specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes		
f <sub>ints_ft</sub>	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	_	kHz			
f <sub>ints_t</sub>	Internal reference frequency (slow clock) — user trimmed	31.25	_	39.0625	kHz			
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	_	± 0.3	± 0.6	%f <sub>dco</sub>	1		
$\Delta f_{dco_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	_	+0.5/-0.7	± 3	%f <sub>dco</sub>	1		
∆f <sub>dco_t</sub>	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		± 0.3	_	%f <sub>dco</sub>	1		
f <sub>intf_ft</sub>	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	_	4	_	MHz			
f <sub>intf_t</sub>	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	_	5	MHz			
f <sub>loc_low</sub>	Loss of external clock minimum frequency — RANGE = 00	(3/5) x f <sub>ints_t</sub>	_	_	kHz			
f <sub>loc_high</sub>	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	(16/5) x f <sub>ints_t</sub>	_	_	kHz			

### Table 13. MCG specifications

Table continues on the next page...

Symbol	Description		Min.	Тур.	Max.	Unit	Notes
f <sub>fll_ref</sub>	FLL reference free	quency range	31.25	—	39.0625	kHz	
f <sub>dco</sub>	DCO output frequency range	Low range (DRS=00) 640 × f <sub>fll_ref</sub>	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f <sub>fll_ref</sub>	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f <sub>fll_ref</sub>	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f <sub>fll_ref</sub>	80	83.89	100	MHz	
f <sub>dco_t_DMX3</sub>	DCO output frequency	Low range (DRS=00) 732 × f <sub>fll_ref</sub>	_	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f <sub>fll_ref</sub>	_	47.97	_	MHz	
		Mid-high range (DRS=10) 2197 × f <sub>fll_ref</sub>	_	71.99	_	MHz	
		High range (DRS=11) 2929 × f <sub>fll_ref</sub>	_	95.98	_	MHz	
J <sub>cyc_fll</sub>	FLL period jitter		_	180	_	ps	
	<ul> <li>f<sub>VCO</sub> = 48 M</li> <li>f<sub>VCO</sub> = 98 M</li> </ul>	Hz Hz	_	150	_		
t <sub>fll_acquire</sub>	FLL target frequer	ncy acquisition time	—		1	ms	6
		Р	LL				
f <sub>vco</sub>	VCO operating fre	quency	48.0	—	100	MHz	
I <sub>pll</sub>	PLL operating cur PLL @ 96 M 2 MHz, VDI	rent 1Hz (f <sub>osc_hi_1</sub> = 8 MHz, f <sub>pll_ref</sub> = V multiplier = 48)	_	1060	_	μΑ	7
I <sub>pll</sub>	PLL operating current • PLL @ 48 MHz (f <sub>osc_hi_1</sub> = 8 MHz, f <sub>pll_ref</sub> = 2 MHz, VDIV multiplier = 24)			600	_	μA	7
f <sub>pll_ref</sub>	PLL reference free	quency range	2.0	—	4.0	MHz	
J <sub>cyc_pll</sub>	PLL period jitter (F	RMS)					8
	• f <sub>vco</sub> = 48 MH	lz	-	120	—	ps	
	• f <sub>vco</sub> = 100 M	Hz	-	50	-	ps	

### Table 13. MCG specifications (continued)

Table continues on the next page ...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
J <sub>acc_pll</sub>	PLL accumulated jitter over 1µs (RMS)					8
	• f <sub>vco</sub> = 48 MHz	—	1350	—	ps	
	• f <sub>vco</sub> = 100 MHz	—	600	_	ps	
D <sub>lock</sub>	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D <sub>unl</sub>	Lock exit frequency tolerance	± 4.47		± 5.97	%	
t <sub>pll_lock</sub>	Lock detector detection time			$150 \times 10^{-6}$ + 1075(1/ f <sub>pll_ref</sub> )	S	9

Table 13. MCG specifications (continued)

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).

2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.

The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation
 (Δf<sub>dco\_t</sub>) over voltage and temperature should be considered.

4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.

5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.

6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

7. Excludes any oscillator currents that are also consuming power while PLL is in operation.

8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.

 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

#### 6.3.2.1 Oscillator DC electrical specifications Table 14. Oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	_	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	-	500	_	nA	
	• 4 MHz	-	200	_	μA	
	• 8 MHz (RANGE=01)	-	300	_	μA	
	• 16 MHz	-	950	_	μA	
	• 24 MHz	_	1.2	_	mA	
	• 32 MHz	_	1.5	—	mA	
1			1		1	1

Table continues on the next page ...

Num	Description	Min.	Max.	Unit
EP1	EZP_CK frequency of operation (all commands except READ)	—	f <sub>SYS</sub> /2	MHz
EP1a	EZP_CK frequency of operation (READ command)		f <sub>SYS</sub> /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t <sub>EZP_CK</sub>	_	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	_	ns
EP4	EZP_CK high to $\overline{\text{EZP}_{CS}}$ input invalid (hold)	5		ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	_	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	_	ns
EP7	EZP_CK low to EZP_Q output valid		17	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	_	ns
EP9	EZP_CS negation to EZP_Q tri-state	_	12	ns







## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

# 6.6 Analog

## 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 23 and Table 24 are achievable on the differential pins ADCx\_DP0, ADCx\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> - V <sub>DDA</sub> )	-100	0	+100	mV	2
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> - V <sub>SSA</sub> )	-100	0	+100	mV	2
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	
V <sub>REFL</sub>	Reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	
V <sub>ADIN</sub>	Input voltage		V <sub>REFL</sub>	—	V <sub>REFH</sub>	V	
C <sub>ADIN</sub>	Input	16 bit modes	_	8	10	pF	
	capacitance	<ul> <li>8/10/12 bit modes</li> </ul>	_	4	5		
R <sub>ADIN</sub>	Input resistance			2	5	kΩ	
R <sub>AS</sub>	Analog source resistance	13/12 bit modes f <sub>ADCK</sub> < 4MHz	_	_	5	kΩ	3
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13 bit modes	1.0		18.0	MHz	4
f <sub>ADCK</sub>	ADC conversion clock frequency	16 bit modes	2.0		12.0	MHz	4
C <sub>rate</sub>	ADC conversion	≤ 13 bit modes					5
	rate	No ADC hardware averaging Continuous conversions enabled.	20.000	_	818.330	Ksps	
		subsequent conversion time					

### 6.6.1.1 16-bit ADC operating conditions Table 23. 16-bit ADC operating conditions

Table continues on the next page...

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
C <sub>rate</sub>	ADC conversion rate	16 bit modes No ADC hardware averaging	37.037	_	461.467	Ksps	5
		Continuous conversions enabled, subsequent conversion time					

Table 23. 16-bit ADC operating conditions (continued)

 Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25°C, f<sub>ADCK</sub> = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

- 2. DC potential difference.
- 3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8  $\Omega$  analog source resistance. The R<sub>AS</sub>/ C<sub>AS</sub> time constant should be kept to <1ns.
- 4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/ files/soft\_dev\_tools/software/app\_software/converters/ADC\_CALCULATOR\_CNV.zip?fpsp=1



Figure 10. ADC input impedance equivalency diagram

### 6.6.1.2 16-bit ADC electrical characteristics Table 24. 16-bit ADC characteristics (V<sub>REFH</sub> = V<sub>DDA</sub>, V<sub>REFL</sub> = V<sub>SSA</sub>)

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
I <sub>DDA_ADC</sub>	Supply current		0.215		1.7	mA	3

Table continues on the next page ...



Figure 14. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

## 6.6.3 Voltage reference electrical specifications

Table 26. VI	REF full-range	operating	requirements
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Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	1.71	3.6	V	
T <sub>A</sub>	Temperature	-40	105	°C	
CL	Output load capacitance	100		nF	1, 2

1. C<sub>L</sub> must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.

 The load capacitance should not exceed +/-25% of the nominal specified C<sub>L</sub> value over the operating temperature range of the device.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim at nominal $V_{\text{DDA}}$ and temperature=25C	1.1915	1.195	1.1977	V	

Table 27. VREF full-range operating behaviors

Table continues on the next page...

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	_	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t <sub>BUS</sub>	—	ns
DS10	DSPI_SCK input high/low time	(t <sub>SCK</sub> /2) - 4	(t <sub>SCK/2)</sub> + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	_	24	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	_	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	_	ns
DS15	DSPI_SS active to DSPI_SOUT driven	_	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	_	19	ns







# 6.8.6 I<sup>2</sup>C switching specifications

See General switching specifications.

## 6.8.7 UART switching specifications

See General switching specifications.





## 6.9 Human-machine interfaces (HMI)

# 6.9.1 TSI electrical specifications

Table 40. TSI electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>DDTSI</sub>	Operating voltage	1.71	—	3.6	V	
C <sub>ELE</sub>	Target electrode capacitance range	1	20	500	pF	1
f <sub>REFmax</sub>	Reference oscillator frequency	—	8	15	MHz	2, 3
f <sub>ELEmax</sub>	Electrode oscillator frequency	_	1	1.8	MHz	2, 4
C <sub>REF</sub>	Internal reference capacitor	_	1	—	pF	
V <sub>DELTA</sub>	Oscillator delta voltage	_	500	_	mV	2, 5
I <sub>REF</sub>	Reference oscillator current source base current	_	2	3	μA	2, 6
	• $32 \mu\text{A}$ setting (REFCHRG = 15)	—	36	50		
I <sub>ELE</sub>	Electrode oscillator current source base current • 2 uA setting (EXTCHBG = 0)	_	2	3	μA	2, 7
	• 32 µA setting (EXTCHRG = 15)	—	36	50		
Pres5	Electrode capacitance measurement precision	_	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution		—	16	bits	

Table continues on the next page ...

Table 40. TSI electrical specifications (continued)

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
T <sub>Con20</sub>	Response time @ 20 pF	8	15	25	μs	12
I <sub>TSI_RUN</sub>	Current added in run mode	_	55	_	μA	
I <sub>TSI_LP</sub>	Low power mode current adder		1.3	2.5	μA	13

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.

2. Fixed external capacitance of 20 pF.

3. REFCHRG = 2, EXTCHRG=0.

4. REFCHRG = 0, EXTCHRG = 10.

- 5.  $V_{DD} = 3.0 V.$
- 6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
- 7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
- 8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; lext = 16.
- 9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; lext = 16.
- 10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; lext = 16.
- 11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: (C<sub>ref</sub> \* I<sub>ext</sub>)/(I<sub>ref</sub> \* PS \* NSCN)

The typical value is calculated with the following configuration:

 $I_{ext} = 6 \ \mu A \ (EXTCHRG = 2), PS = 128, NSCN = 2, I_{ref} = 16 \ \mu A \ (REFCHRG = 7), C_{ref} = 1.0 \ pF$ 

The minimum value is calculated with the following configuration:

 $I_{ext} = 2 \ \mu A$  (EXTCHRG = 0), PS = 128, NSCN = 32,  $I_{ref} = 32 \ \mu A$  (REFCHRG = 15),  $C_{ref} = 0.5 \ pF$ 

The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.

- 12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
- 13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number				
48-pin LQFP	98ASH00962A				
48-pin QFN	98ARH99048A				

# 8 Pinout

# 8.1 K20 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

48	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
LQFP -QFN											
1	VDD	VDD	VDD								
2	VSS	VSS	VSS								
3	USB0_DP	USB0_DP	USB0_DP								
4	USB0_DM	USB0_DM	USB0_DM								
5	VOUT33	VOUT33	VOUT33								
6	VREGIN	VREGIN	VREGIN								
7	ADC0_DP0	ADC0_DP0	ADC0_DP0								
8	ADC0_DM0	ADC0_DM0	ADC0_DM0								
9	VDDA	VDDA	VDDA								
10	VREFH	VREFH	VREFH								
11	VREFL	VREFL	VREFL								
12	VSSA	VSSA	VSSA								
13	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5								
14	XTAL32	XTAL32	XTAL32								
15	EXTAL32	EXTAL32	EXTAL32								
16	VBAT	VBAT	VBAT								
17	PTAO	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
18	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UARTO_RX	FTM0_CH6				JTAG_TDI	EZP_DI
19	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UARTO_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
20	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UARTO_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
21	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
22	VDD	VDD	VDD								
23	VSS	VSS	VSS								

## 8.2 K20 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.



Figure 23. K20 48 LQFP/QFN Pinout Diagram

# 9 Revision History

The following table provides a revision history for this document.