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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk20dx128vlf5

Table of Contents

1 Ordering parts.....	3	5.4.1 Thermal operating requirements.....	21
1.1 Determining valid orderable parts.....	3	5.4.2 Thermal attributes.....	21
2 Part identification.....	3	6 Peripheral operating requirements and behaviors.....	22
2.1 Description.....	3	6.1 Core modules.....	22
2.2 Format.....	3	6.1.1 JTAG electricals.....	22
2.3 Fields.....	3	6.2 System modules.....	25
2.4 Example.....	4	6.3 Clock modules.....	25
3 Terminology and guidelines.....	4	6.3.1 MCG specifications.....	25
3.1 Definition: Operating requirement.....	4	6.3.2 Oscillator electrical specifications.....	27
3.2 Definition: Operating behavior.....	5	6.3.3 32 kHz Oscillator Electrical Characteristics.....	29
3.3 Definition: Attribute.....	5	6.4 Memories and memory interfaces.....	30
3.4 Definition: Rating.....	6	6.4.1 Flash electrical specifications.....	30
3.5 Result of exceeding a rating.....	6	6.4.2 EzPort Switching Specifications.....	34
3.6 Relationship between ratings and operating requirements.....	6	6.5 Security and integrity modules.....	35
3.7 Guidelines for ratings and operating requirements.....	7	6.6 Analog.....	35
3.8 Definition: Typical value.....	7	6.6.1 ADC electrical specifications.....	35
3.9 Typical value conditions.....	8	6.6.2 CMP and 6-bit DAC electrical specifications.....	40
4 Ratings.....	9	6.6.3 Voltage reference electrical specifications.....	43
4.1 Thermal handling ratings.....	9	6.7 Timers.....	44
4.2 Moisture handling ratings.....	9	6.8 Communication interfaces.....	44
4.3 ESD handling ratings.....	9	6.8.1 USB electrical specifications.....	44
4.4 Voltage and current operating ratings.....	9	6.8.2 USB DCD electrical specifications.....	45
5 General.....	10	6.8.3 USB VREG electrical specifications.....	45
5.1 AC electrical characteristics.....	10	6.8.4 DSPI switching specifications (limited voltage range).....	46
5.2 Nonswitching electrical specifications.....	11	6.8.5 DSPI switching specifications (full voltage range).....	47
5.2.1 Voltage and current operating requirements.....	11	6.8.6 I2C switching specifications.....	49
5.2.2 LVD and POR operating requirements.....	11	6.8.7 UART switching specifications.....	49
5.2.3 Voltage and current operating behaviors.....	12	6.8.8 I2S/SAI Switching Specifications.....	49
5.2.4 Power mode transition operating behaviors.....	13	6.9 Human-machine interfaces (HMI).....	54
5.2.5 Power consumption operating behaviors.....	14	6.9.1 TSI electrical specifications.....	54
5.2.6 EMC radiated emissions operating behaviors.....	18	7 Dimensions.....	55
5.2.7 Designing with radiated emissions in mind.....	19	7.1 Obtaining package dimensions.....	55
5.2.8 Capacitance attributes.....	19	8 Pinout.....	56
5.3 Switching specifications.....	19	8.1 K20 Signal Multiplexing and Pin Assignments.....	56
5.3.1 Device clock specifications.....	19	8.2 K20 Pinouts.....	58
5.3.2 General switching specifications.....	20	9 Revision History.....	58
5.4 Thermal specifications.....	21		

Symbol	Description	Min.	Max.	Unit
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	$V_{DD} + 0.3$	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB_DP}	USB_DP input voltage	-0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

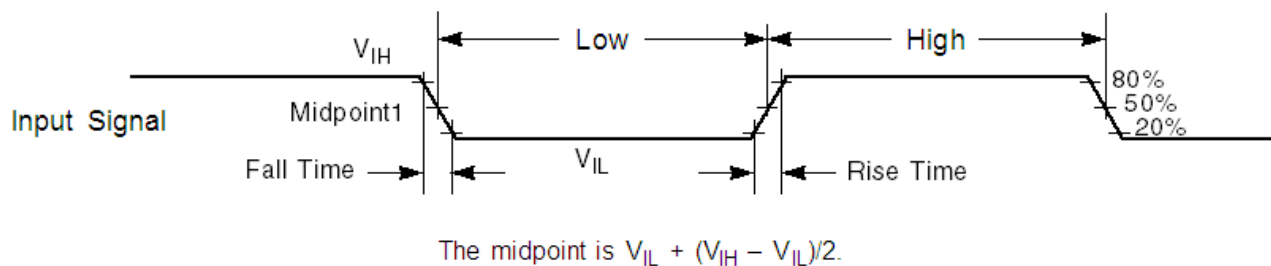


Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are configured for fast slew rate ($\text{PORTx_PCRn[SRE]}=0$), and
 - are configured for high drive strength ($\text{PORTx_PCRn[DSE]}=1$)
2. input pins
 - have their passive filter disabled ($\text{PORTx_PCRn[PFE]}=0$)

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	I/O pin DC injection current — single pin <ul style="list-style-type: none"> $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection) 	-3 —	— +3	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> Negative current injection Positive current injection 	-25 —	— +25	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} ($=V_{SS}-0.3\text{V}$) and V_{IN} is less than V_{AIO_MAX} ($=V_{DD}+0.3\text{V}$) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	• VLLS0 → RUN	—	130	μs	
	• VLLS1 → RUN	—	130	μs	
	• VLLS2 → RUN	—	70	μs	
	• VLLS3 → RUN	—	70	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	—	5.2	μs	
	• STOP → RUN	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash	—	13.7	15.1	mA	2
		—	13.9	15.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash	—	16.1	18.2	mA	3, 4
		—	16.3	17.7	mA	
		—	16.7	18.4	mA	
		—	16.7	18.4	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.5	8.4	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.6	6.4	mA	5

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	867	—	μA	6
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	509	—	μA	8
I _{DD_STOP}	Stop mode current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	310	426	μA	
		—	384	458	μA	
		—	629	1100	μA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	3.5	22.6	μA	
		—	20.7	52.9	μA	
		—	85	220	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	2.1	3.7	μA	
		—	7.7	43.1	μA	
		—	32.2	68	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	1.5	2.9	μA	
		—	4.8	22.5	μA	
		—	20	37.8	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	1.4	2.8	μA	
		—	4.1	19.2	μA	
		—	17.3	32.4	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.678	1.3	μA	
		—	2.8	13.6	μA	
		—	13.6	24.5	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.367	1.0	μA	
		—	2.4	13.3	μA	
		—	13.2	24.1	μA	

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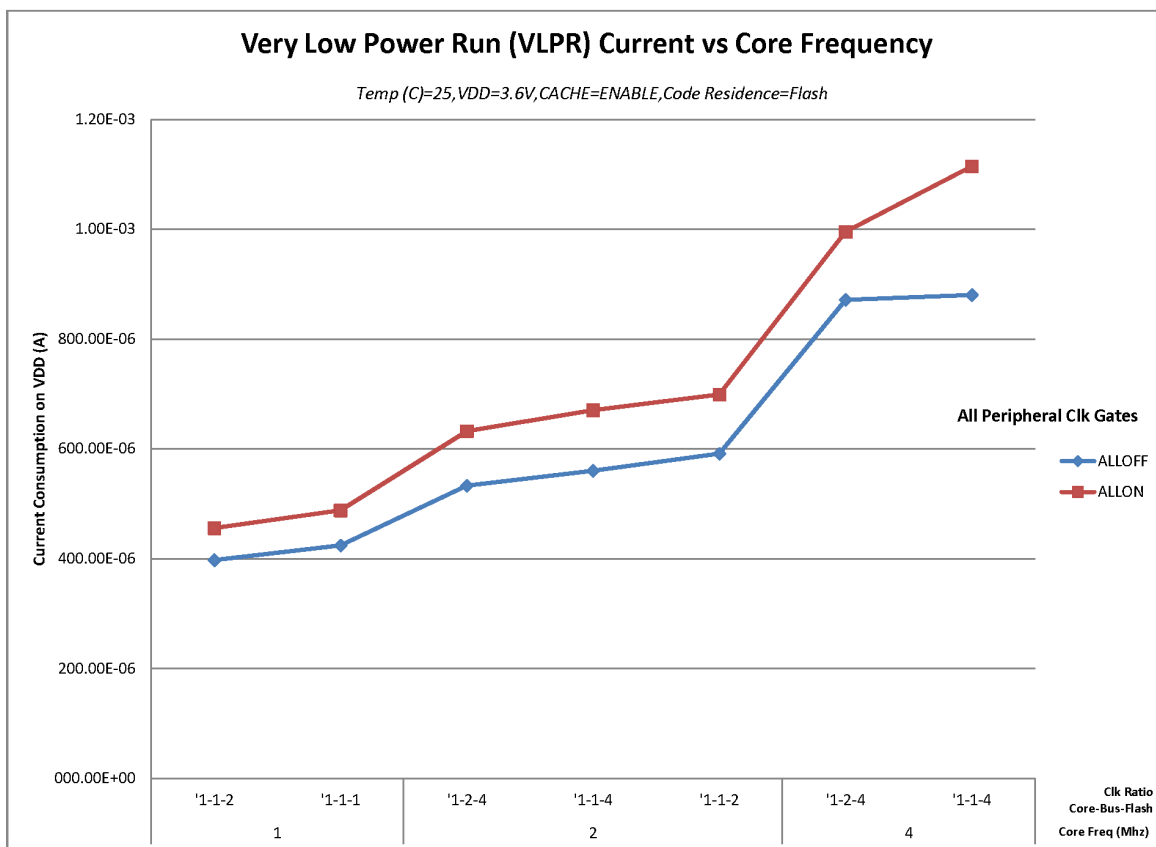


Figure 3. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 64LQFP

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	19	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	21	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	19	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	11	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported

emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{OSC} = 12\text{ MHz}$ (crystal), $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to <http://www.freescale.com>.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	

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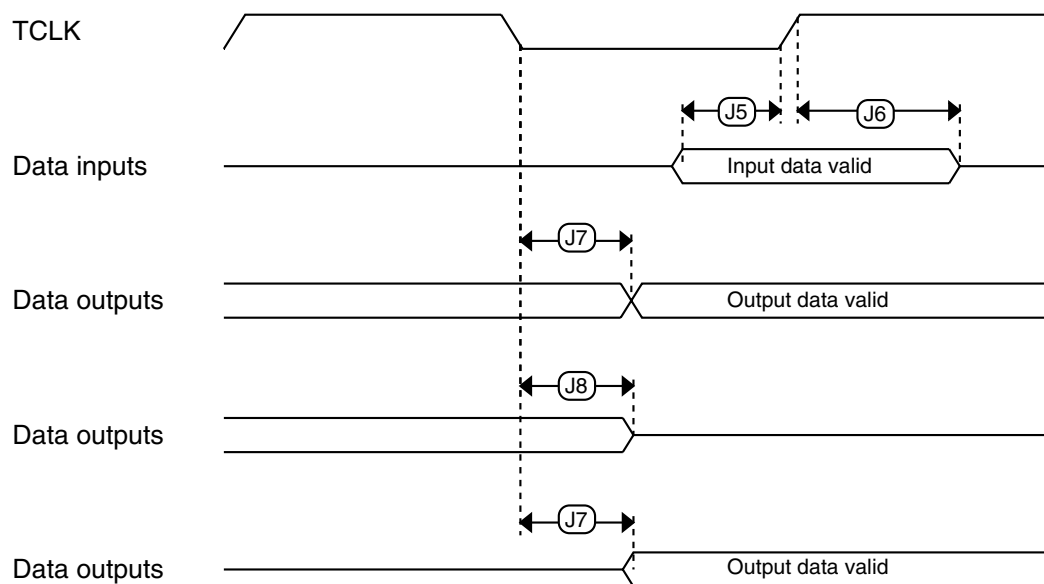


Figure 5. Boundary scan (JTAG) timing

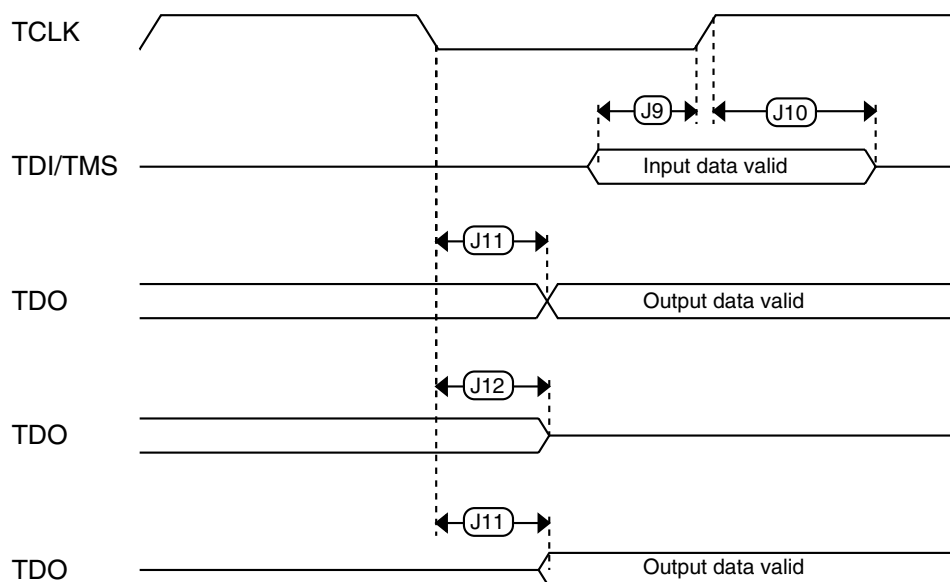
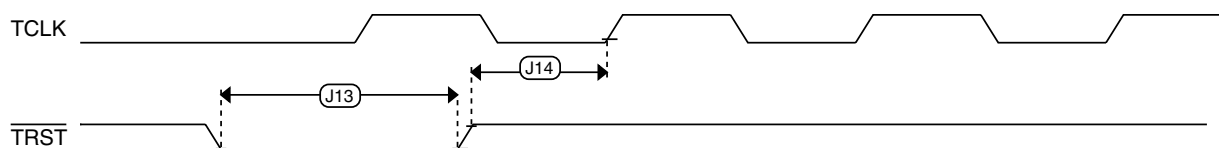


Figure 6. Test Access Port timing

Figure 7. $\overline{\text{TRST}}$ timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 13. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 3	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	—	$\%f_{\text{dco}}$	1
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$f_{\text{loc_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints_t}}$	—	—	kHz	
$f_{\text{loc_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints_t}}$	—	—	kHz	
FLL						

Table continues on the next page...

Table 14. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.4. When low power mode is selected, R_F is integrated and must not be attached externally.

Table 16. 32kHz oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32kHz oscillator frequency specifications

Table 17. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 18. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp gm4}$	Longword Program high-voltage time	—	7.5	18	μ s	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 19. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk32k}$	Read 1s Block execution time	—	—	0.5	ms	
$t_{rd1blk128k}$	<ul style="list-style-type: none"> 32 KB data flash 128 KB program flash 	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
$t_{ersblk32k}$	Erase Flash Block execution time	—	55	465	ms	2
$t_{ersblk128k}$	<ul style="list-style-type: none"> 32 KB data flash 128 KB program flash 	—	61	495	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgmsec512}$	Program Section execution time	—	4.7	—	ms	
$t_{pgmsec1k}$	<ul style="list-style-type: none"> 512 B flash 1 KB flash 	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	115	1000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
$t_{pgmpart32k}$	Program Partition for EEPROM execution time	—	70	—	ms	
$t_{setramff}$	Set FlexRAM Function execution time:	—	50	—	μs	
$t_{setram8k}$	<ul style="list-style-type: none"> Control Code 0xFF 8 KB EEPROM backup 	—	0.3	0.5	ms	
$t_{setram32k}$	<ul style="list-style-type: none"> 32 KB EEPROM backup 	—	0.7	1.0	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
$t_{eewr8b8k}$	Byte-write to FlexRAM execution time:	—	340	1700	μs	
$t_{eewr8b16k}$	<ul style="list-style-type: none"> 8 KB EEPROM backup 16 KB EEPROM backup 	—	385	1800	μs	
$t_{eewr8b32k}$	<ul style="list-style-type: none"> 32 KB EEPROM backup 	—	475	2000	μs	

Table continues on the next page...

Table 19. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Word-write to FlexRAM for EEPROM operation						
$t_{\text{eewr16bers}}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
$t_{\text{eewr16b8k}}$	Word-write to FlexRAM execution time: • 8 KB EEPROM backup	—	340	1700	μs	
$t_{\text{eewr16b16k}}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr16b32k}}$	• 32 KB EEPROM backup	—	475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{\text{eewr32bers}}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
$t_{\text{eewr32b8k}}$	Longword-write to FlexRAM execution time: • 8 KB EEPROM backup	—	545	1950	μs	
$t_{\text{eewr32b16k}}$	• 16 KB EEPROM backup	—	630	2050	μs	
$t_{\text{eewr32b32k}}$	• 32 KB EEPROM backup	—	810	2250	μs	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash high voltage current behaviors

Table 20. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{\text{DD_PGM}}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{\text{DD_ERS}}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 21. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
$t_{\text{nv mretp10k}}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{\text{nv mretp1k}}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{\text{nv mcycp}}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{\text{nv mretd10k}}$	Data retention after up to 10 K cycles	5	50	—	years	

Table continues on the next page...

Table 21. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
$t_{\text{nvmretd1k}}$	Data retention after up to 1 K cycles	20	100	—	years	
n_{nvmcyed}	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{\text{nvmretee100}}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{\text{nvmretee10}}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{\text{nvmwree16}}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{\text{nvmwree128}}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{\text{nvmwree512}}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{\text{nvmwree4k}}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{\text{nvmwree8k}}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$.
3. Write endurance represents the number of writes to each FlexRAM location at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write_efficiency} \times n_{\text{nvmcyed}}$$

where

- Writes_FlexRAM — minimum number of writes to each FlexRAM location

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32	82	95	—	dB	7
		16 bit single-ended mode • Avg=32	78	90	—	dB	
E_{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	–40°C to 105°C	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25°C	—	719	—	mV	

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.

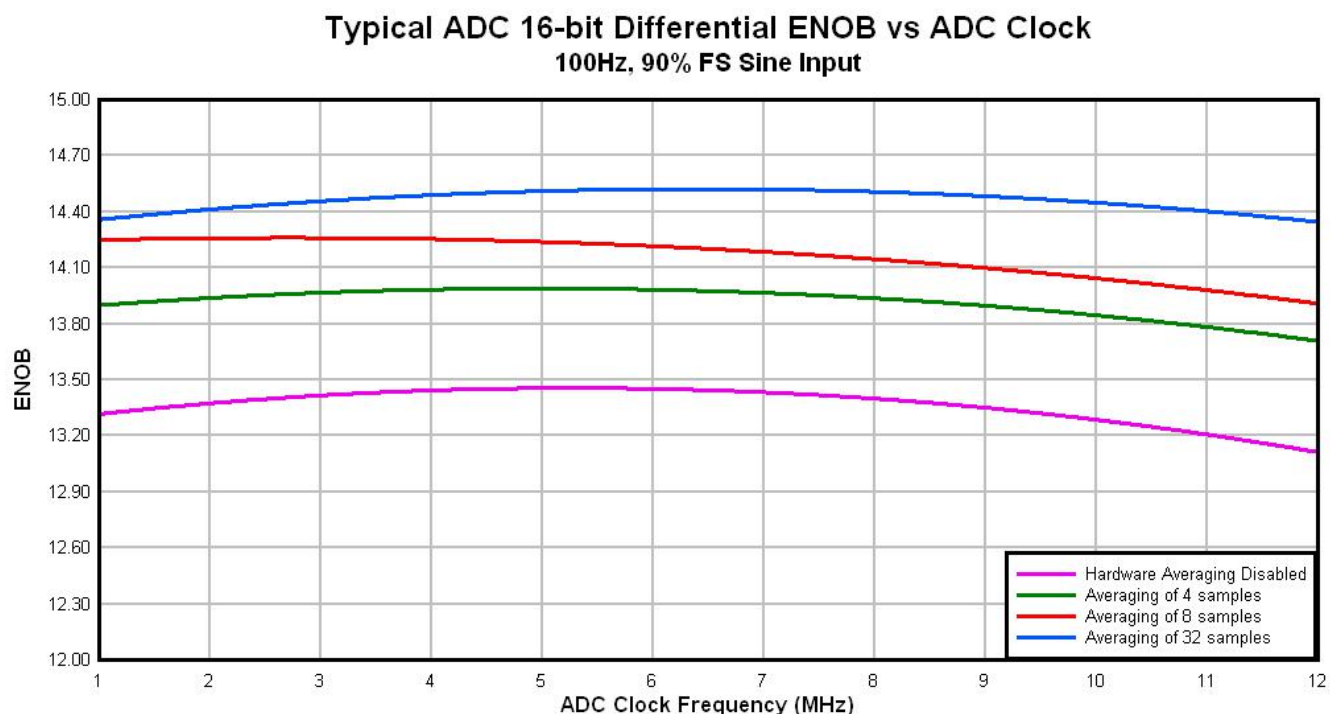


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit differential mode

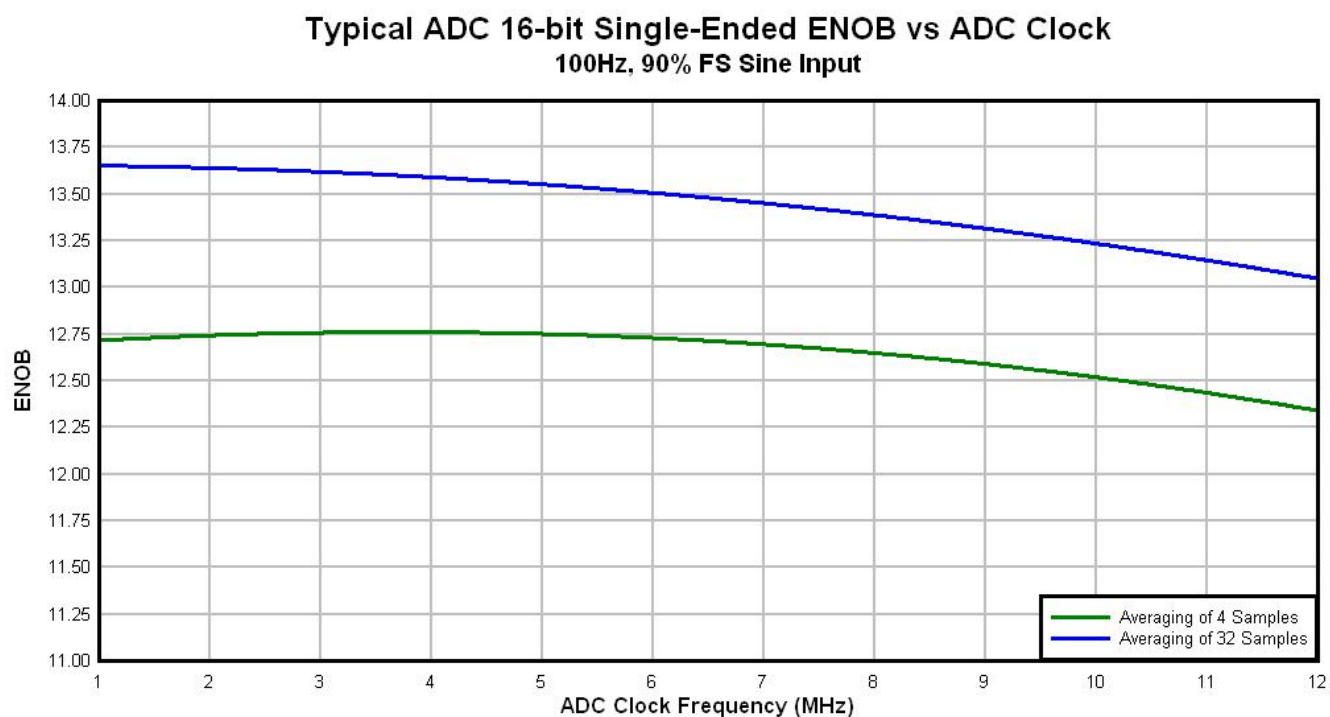


Figure 12. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

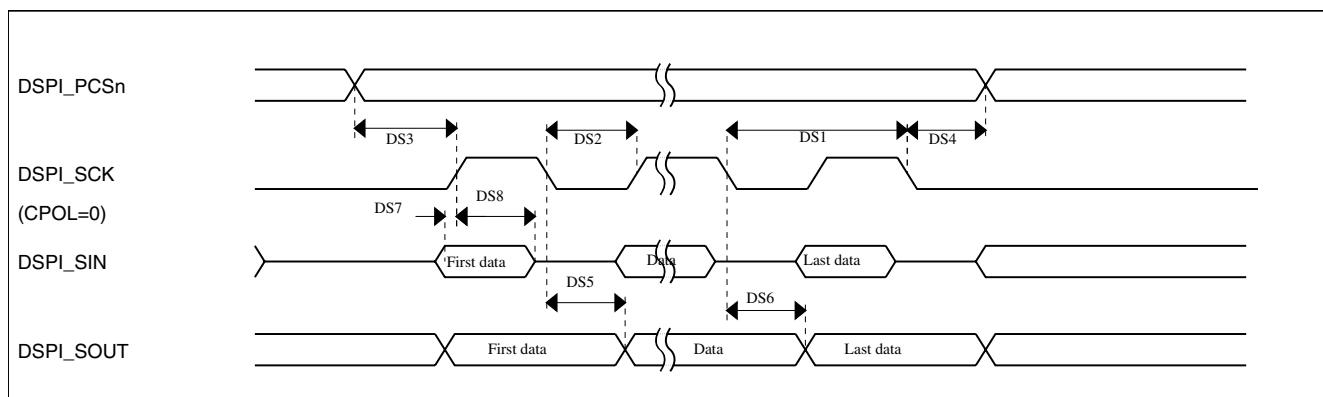


Figure 15. DSPI classic SPI timing — master mode

Table 33. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SS to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{DSPI_SS}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{DSPI_SS}$ inactive to DSPI_SOUT not driven	—	14	ns

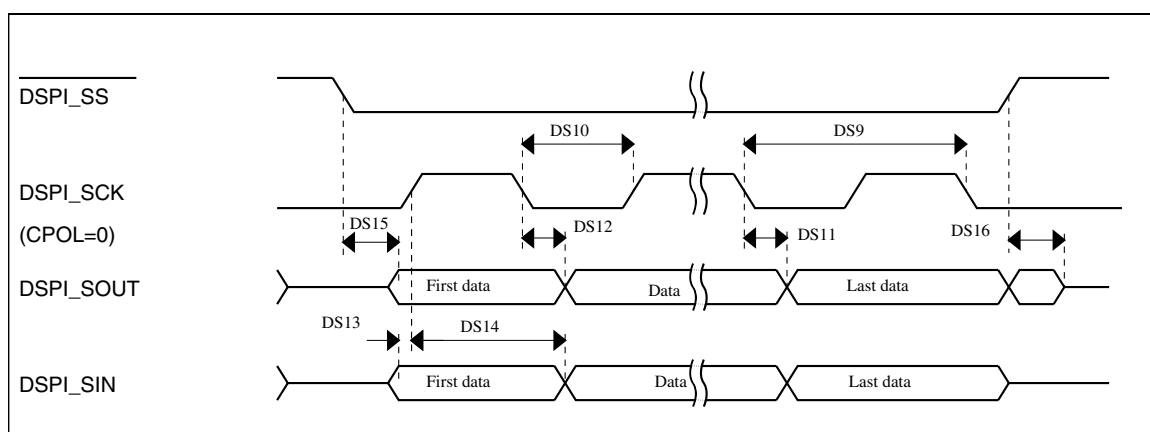


Figure 16. DSPI classic SPI timing — slave mode

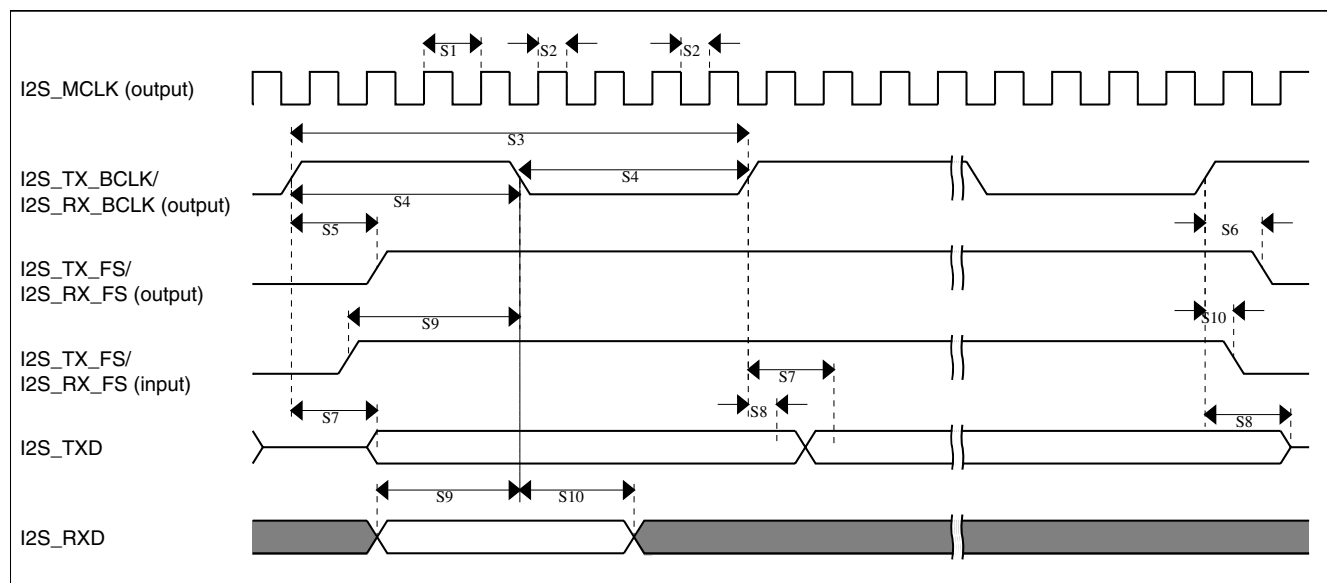


Figure 19. I2S/SAI timing — master modes

Table 37. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

8 Pinout

8.1 K20 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

48 LQFP -QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	VDD	VDD	VDD								
2	VSS	VSS	VSS								
3	USB0_DP	USB0_DP	USB0_DP								
4	USB0_DM	USB0_DM	USB0_DM								
5	VOUT33	VOUT33	VOUT33								
6	VREGIN	VREGIN	VREGIN								
7	ADC0_DP0	ADC0_DP0	ADC0_DP0								
8	ADC0_DM0	ADC0_DM0	ADC0_DM0								
9	VDDA	VDDA	VDDA								
10	VREFH	VREFH	VREFH								
11	VREFL	VREFL	VREFL								
12	VSSA	VSSA	VSSA								
13	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5								
14	XTAL32	XTAL32	XTAL32								
15	EXTAL32	EXTAL32	EXTAL32								
16	VBAT	VBAT	VBAT								
17	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSIO_CH1	PTA0	UART0_CTS_b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
18	PTA1	JTAG_TDI/ EZP_DI	TSIO_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
19	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSIO_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
20	PTA3	JTAG_TMS/ SWD_DIO	TSIO_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
21	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSIO_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
22	VDD	VDD	VDD								
23	VSS	VSS	VSS								

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