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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l063c8t6

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2 Description

The ultra-low-power STM32L063x8 microcontrollers incorporate the connectivity power of the universal serial bus (USB 2.0 crystal-less) with the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (64 Kbytes of Flash program memory, 2 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L063x8 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L063x8 devices offer several analog features, one 12-bit ADC with hardware oversampling, one DAC, two ultra-low-power comparators, AES, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers and one basic timer, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L063x8 devices embed standard and advanced communication interfaces: up to two I2C, two SPIs, one I2S, two USARTs, a low-power UART (LPUART), and a crystal-less USB. The devices offer up to 24 capacitive sensing channels to simply add touch sensing functionality to any application.

The STM32L063x8 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, their integrated LCD controller has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L063x8 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



- **Stop mode without RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode. The LCD is not stopped automatically by entering Stop mode.

**Table 4. Functionalities depending on the working mode
(from Run/active down to standby) ⁽¹⁾**

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	⁽²⁾		--	
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
LCD	O	O	O	O	O		--	
USB	O	O	--	--	--	O	--	
USART	O	O	O	O	O ⁽³⁾	O	--	
LPUART	O	O	O	O	O ⁽³⁾	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	O	O	O ⁽⁴⁾	O	--	
ADC	O	O	--	--	--		--	

3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L063x8 are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L063x8 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

- **Startup clock**

After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled. Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output)**

It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

3.8 Memories

The STM32L063x8 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 32 or 64 Kbytes of embedded Flash program memory
 - 2 Kbytes of data EEPROM
 - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0:** no protection
- **Level 1:** memory readout protected.
The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2:** chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA5, PA6, PA7) or SPI2 (PB12, PB13, PB14, PB15), USART1 (PA9, PA10) or USART2 (PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.

Table 11. STM32L063x8 I²C implementation (continued)

I2C features ⁽¹⁾	I2C1	I2C2
SMBus	X	-
Wakeup from STOP	X	-

1. X = supported.

2. See [Table 15: STM32L063x8 pin definitions](#) for the list of I/Os that feature Fast Mode Plus capability

3.20.2 Universal synchronous/asynchronous receiver transmitter (USART)

The two USART interfaces (USART1, USART2) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. They also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

[Table 12](#) for the supported modes and features of USART interfaces.

Table 12. USART implementation

USART modes/features ⁽¹⁾	USART1 and USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode ⁽²⁾	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection (4 modes)	X
Driver Enable	X

1. X = supported.

2. This mode allows using the USART as an SPI master.

3.20.3 Low-power universal asynchronous receiver transmitter (LPUART)

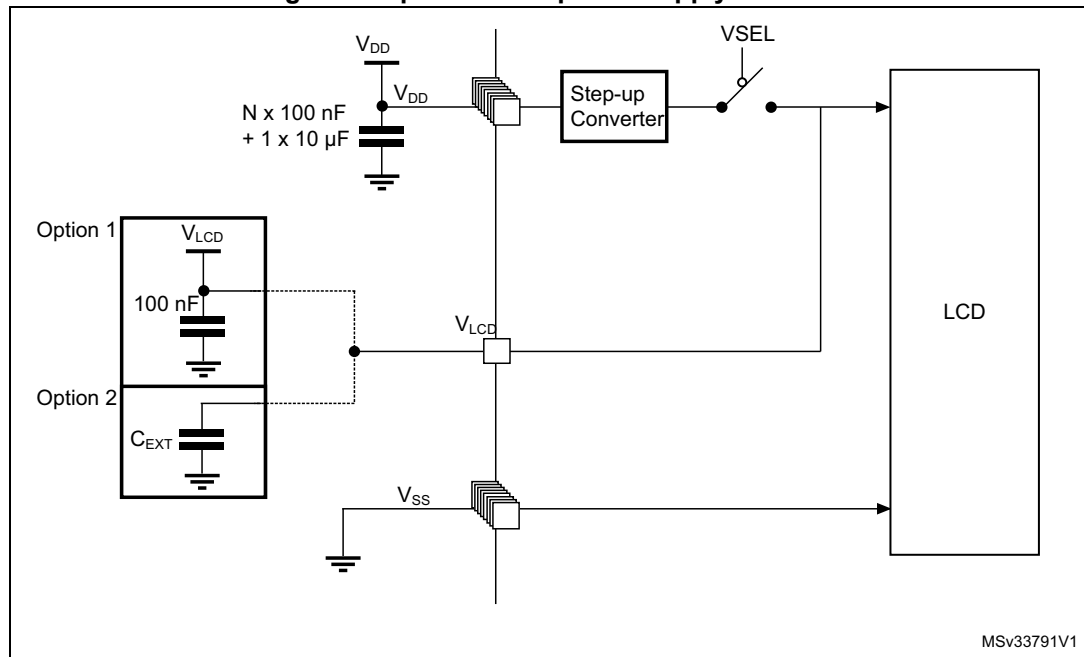
The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire

Table 15. STM32L063x8 pin definitions (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48	LQFP64						
18	26	PB0	I/O	FT	-	EVENTOUT, LCD_SEG5, TSC_G3_IO2	LCD_VLCD3, ADC_IN8, VREF_OUT
19	27	PB1	I/O	FT	-	LCD_SEG6, TSC_G3_IO3, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
20	28	PB2	I/O	FT	-	LPTIM1_OUT, TSC_G3_IO4	LCD_VLCD1
21	29	PB10	I/O	FT	-	LCD_SEG10, TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL	-
22	30	PB11	I/O	FT	-	EVENTOUT, LCD_SEG11, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA	-
23	31	VSS	S		-	-	-
24	32	VDD	S		-	-	-
25	33	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LCD_SEG12, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	LCD_VLCD2
26	34	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, LCD_SEG13, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
27	35	PB14	I/O	FTf	-	SPI2_MISO/I2S2_MCK, LCD_SEG14, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
28	36	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, LCD_SEG15, RTC_REFIN	-
-	37	PC6	I/O	FT	-	TIM22_CH1, LCD_SEG24, TSC_G8_IO1	-

6.1.7 Optional LCD power supply scheme

Figure 9. Optional LCD power supply scheme



1. Option 1: LCD power supply is provided by a dedicated V_{LCD} supply source, V_{SEL} switch is open.
2. Option 2: LCD power supply is provided by the internal step-up converter, V_{SEL} switch is closed, an external capacitance is needed for correct behavior of this converter.

6.1.8 Current consumption measurement

Figure 10. Current consumption measurement scheme

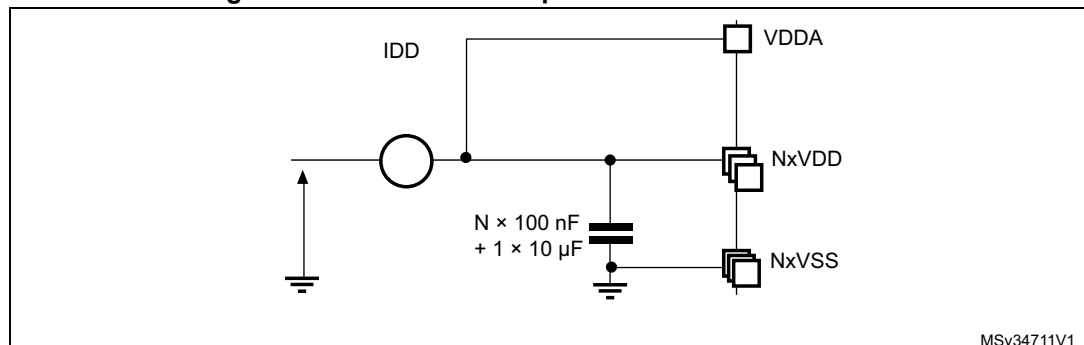


Table 25. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.

2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in [Table 27](#) are based on characterization results, unless otherwise specified.

Table 26. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C $V_{DDA} = 3\text{ V}$	0x1FF8 0078 - 0x1FF8 0079

Table 27. Embedded internal reference voltage⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}^{(2)}$	Internal reference voltage	$-40\text{ °C} < T_J < +125\text{ °C}$	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value ⁽³⁾	Including uncertainties due to ADC and V_{DDA} values	-	-	±5	mV
$T_{Coeff}^{(4)}$	Temperature coefficient	$-40\text{ °C} < T_J < +125\text{ °C}$	-	25	100	ppm/°C
$A_{Coeff}^{(4)}$	Long-term stability	1000 hours, $T = 25\text{ °C}$	-	-	1000	ppm
$V_{DDCoeff}^{(4)}$	Voltage coefficient	$3.0\text{ V} < V_{DDA} < 3.6\text{ V}$	-	-	2000	ppm/V
$T_{S_vrefint}^{(4)(5)}$	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
$T_{ADC_BUF}^{(4)}$	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
$I_{BUF_ADC}^{(4)}$	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
$I_{VREF_OUT}^{(4)}$	VREF_OUT output current ⁽⁶⁾	-	-	-	1	µA
$C_{VREF_OUT}^{(4)}$	VREF_OUT output load	-	-	-	50	pF

Table 36. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
I _{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	T _A = - 40 to 25°C	1.3	1.7
			T _A = 55 °C	-	2.9
			T _A = 85 °C	-	3.3
			T _A = 105 °C	-	4.1
			T _A = 125 °C	-	8.5
		Independent watchdog and LSI off	T _A = - 40 to 25°C	0.29	0.6
			T _A = 55 °C	0.32	0.9
			T _A = 85 °C	0.5	2.3
			T _A = 105 °C	0.94	3
			T _A = 125 °C	2.6	7

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

Table 37. Average current consumption during Wakeup

Symbol	parameter	System frequency	Current consumption during wakeup	Unit
I _{DD} (Wakeup from Stop)	Supply current during Wakeup from Stop mode	HSI	1	mA
		HSI/4	0,7	
		MSI clock = 4,2 MHz	0,7	
		MSI clock = 1,05 MHz	0,4	
		MSI clock = 65 KHz	0,1	
I _{DD} (Reset)	Reset pin pulled down	-	0,21	
I _{DD} (Power-up)	BOR on	-	0,23	
I _{DD} (Wakeup from StandBy)	With Fast wakeup set	MSI clock = 2,1 MHz	0,5	
	With Fast wakeup disabled	MSI clock = 2,1 MHz	0,12	

Low-speed external user clock generated from an external source

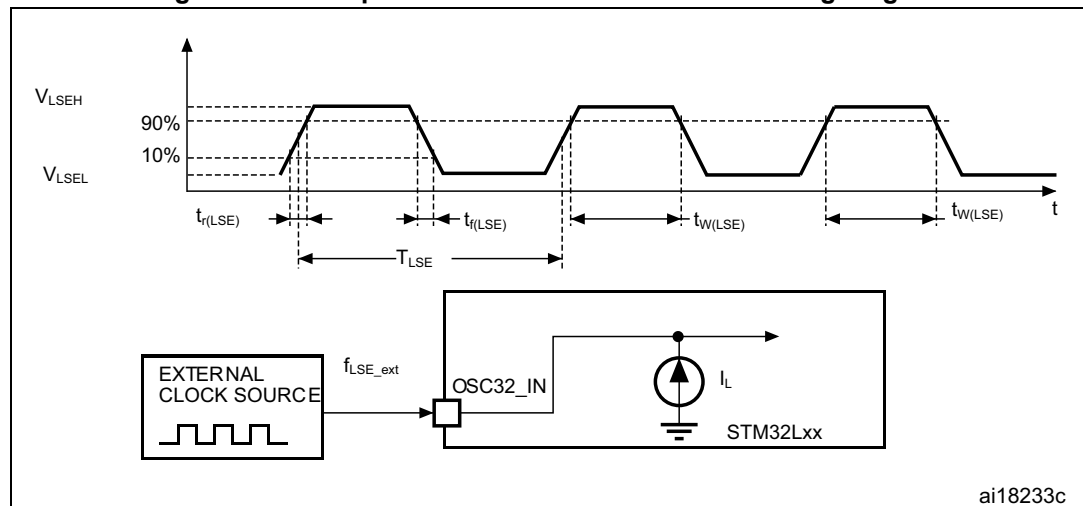
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 24](#).

Table 42. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design, not tested in production

Figure 17. Low-speed external clock source AC timing diagram



ai18233c

The analog spike filter is compliant with I²C timings requirements only for the following voltage ranges:

- Fast mode Plus: $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ and voltage scaling Range 1
- Fast mode:
 - $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ and voltage scaling Range 1 or Range 2.
 - $V_{DD} < 2\text{ V}$, voltage scaling Range 1 or Range 2, $C_{load} < 200\text{ pF}$.

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

Note: In Standard mode, no spike filter is required.

Table 71. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	Range 1	50 ⁽²⁾	100 ⁽³⁾	ns
		Range 2		-	
		Range 3		-	

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

Table 72. USART/LPUART characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode	Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	μs
		Stop mode with main regulator in Run mode, Range 1	-	8.1	
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 24](#).

Refer to [Section 6.3.12: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 73. SPI characteristics in voltage Range 1 ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter $1.71 < V_{DD} < 3.6V$	-	-	12 ⁽²⁾	
		Slave mode Transmitter $2.7 < V_{DD} < 3.6V$	-	-	16 ⁽²⁾	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4 \cdot T_{pclk}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2 \cdot T_{pclk}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{pclk} - 2$	T_{pclk}	$T_{pclk} + 2$	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	7	-	-	
$t_{h(SI)}$		Slave mode	3.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode $1.65 V < V_{DD} < 3.6 V$	-	18	41	
		Slave mode $2.7 V < V_{DD} < 3.6 V$	-	18	25	
		Master mode	-	4	7	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while $Duty_{(SCK)} = 50\%$.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 77. USB startup time

Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB transceiver startup time	1	μs

1. Guaranteed by design.

Table 78. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input levels					
V _{DD}	USB operating voltage	-	3.0	3.6	V
V _{DI} ⁽²⁾	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V _{CM} ⁽²⁾	Differential common mode range	Includes V _{DI} range	0.8	2.5	
V _{SE} ⁽²⁾	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V _{OL} ⁽³⁾	Static output level low	R _L of 1.5 kΩ to 3.6 V ⁽⁴⁾	-	0.3	V
V _{OH} ⁽³⁾	Static output level high	R _L of 15 kΩ to V _{SS} ⁽⁴⁾	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_{L} is the load connected on the USB drivers.

Table 80. LCD controller characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
$I_{LCD}^{(1)}$	Supply current at $V_{DD} = 2.2\text{ V}$	-	3.3	-	μA
	Supply current at $V_{DD} = 3.0\text{ V}$	-	3.1	-	
$R_{Htot}^{(2)}$	Low drive resistive network overall value	5.28	6.6	7.92	$\text{M}\Omega$
$R_L^{(2)}$	High drive resistive network total value	192	240	288	$\text{k}\Omega$
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4 V_{LCD}$	-	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3 V_{LCD}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2 V_{LCD}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3 V_{LCD}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4 V_{LCD}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	
$\Delta V_{xx}^{(3)}$	Segment/Common level voltage error $T_A = -40\text{ to }85\text{ }^\circ\text{C}$	-	-	± 50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.
2. Guaranteed by design.
3. Guaranteed by characterization results.

7.3 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

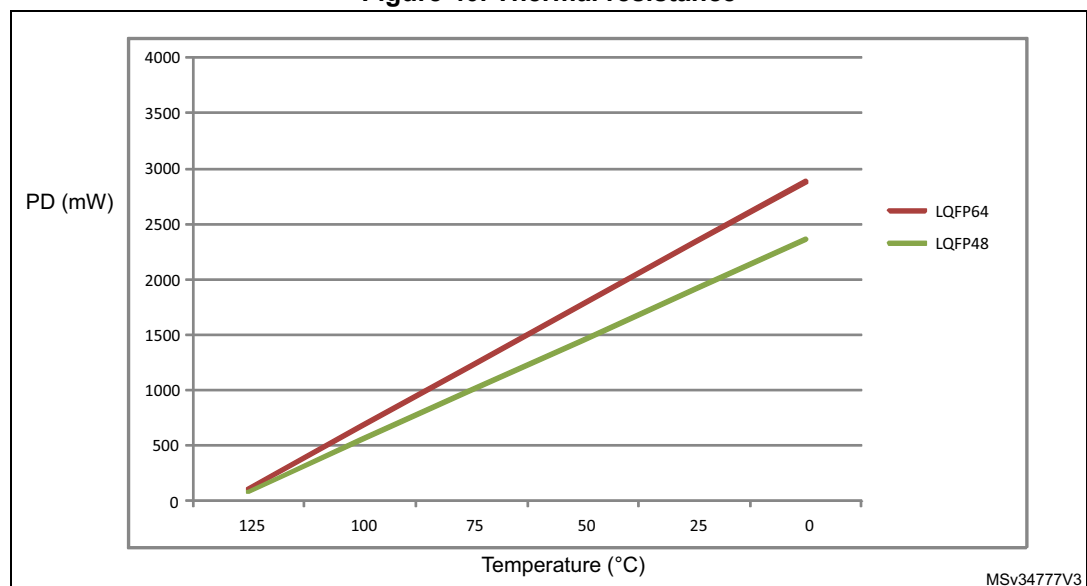
$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 83. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	

Figure 40. Thermal resistance



7.3.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 85. Document revision history (continued)

Date	Revision	Changes
22-Mar-2016	6	<p>Updated number of SPIs on cover page and in Table 1: Ultra-low-power STM32L063x8 device features and peripheral counts.</p> <p>Changed minimum comparator supply voltage to 1.65 V on cover page.</p> <p>Added number of fast and standard channels in Section 3.12: Analog-to-digital converter (ADC).</p> <p>Changed LCD_VLCD1 into LCD_VLCD2 in Section 3.13.2: VLCD voltage monitoring.</p> <p>Updated Section 3.20.2: Universal synchronous/asynchronous receiver transmitter (USART) and Section 3.20.4: Serial peripheral interface (SPI)/Inter-integrated sound (I2S) to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces.</p> <p>Added baudrate allowing to wake up the MCU from Stop mode in Section 3.20.2: Universal synchronous/asynchronous receiver transmitter (USART) and Section 3.20.3: Low-power universal asynchronous receiver transmitter (LPUART).</p> <p>In Section 6: Electrical characteristics, updated all the notes related to values guaranteed by characterization.</p> <p>Section 6.3.15: 12-bit ADC characteristics:</p> <ul style="list-style-type: none"> – Table 62: ADC characteristics: <ul style="list-style-type: none"> Distinction made between V_{DDA} for fast and standard channels; added note 1. Added note 4. related to R_{ADC}. Updated f_{TRIG}. Updated t_S and t_{CONV}. – Updated equation 1 description. – Updated Table 63: RAIN max for $f_{ADC} = 16$ MHz for $f_{ADC} = 16$ MHz and distinction made between fast and standard channels. <p>Added Table 72: USART/LPUART characteristics.</p> <p>Updated R_O and added Note 1. in Table 65: DAC characteristics.</p> <p>Updated Figure 39: LQFP48 marking example (package top view).</p>