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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l063r8t6

1 Introduction

The ultra-low-power STM32L063x8 are offered in 48- and 64-pin packages. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L063x8 microcontrollers suitable for a wide range of applications:

- Gas/water meters and industrial sensors
- Healthcare and fitness equipment
- Remote control and user interface
- PC peripherals, gaming, GPS equipment
- Alarm system, wired and wireless sensors, video intercom

This STM32L063x8 datasheet should be read in conjunction with the STM32L0x3xx reference manual (RM0367).

For information on the ARM® Cortex®-M0+ core please refer to the Cortex®-M0+ Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family.

2.1 Device overview

Table 1. Ultra-low-power STM32L063x8 device features and peripheral counts

Peripheral		STM32L063C8	STM32L063R8
Flash (Kbytes)		64	
Data EEPROM (Kbytes)		2	
RAM (Kbytes)		8	
AES		1	
Timers	General-purpose	3	
	Basic	1	
	LPTIMER	1	
RTC/SYSTICK/IWDG/WWDG		1/1/1/1	
Communication interfaces	SPI/I2S	4(2)[1]/1	
	I^2C	2	
	USART	2	
	LPUART	1	
	USB/(VDD_USB)	1/(1)	
GPIOs		37	51
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1	
12-bit synchronized ADC Number of channels		1 10	1 16
12-bit DAC Number of channels		1 1	
LCD COM x SEG		1 4x18	1 4x32 or 8x28
Comparators		2	
Capacitive sensing channels		17	24
Max. CPU frequency		32 MHz	
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option	
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C	
Packages		LQFP48	LQFP64

1. 2 SPI interfaces are USARTs operating in SPI master mode.

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

Table 2. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	Dynamic voltage scaling range	I/O operation	USB
V_{DD} = 1.65 to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance	Not functional
V_{DD} = 1.71 to 1.8 V(1)	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. To be USB compliant from the I/O voltage standpoint, the minimum V_{DD_USB} is 3.0 V.

Table 3. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L063x8 are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L063x8 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

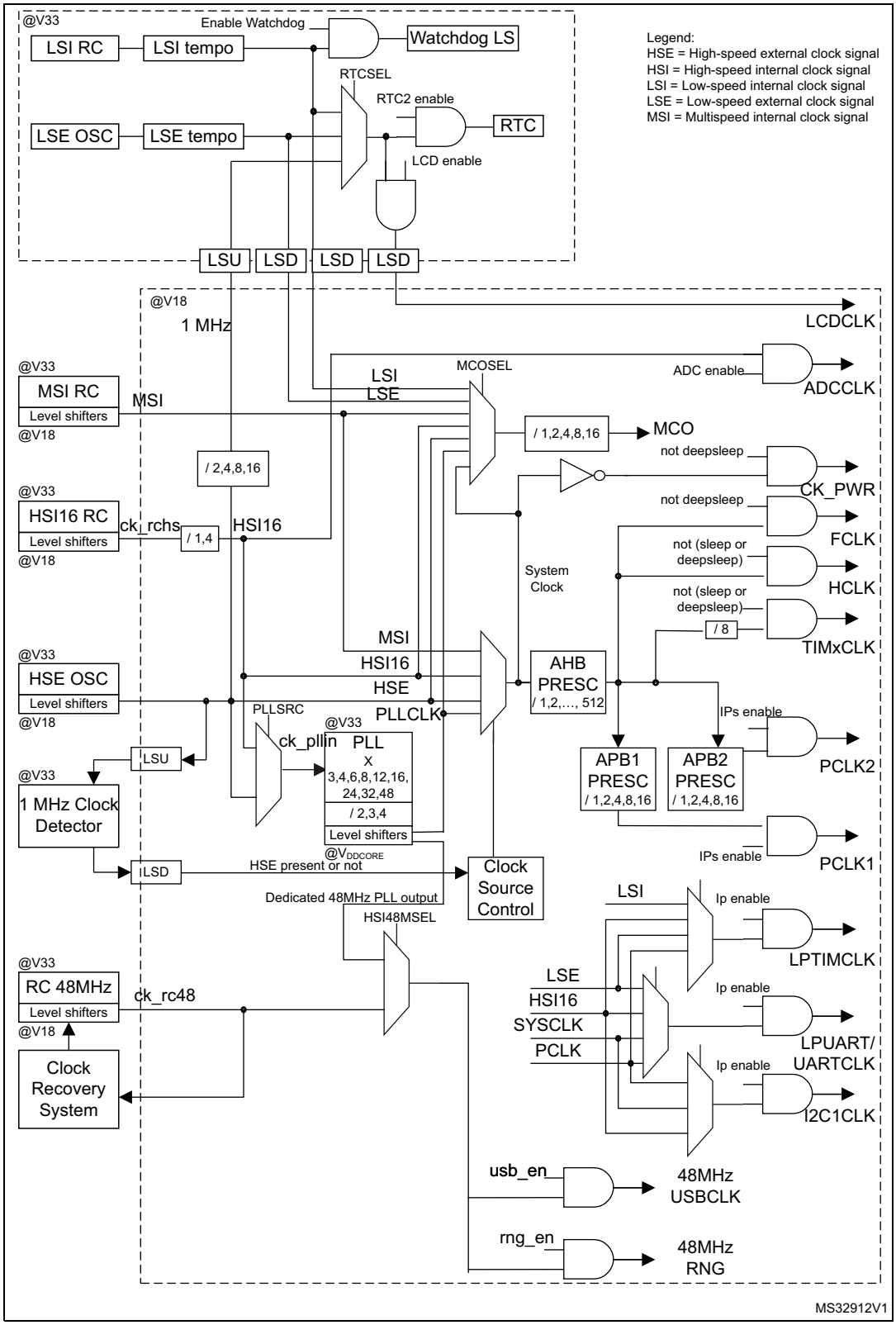
The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.


Legend:
HSE = High-speed external clock signal
HSI = High-speed internal clock signal
LSI = Low-speed internal clock signal
LSE = Low-speed external clock signal
MSI = Multispeed internal clock signal
@V33
Enable Watchdog
LSI RC
LSI tempo
Watchdog LS
RTCSEL
RTC2 enable
LSE OSC
LSE tempo
RTC
LCD enable
LSU
LSD
LSD
LSD
@V18
1 MHz
LCDCLK
@V33
MSI RC
Level shifters
@V18
MSI
LSI
LSE
MCOSEL
ADC enable
ADCCLK
/ 1,2,4,8,16
MCO
not deepsleep
CK_PWR
/ 2,4,8,16
@V33
HSI16 RC
Level shifters
@V18
ck_rchs
/ 1,4
HSI16
not deepsleep
FCLK
not (sleep or deepsleep)
System Clock
HCLK
not (sleep or deepsleep)
/ 8
TIMxCLK
MSI
HSI16
HSE
PLLCLK
@V33
HSE OSC
Level shifters
@V18
PLLSRC
ck_pllin
@V33
PLL
x
3,4,6,8,12,16, 24,32,48
/ 2,3,4
Level shifters
@VDDCORE
AHB PRESC
/ 1,2,..., 512
IPs enable
PCLK2
APB1 PRESC
/ 1,2,4,8,16
APB2 PRESC
/ 1,2,4,8,16
IPs enable
PCLK1
LSU
@V33
1 MHz Clock Detector
LSD
HSE present or not
Clock Source Control
Dedicated 48MHz PLL output
HSI48MSEL
LSI
Ip enable
LPTIMCLK
@V33
RC 48MHz
Level shifters
@V18
ck_rc48
LSE
HSI16
SYSCLK
PCLK
Ip enable
LPUART/ UARTCLK
Ip enable
I2C1CLK
Clock Recovery System
usb_en
48MHz USBCLK
rng_en
48MHz RNG
MS32912V1

3.20.5 Universal serial bus (USB)

The STM32L063x8 embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.21 Clock recovery system (CRS)

The STM32L063x8 embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.22 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.23 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 15. STM32L063x8 pin definitions (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48	LQFP64						
18	26	PB0	I/O	FT	-	EVENTOUT, LCD_SEG5, TSC_G3_IO2	LCD_VLCD3, ADC_IN8, VREF_OUT
19	27	PB1	I/O	FT	-	LCD_SEG6, TSC_G3_IO3, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
20	28	PB2	I/O	FT	-	LPTIM1_OUT, TSC_G3_IO4	LCD_VLCD1
21	29	PB10	I/O	FT	-	LCD_SEG10, TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL	-
22	30	PB11	I/O	FT	-	EVENTOUT, LCD_SEG11, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA	-
23	31	VSS	S		-	-	-
24	32	VDD	S		-	-	-
25	33	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LCD_SEG12, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	LCD_VLCD2
26	34	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, LCD_SEG13, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
27	35	PB14	I/O	FTf	-	SPI2_MISO/I2S2_MCK, LCD_SEG14, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
28	36	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, LCD_SEG15, RTC_REFIN	-
-	37	PC6	I/O	FT	-	TIM22_CH1, LCD_SEG24, TSC_G8_IO1	-

Table 20. Alternate function port H

Port	AF0
	USB
Port H	PH0	USB_CRS_SYNC
	PH1	-

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 33. Current consumption in Low-power run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals off, code executed from RAM, Flash switched off, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, f_{HCLK} = 32 kHz	T_A = − 40 to 25°C	8.5	10	µA
				T_A = 85 °C	11.5	48	
				T_A = 105 °C	15.5	53	
				T_A = 125 °C	27.5	130	
			MSI clock= 65 kHz, f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	10	15	
				T_A = 85 °C	15.5	50	
				T_A = 105 °C	19.5	54	
				T_A = 125 °C	31.5	130	
			MSI clock= 131 kHz, f_{HCLK} = 131 kHz	T_A = − 40 to 25°C	20	25	
				T_A = 55 °C	23	50	
				T_A = 85 °C	25.5	55	
				T_A = 105 °C	29.5	64	
				T_A = 125 °C	40	140	
		All peripherals off, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock= 65 kHz, f_{HCLK} = 32 kHz	T_A = − 40 to 25°C	22	28	
				T_A = 85 °C	26	68	
				T_A = 105 °C	31	75	
				T_A = 125 °C	44	95	
			MSI clock = 65 kHz, f_{HCLK} = 65 kHz	T_A = − 40 to 25°C	27.5	33	
				T_A = 85 °C	31.5	73	
				T_A = 105 °C	36.5	80	
				T_A = 125 °C	49	100	
			MSI clock = 131 kHz, f_{HCLK} = 131 kHz	T_A = − 40 to 25°C	39	46	
				T_A = 55 °C	41	80	
				T_A = 85 °C	44	86	
				T_A = 105 °C	49.5	100	
				T_A = 125 °C	60	120	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Table 39. Peripheral current consumption in Stop and Standby mode(1)

Symbol	Peripheral	Typical consumption, T_A = 25 °C		Unit
		V_{DD}=1.8 V	V_{DD}=3.0 V	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	µA
I_{REFINT}	-	-	1.4	
-	LSE Low drive(2)	0,1	0,1	
-	LPTIM1, Input 100 Hz	0,01	0,01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0,2	0,2	
-	RTC	0,3	0,48	
-	LCD1 (static duty)	0,15	0,15	µA
-	LCD1 (1/8 duty)	1,6	2,6	

1. LPTIM peripheral cannot operate in Standby mode.
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

6.3.9 Memory characteristics

RAM memory

Table 50. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 51. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	500	700	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 52. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{CYC}(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T_A = -40°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the conditions summarized in *Table 24*. All I/Os are CMOS and TTL compliant.

Table 58. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC, FT, FTf, RST I/Os	-	-	$0.3V_{DD}$	V
		BOOT0 pin	-	-	$0.14V_{DD}$ (1)	
V_{IH}	Input high level voltage	All I/Os	$0.7\ V_{DD}$	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis (2)	Standard I/Os	-	$10\%\ V_{DD}$ (3)	-	
		BOOT0 pin	-	0.01	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ All I/Os except for PA11, PA12, BOOT0 and FTf I/Os	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$, PA11 and PA12 I/Os	-	-	-50/+250	
		$V_{SS} \le V_{IN} \le V_{DD}$ FTf I/Os	-	-	±100	
		$V_{DD} \le V_{IN} \le 5$ V All I/Os except for PA11, PA12, BOOT0 and FTf I/Os	-	-	200	nA
		$V_{DD} \le V_{IN} \le 5$ V FTf I/Os	-	-	500	
		$V_{DD} \le V_{IN} \le 5$ V PA11, PA12 and BOOT0	-	-	10	µA
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by characterization.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 200 mV. Guaranteed by characterization results.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 21. V_{IH}/V_{IL} versus VDD (CMOS I/Os)

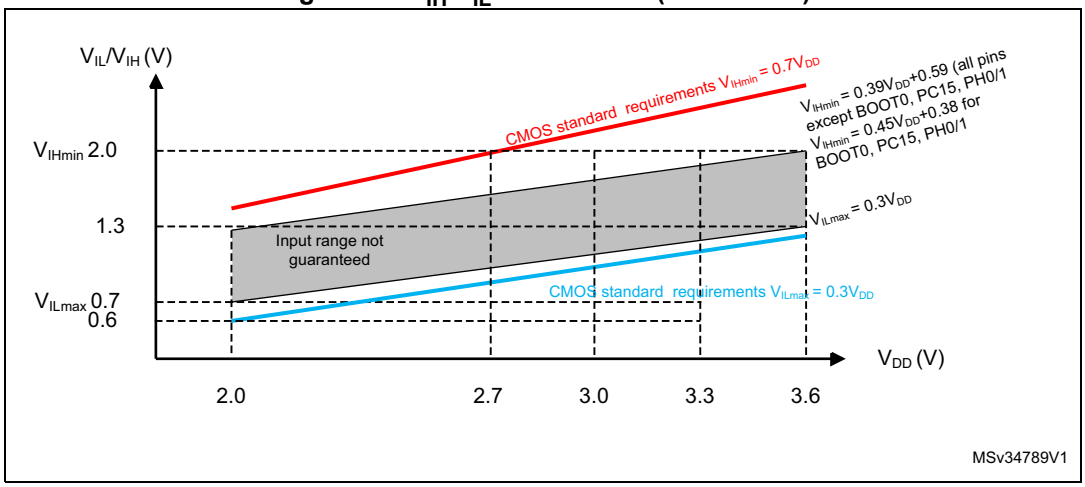
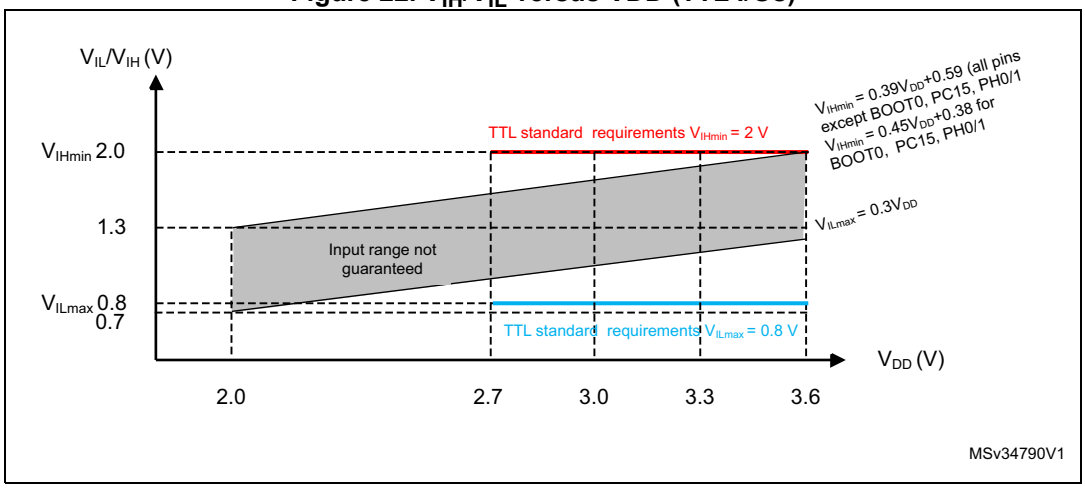


Figure 22. V_{IH}/V_{IL} versus VDD (TTL I/Os)



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±15 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 59*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 22*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 22*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*. All I/Os are CMOS and TTL compliant.

Table 59. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin	CMOS port(2), I_{IO} = +8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2), I_{IO} =+ 8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} (3)(4)	Output high level voltage for an I/O pin	TTL port(2), I_{IO} = -6 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = +15 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin	I_{IO} = -15 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.65 V ≤ V_{DD} < 3.6 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin	I_{IO} = -4 mA 1.65 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.45	-	
V_{OLFM+} (1)(4)	Output low level voltage for an FTf I/O pin in Fm+ mode	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 10 mA 1.65 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 22*. The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 22*. The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
4. Guaranteed by characterization results.

Table 65. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dGain/dT(1)	Gain error temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C DAC output buffer off	-10	-2	0	µV/°C
		V_{DDA} = 3.3V T_A = 0 to 50 °C DAC output buffer on	-40	-8	0	
TUE(1)	Total unadjusted error	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	12	30	LSB
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(8)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	-60	-35	dB

1. Guaranteed by design, not tested in production.
2. Connected between DAC_OUT and V_{SSA}.
3. Difference between two consecutive codes - 1 LSB.
4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
5. Difference between the value measured at Code (0x800) and the ideal value = V_{DDA}/2.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is off, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is on.
8. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Table 68. Comparator 1 characteristics (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V, V_{IN+} = 0 V, V_{IN-} = V_{REFINT}, T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 69. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V, T_A = 0 to 50 °C, V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	30	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (required for comparator operation) is not included.

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 24*.

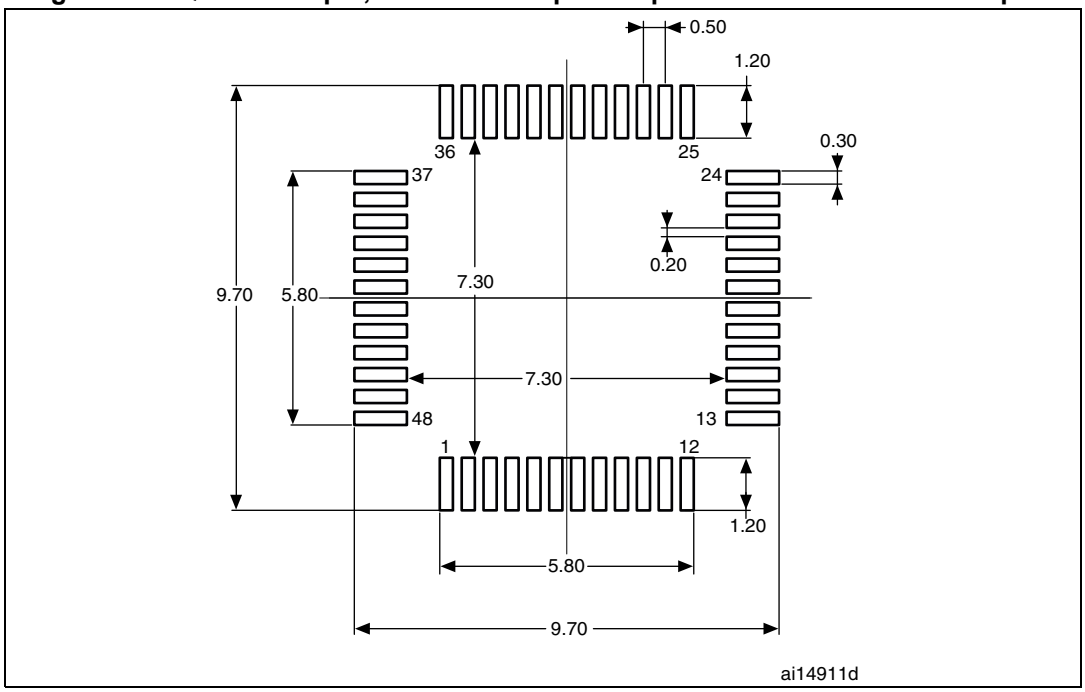
Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 73. SPI characteristics in voltage Range 1 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter $1.71<V_{DD}<3.6V$	-	-	12(2)	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$	-	-	16(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+ 2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	7	-	-	
$t_{h(SI)}$		Slave mode	3.5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode $1.65\ V<V_{DD}<3.6\ V$	-	18	41	
		Slave mode $2.7\ V<V_{DD}<3.6\ V$	-	18	25	
$t_{v(MO)}$		Master mode	-	4	7	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 38. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

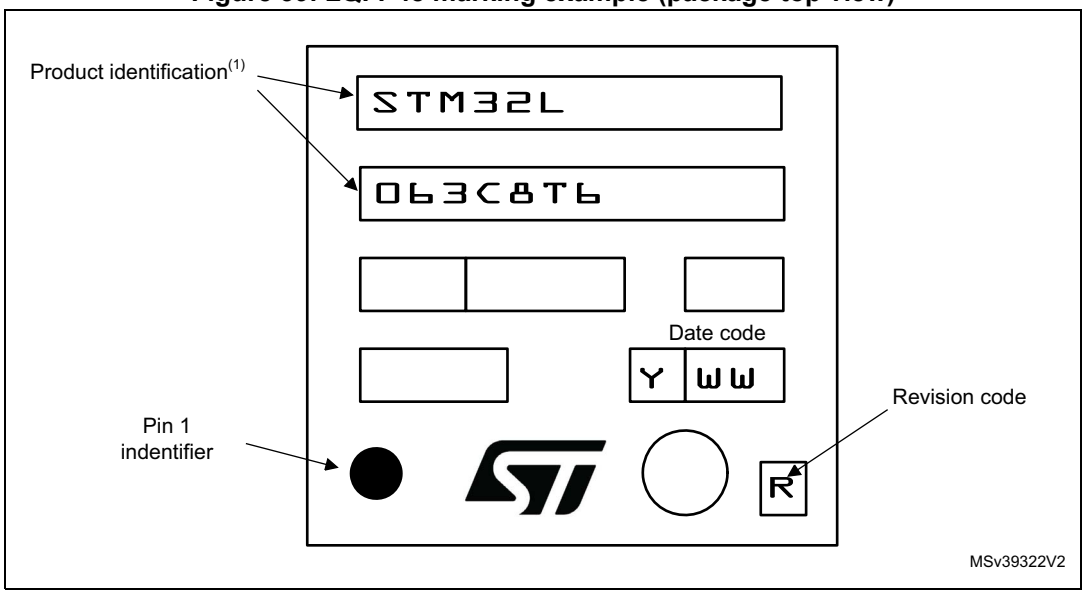


1. Dimensions are expressed in millimeters.

Device marking for LQFP48

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 39. LQFP48 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 85. Document revision history (continued)

Date	Revision	Changes
08-Sep-2015	5	Removed note 1 in *Table 1: Ultra-low-power STM32L063x8 device features and peripheral counts*. Updated all pinout/ballout schematics to highlight pin/ball supplied through VDD_USB. Updated current consumption in Run mode in *Section : Features*. Renamed BOOT1 into nBOOT1. Changed USARTx_RTS into USARTx_RTS_DE and LPUARTx_RTS into LPUARTx_RTS_DE. Updated VLCD in section Analog to digital converter (ADC). ADC no more available in Low-power run and Low-power Sleep modes in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)*. Updated *Figure 4: STM32L063x8 LQFP48 pinout - 7 x 7 mm* and *Figure 3: STM32L063x8 LQFP64 pinout - 10 x 10 mm*. Changed I/O structure for PC5 in *Table 15: STM32L063x8 pin definitions*. Updated VDD_USB in *Table 24: General operating conditions*. Changed temperature condition in *Table 7: Internal voltage reference measured values* and *Table 26: Embedded internal reference voltage calibration values*. Updated T_{Coeff} in *Table 27: Embedded internal reference voltage*. Added note related to Standby mode in *Table 39: Peripheral current consumption in Stop and Standby mode*. Updated *Figure 13: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 14: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive* and *Figure 15: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off*. Updated *Table 40: Low-power mode wakeup timings*. Updated MSI oscillator temperature frequency drift in *Table 48: MSI oscillator characteristics*. Updated *Table 53: EMS characteristics* and *Table 54: EMI characteristics*. Added t_{UP_LDO} in *Table 62: ADC characteristics*. Updated *Table 57: I/O current injection susceptibility*, *Table 58: I/O static characteristics* (I_{lkg}) and *Table 60: I/O AC characteristics*. *Section : Input/output AC characteristics*: updated introduction and *Table 71: I2C analog filter characteristics*. Updated *Figure 28: SPI timing diagram - slave mode and CPHA = 0*, *Table 73: SPI characteristics in voltage Range 1*, *Table 74: SPI characteristics in voltage Range 2* and *Table 75: SPI characteristics in voltage Range 3* and *Table 76: I2S characteristics*. Added *Section : Device marking for LQFP64* and *Section : Device marking for LQFP48*.