Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l063r8t6tr

**Table 4. Functionalities depending on the working mode
(from Run/active down to standby)** [1]

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(2)		--	
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
LCD	O	O	O	O	O		--	
USB	O	O	--	--	--	O	--	
USART	O	O	O	O	O[3]	O	--	
LPUART	O	O	O	O	O[3]	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	O	O	O[4]	O	--	
ADC	O	O	--	--	--		--	

3.8 Memories

The STM32L063x8 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32 or 64 Kbytes of embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1(PA4, PA5, PA6, PA7) or SPI2 (PB12, PB13, PB14, PB15), USART1(PA9, PA10) or USART2(PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: AES, SPI, I^2C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.11 Liquid crystal display (LCD)

The LCD drives up to 8 common terminals and 32 segment terminals to drive up to 224 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rails decoupling capability

3.12 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L063x8 device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference, V_{LCD} voltage measurement). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 μA at 10 kSPS, ~200 μA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock. It can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.20.4 Serial peripheral interface (SPI)/Inter-integrated sound (I2S)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

One standard I2S interfaces (multiplexed with SPI2) is available. It can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When the I2S interfaces is configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The SPIs can be served by the DMA controller.

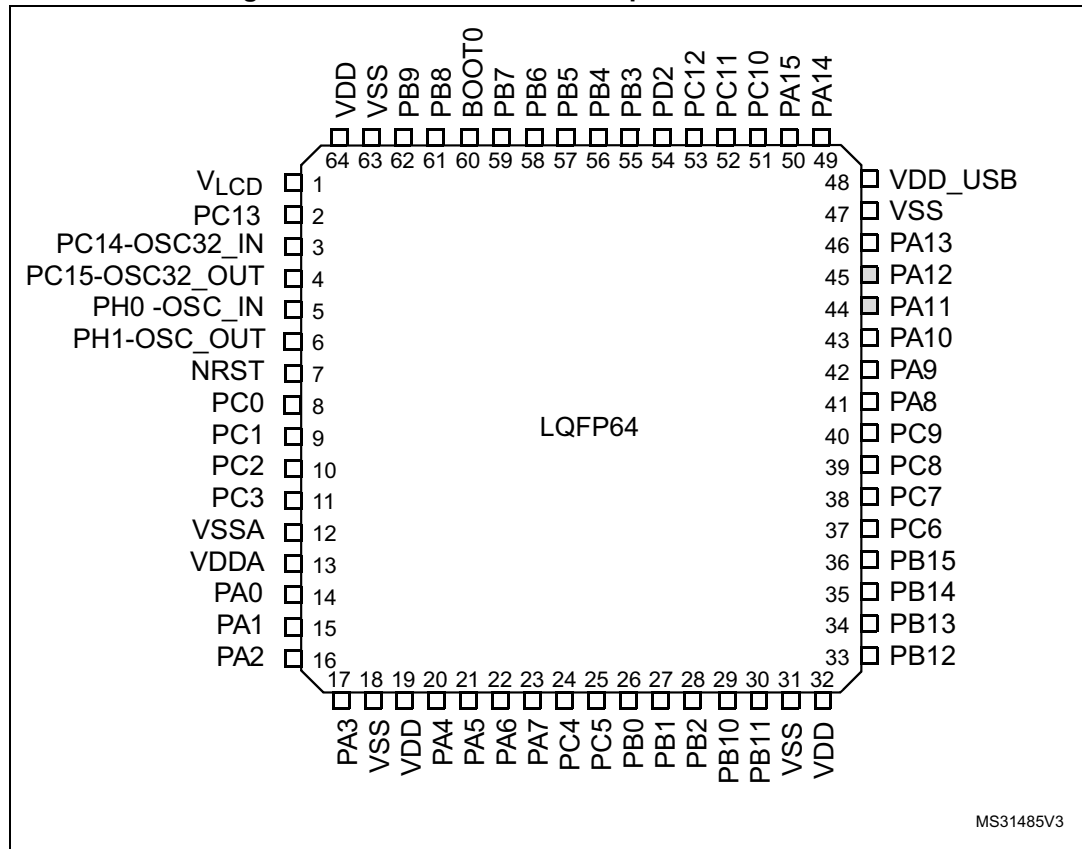Refer to *Table 13* for the differences between SPI1 and SPI2.

Table 13. SPI/I2S implementation

SPI features[1]	SPI1	SPI2
Hardware CRC calculation	X	X
I2S mode	-	X
TI mode	X	X

1. X = supported.

4 Pin descriptions

Figure 3. STM32L063x8 LQFP64 pinout - 10 x 10 mm

1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 15. STM32L063x8 pin definitions (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48	LQFP64						
18	26	PB0	I/O	FT	-	EVENTOUT, LCD_SEG5, TSC_G3_IO2	LCD_VLCD3, ADC_IN8, VREF_OUT
19	27	PB1	I/O	FT	-	LCD_SEG6, TSC_G3_IO3, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
20	28	PB2	I/O	FT	-	LPTIM1_OUT, TSC_G3_IO4	LCD_VLCD1
21	29	PB10	I/O	FT	-	LCD_SEG10, TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL	-
22	30	PB11	I/O	FT	-	EVENTOUT, LCD_SEG11, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA	-
23	31	VSS	S		-	-	-
24	32	VDD	S		-	-	-
25	33	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LCD_SEG12, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	LCD_VLCD2
26	34	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, LCD_SEG13, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
27	35	PB14	I/O	FTf	-	SPI2_MISO/I2S2_MCK, LCD_SEG14, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
28	36	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, LCD_SEG15, RTC_REFIN	-
-	37	PC6	I/O	FT	-	TIM22_CH1, LCD_SEG24, TSC_G8_IO1	-

Table 16. Alternate function port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/TIM21/SYS_AF/EVENTOUT/	LCD	USB/TIM2/EVENTOUT/	TSC/EVENTOUT	USART1/2/3	TIM2/21/22	EVENTOUT	COMP1/2
Port A	PA0	-	-	TIM2_CH1	TSC_G1_IO1	USART2_CTS	TIM2_ETR	-	COMP1_OUT
	PA1	EVENTOUT	LCD_SEG0	TIM2_CH2	TSC_G1_IO2	USART2_RTS_DE	TIM21_ETR	-	-
	PA2	TIM21_CH1	LCD_SEG1	TIM2_CH3	TSC_G1_IO3	USART2_TX	-	-	COMP2_OUT
	PA3	TIM21_CH2	LCD_SEG2	TIM2_CH4	TSC_G1_IO4	USART2_RX	-	-	-
	PA4	SPI1_NSS	-	-	TSC_G2_IO1	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	-	TIM2_ETR	TSC_G2_IO2	-	TIM2_CH1	-	-
	PA6	SPI1_MISO	LCD_SEG3		TSC_G2_IO3	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI	LCD_SEG4		TSC_G2_IO4	-	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO	LCD_COM0	USB_CRS_SYNC	EVENTOUT	USART1_CK	-	-	-
	PA9	MCO	LCD_COM1	-	TSC_G4_IO1	USART1_TX	-	-	-
	PA10	-	LCD_COM2	-	TSC_G4_IO2	USART1_RX	-	-	-
	PA11	SPI1_MISO	-	EVENTOUT	TSC_G4_IO3	USART1_CTS	-	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	TSC_G4_IO4	USART1_RTS_DE	-	-	COMP2_OUT
	PA13	SWDIO	-	USB_OE	-	-	-	-	-
	PA14	SWCLK	-	-	-	USART2_TX	-	-	-
	PA15	SPI1_NSS	LCD_SEG17	TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	-	-

Table 25. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.

2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 27* are based on characterization results, unless otherwise specified.

Table 26. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 27. Embedded internal reference voltage[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$[2]	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value[3]	Including uncertainties due to ADC and V_{DDA} values	-	-	±5	mV
T_{Coeff}[4]	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
A_{Coeff}[4]	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$[4]	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$[4][5]	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}[4]	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}[4]	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}[4]	VREF_OUT output current[6]	-	-	-	1	µA
C_{VREF_OUT}[4]	VREF_OUT output load	-	-	-	50	pF

Table 27. Embedded internal reference voltage[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LPBUF}[4]	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}[4]	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}[4]	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}[4]	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 39: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).

2. Guaranteed by test in production.

3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

4. Guaranteed by design.

5. Shortest sampling time can be determined in the application by multiple iterations.

6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 41: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 49*, *Table 24* and *Table 25* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Figure 11. I$_{DD}$ vs V$_{DD}$, at T$_A$= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS

MSv34792V1

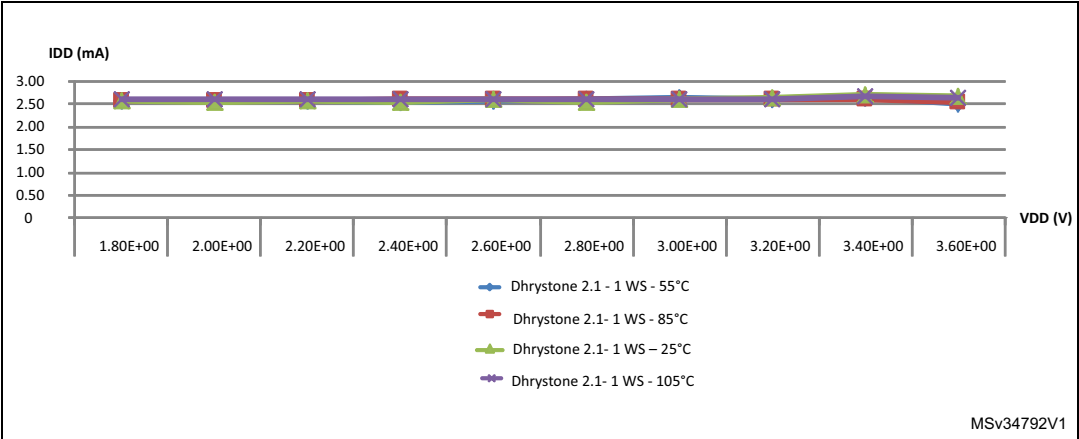**Figure 12. I$_{DD}$ vs V$_{DD}$, at T$_A$= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS**
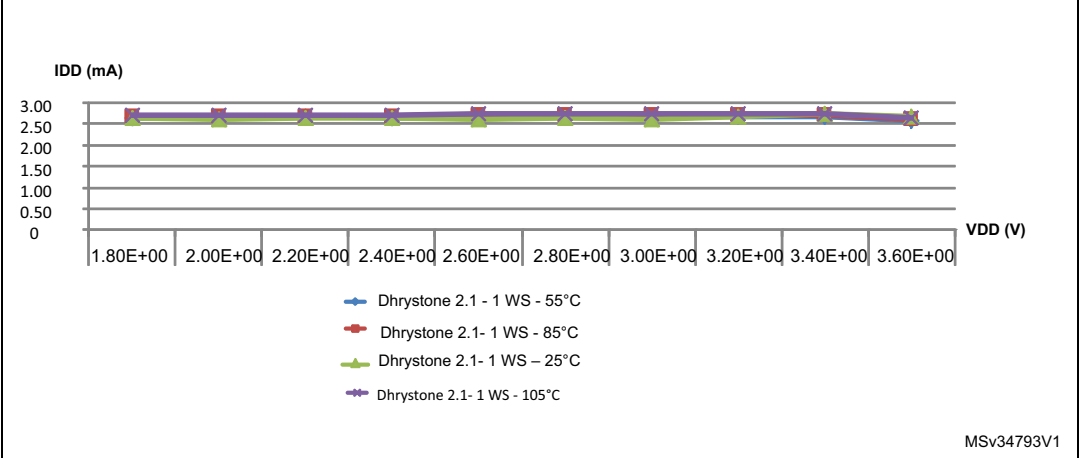

MSv34793V1

Figure 13. I_{DD} vs V_{DD}, at T_A= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

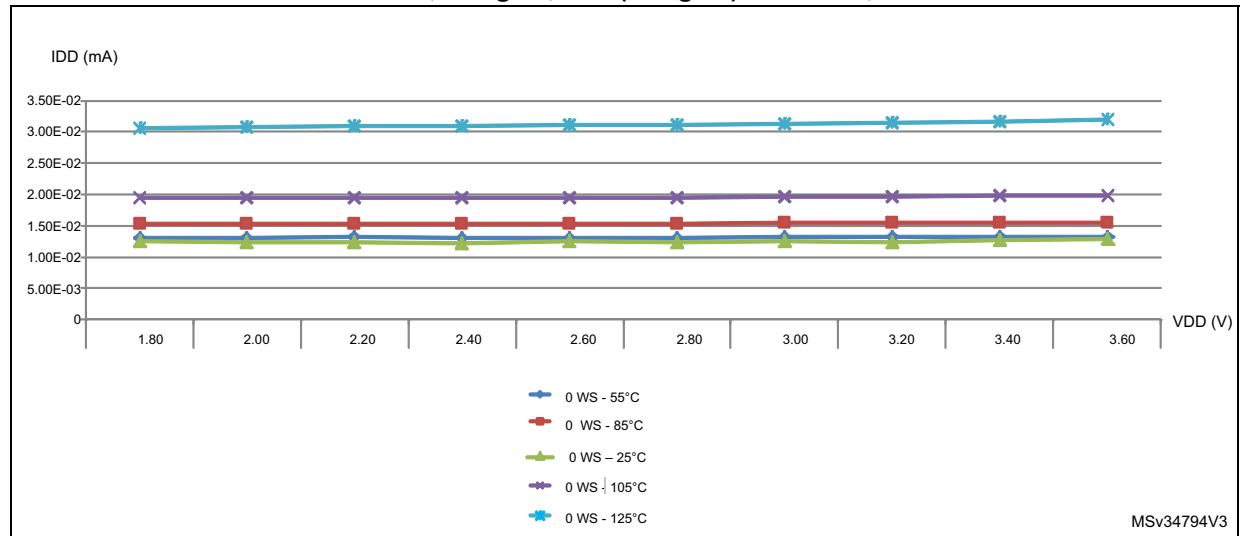**Table 34. Current consumption in Low-power sleep mode**

Symbol	Parameter	Conditions		Typ	Max[1]	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals off, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, f_{HCLK} = 32 kHz, Flash off	T_A = − 40 to 25°C	4.7[2]	-	μA
			MSI clock = 65 kHz, f_{HCLK} = 32 kHz, Flash on	T_A = − 40 to 25°C	17	23	
				T_A = 85 °C	19.5	63	
				T_A = 105 °C	23	69	
				T_A = 125 °C	32.5	90	
			MSI clock =65 kHz, f_{HCLK} = 65 kHz, Flash on	T_A = − 40 to 25°C	17	23	
				T_A = 85 °C	20	63	
				T_A = 105 °C	23.5	69	
				T_A = 125 °C	32.5	90	
			MSI clock = 131 kHz, f_{HCLK} = 131 kHz, Flash on	T_A = − 40 to 25°C	19.5	36	
				T_A = 55 °C	20.5	64	
				T_A = 85 °C	22.5	66	
				T_A = 105 °C	26	72	
				T_A = 125 °C	35	95	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. As the CPU is in Sleep mode, the difference between the current consumption with Flash on and off (nearly 12 μA) is the same whatever the clock frequency.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 54. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. f_{osc}/f_{CPU}			Unit
				8 MHz/ 4 MHz	8 MHz/ 16 MHz	8 MHz/ 32 MHz	
S_{EMI}	Peak level	$V_{DD} = 3.6$ V, $T_A = 25$ °C, compliant with IEC 61967-2	0.1 to 30 MHz	-21	-15	-12	dBµV
			30 to 130 MHz	-14	-12	-1	
			130 MHz to 1GHz	-10	-11	-7	
			EMI Level	1	1	1	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 56. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the conditions summarized in *Table 24*. All I/Os are CMOS and TTL compliant.

Table 58. I/O static characteristics

| Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC, FT, FTf, RST I/Os	-	-	$0.3V_{DD}$	V
		BOOT0 pin	-	-	$0.14V_{DD}$[1]	
V_{IH}	Input high level voltage	All I/Os	$0.7\ V_{DD}$	-	-	
V_{hys} [2]	I/O Schmitt trigger voltage hysteresis	Standard I/Os	-	10% V_{DD}[3]	-	
		BOOT0 pin	-	0.01	-	
I_{lkg}	Input leakage current [4]	$V_{SS} \leq V_{IN} \leq V_{DD}$ All I/Os except for PA11, PA12, BOOT0 and FTf I/Os	-	-	±50	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$, PA11 and PA12 I/Os	-	-	-50/+250	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ FTf I/Os	-	-	±100	
		$V_{DD} \leq V_{IN} \leq 5\ V$ All I/Os except for PA11, PA12, BOOT0 and FTf I/Os	-	-	200	nA
		$V_{DD} \leq V_{IN} \leq 5\ V$ FTf I/Os	-	-	500	
		$V_{DD} \leq V_{IN} \leq 5\ V$ PA11, PA12 and BOOT0	-	-	10	µA
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by characterization.

2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

3. With a minimum of 200 mV. Guaranteed by characterization results.

4. The max. value may be exceeded if negative current is injected on adjacent pins.

5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 21. V_{IH}/V_{IL} versus VDD (CMOS I/Os)
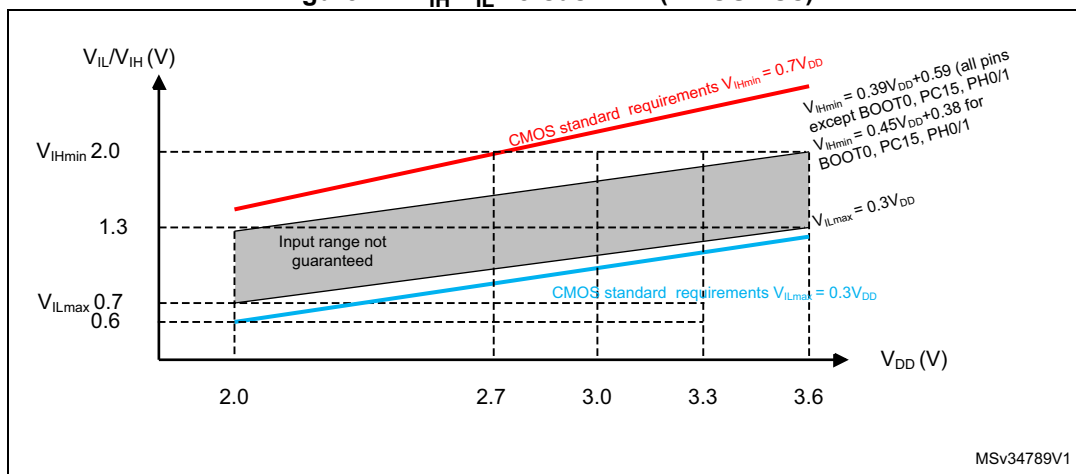
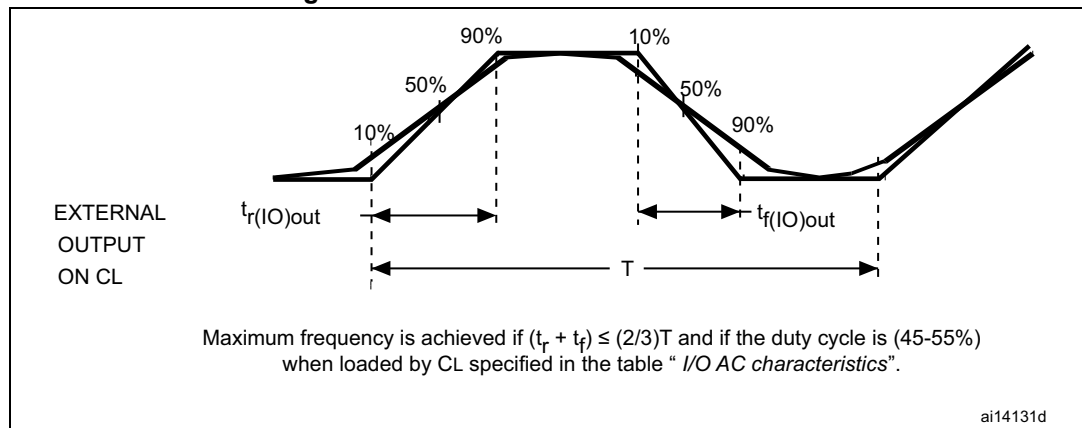**Figure 22. V_{IH}/V_{IL} versus VDD (TTL I/Os)**
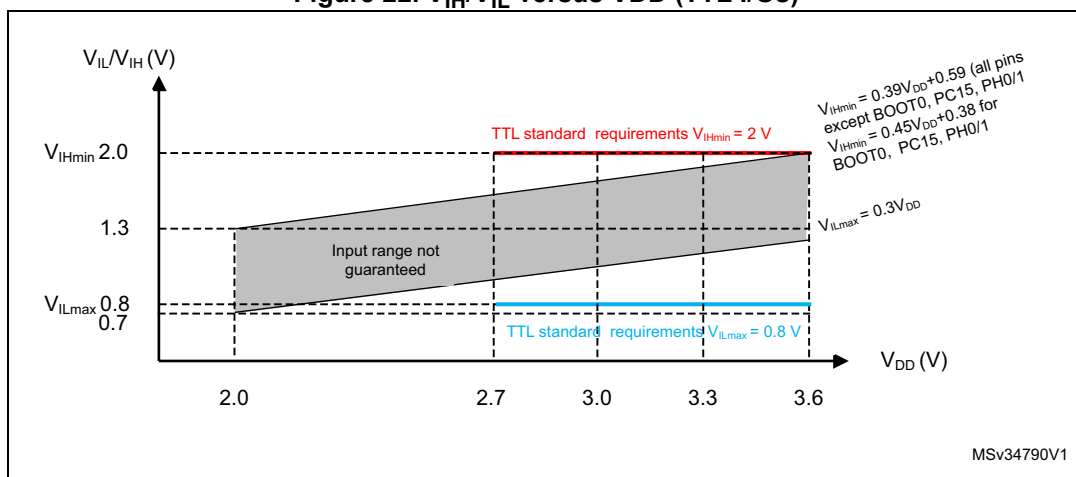
Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±15 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 59*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 22*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 22*).

Figure 23. I/O AC characteristics definition

EXTERNAL OUTPUT ON CL

$t_{r(IO)out}$

$t_{f(IO)out}$

T

Maximum frequency is achieved if $(t_r + t_f) \leq (2/3)T$ and if the duty cycle is (45-55%) when loaded by CL specified in the table "*I/O AC characteristics*".

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6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} , except when it is internally driven low (see *Table 61*).

Unless otherwise specified, the parameters given in *Table 61* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 61. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$[1]	NRST input low level voltage	-	V_{SS}	-	0.8	
$V_{IH(NRST)}$[1]	NRST input high level voltage	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$[1]	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	V
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$[1]	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}[2]	-	mV
R_{PU}	Weak pull-up equivalent resistor[3]	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$[1]	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$[1]	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.

2. 200 mV minimum value

3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 77. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$[1]	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 78. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.[1]	Max.[1]	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}[2]	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	
V_{CM}[2]	Differential common mode range	Includes V_{DI} range	0.8	2.5	V
V_{SE}[2]	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}[3]	Static output level low	R_L of 1.5 kΩ to 3.6 V[4]	-	0.3	V
V_{OH}[3]	Static output level high	R_L of 15 kΩ to V_{SS}[4]	2.8	3.6	

1. All the voltages are measured from the local ground potential.

2. Guaranteed by characterization results.

3. Guaranteed by test in production.

4. R_L is the load connected on the USB drivers.

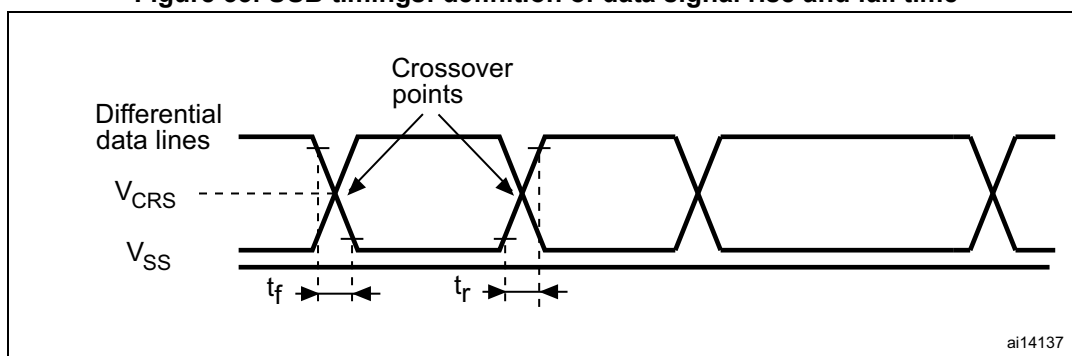**Figure 33. USB timings: definition of data signal rise and fall time**

Table 79. USB: full speed electrical characteristics

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time[2]	C_L = 50 pF	4	20	ns
t_f	Fall Time[2]	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.

2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
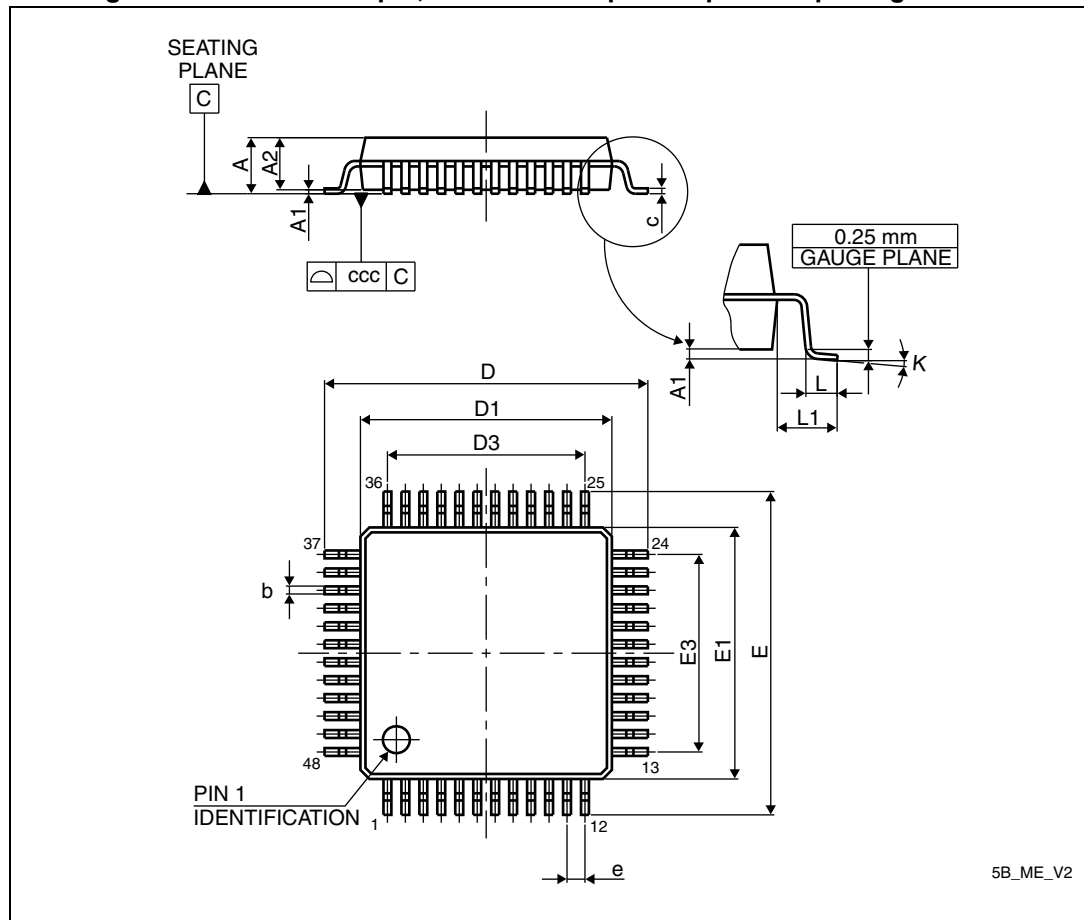
6.3.21 LCD controller

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 80. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	V
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF

7.2 LQFP48 package information

Figure 37. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline

1. Drawing is not to scale.

Table 85. Document revision history (continued)

Date	Revision	Changes
08-Sep-2015	5	Removed note 1 in *Table 1: Ultra-low-power STM32L063x8 device features and peripheral counts*. Updated all pinout/ballout schematics to highlight pin/ball supplied through VDD_USB. Updated current consumption in Run mode in *Section : Features*. Renamed BOOT1 into nBOOT1. Changed USARTx_RTS into USARTx_RTS_DE and LPUARTx_RTS into LPUARTx_RTS_DE. Updated VLCD in section Analog to digital converter (ADC). ADC no more available in Low-power run and Low-power Sleep modes in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)*. Updated *Figure 4: STM32L063x8 LQFP48 pinout - 7 x 7 mm* and *Figure 3: STM32L063x8 LQFP64 pinout - 10 x 10 mm*. Changed I/O structure for PC5 in *Table 15: STM32L063x8 pin definitions*. Updated VDD_USB in *Table 24: General operating conditions*. Changed temperature condition in *Table 7: Internal voltage reference measured values* and *Table 26: Embedded internal reference voltage calibration values*. Updated T_{Coeff} in *Table 27: Embedded internal reference voltage*. Added note related to Standby mode in *Table 39: Peripheral current consumption in Stop and Standby mode*. Updated *Figure 13: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS, Figure 14: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive* and *Figure 15: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off*. Updated *Table 40: Low-power mode wakeup timings*. Updated MSI oscillator temperature frequency drift in *Table 48: MSI oscillator characteristics*. Updated *Table 53: EMS characteristics* and *Table 54: EMI characteristics*. Added t_{UP_LDO} in *Table 62: ADC characteristics*. Updated *Table 57: I/O current injection susceptibility, Table 58: I/O static characteristics* (I_{lkg}) and *Table 60: I/O AC characteristics*. *Section : Input/output AC characteristics*: updated introduction and *Table 71: I2C analog filter characteristics*. Updated *Figure 28: SPI timing diagram - slave mode and CPHA = 0, Table 73: SPI characteristics in voltage Range 1, Table 74: SPI characteristics in voltage Range 2* and *Table 75: SPI characteristics in voltage Range 3* and *Table 76: I2S characteristics*. Added *Section : Device marking for LQFP64* and *Section : Device marking for LQFP48*.