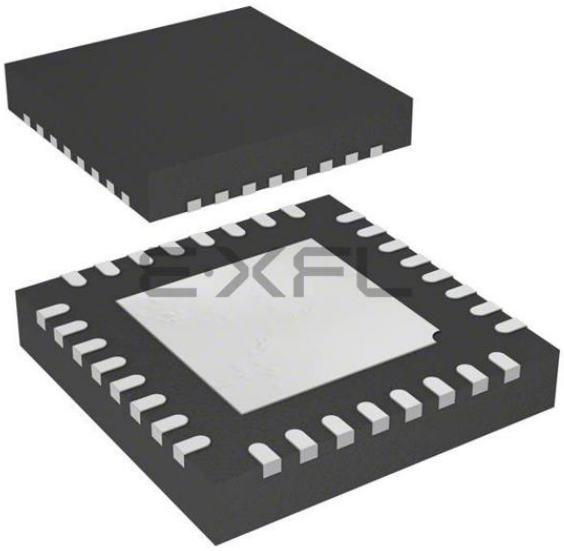

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, QSPI, SAI, SPI, SWPMI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l432kbu6

Table 3. Functionalities depending on the working mode[1]

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown	
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-
Flash memory (up to 256 KB)	O[2]	O[2]	O[2]	O[2]	-	-	-	-	-	-	-	-
SRAM1 (48 KB)	Y	Y[3]	Y	Y[3]	Y	-	Y	-	-	-	-	-
SRAM2 (16 KB)	Y	Y[3]	Y	Y[3]	Y	-	Y	-	O[4]	-	-	-
Quad SPI	O	O	O	O	-	-	-	-	-	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-
Peripheral Voltage Monitor (PVMx; x=1,3,4)	O	O	O	O	O	O	O	O	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-
High Speed Internal (HSI16)	O	O	O	O	(5)	-	(5)	-	-	-	-	-
Oscillator RC48	O	O	-	-	-	-	-	-	-	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-	O	-	O	-
Multi-Speed Internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-
Clock Security System (CSS)	O	O	O	O	-	-	-	-	-	-	-	-
Clock Security System on LSE	O	O	O	O	O	O	O	O	O	O	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	1	1	1	1	1	O	1	O	1	O	1	O
USB FS	O[8]	O[8]	-	-	-	O	-	-	-	-	-	-

Table 3. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown	
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability
USARTx (x=1,2)	O	O	O	O	O[6]	O[6]	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O[6]	O[6]	O[6]	O[6]	-	-	-	-
I2Cx (x=1)	O	O	O	O	O[7]	O[7]	-	-	-	-	-	-
I2C3	O	O	O	O	O[7]	O[7]	O[7]	O[7]	-	-	-	-
SPIx (x=1,3)	O	O	O	O	-	-	-	-	-	-	-	-
CAN	O	O	O	O	-	-	-	-	-	-	-	-
SWPMI1	O	O	O	O	-	O	-	-	-	-	-	-
SAIx (x=1)	O	O	O	O	-	-	-	-	-	-	-	-
ADCx (x=1)	O	O	O	O	-	-	-	-	-	-	-	-
DACx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-
OPAMPx (x=1)	O	O	O	O	O	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-
Random number generator (RNG)	O[8]	O[8]	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	[9]	2 pins [10]	[11]	2 pins [10]

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.21.5 Infrared interface (IRTIM)

The STM32L432xx includes one infrared interface (IRTIM). It can be used with an infrared LED to perform remote control functions. It uses TIM15 and TIM16 output channels to generate output signal waveforms on IR_OUT pin.

3.21.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.21.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.21.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.23 Inter-integrated circuit interface (I2C)

The device embeds 2 I2C. Refer to *Table 9: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol ($PMBus^{TM}$) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 3: Clock tree*.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 9. I2C implementation

I2C features(1)	I2C1	I2C3
Standard-mode (up to 100 kbit/s)	X	X
Fast-mode (up to 400 kbit/s)	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X
Independent clock	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X
Wakeup from Stop 2 mode on address match	-	X

1. X: supported

3.24 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L432xx devices have two embedded universal synchronous receiver transmitters (USART1 and USART2).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1 and USART2 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 10. STM32L432xx USART/LPUART features

USART modes/features(1)	USART1	USART2	LPUART1
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	-
Smartcard mode	X	X	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual clock domain	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X
Wakeup from Stop 2 mode	-	-	X
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto baud rate detection	X (4 modes)		-
Driver Enable	X	X	X
LPUART/USART data length	7, 8 and 9 bits		

1. X = supported.

3.32 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

Both throughput and capacity can be increased two-fold using dual-flash mode, where two quad SPI flash memories are accessed simultaneously.

The Quad SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

Table 13. STM32L432xx pin definitions (continued)

Pin Number	Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32					Alternate functions	Additional functions
13	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, COMP2_OUT, EVENTOUT	ADC1_IN12
14	PB0	I/O	FT_a	-	TIM1_CH2N, SPI1_NSS, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	ADC1_IN15
15	PB1	I/O	FT_a	-	TIM1_CH3N, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
16	VSS	S	-	-	-	-
17	VDD	S	-	-	-	-
18	PA8	I/O	FT	-	MCO, TIM1_CH1, USART1_CK, SWPMI1_IO, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
19	PA9	I/O	FT_f	-	TIM1_CH2, I2C1_SCL, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
20	PA10	I/O	FT_f	-	TIM1_CH3, I2C1_SDA, USART1_RX, USB_CRS_SYNC, SAI1_SD_A, EVENTOUT	-
21	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, COMP1_OUT, USART1_CTS, CAN1_RX, USB_DM, TIM1_BKIN2_COMP1, EVENTOUT	-
22	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, USB_DP, EVENTOUT	-
23	PA13 (JTMS-SWDIO)	I/O	FT	(3)	JTMS-SWDIO, IR_OUT, USB_NOE, SWPMI1_TX, SAI1_SD_B, EVENTOUT	-

Table 16. STM32L432xx memory map and peripheral register boundary addresses

Bus	Boundary address	Size(bytes)	Peripheral
APB1	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0400- 0x4000 0FFF	3 KB	Reserved
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

Table 24. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.37	2.38	2.44	2.52	2.66	2.7	2.7	2.8	2.9	3.2	mA
				16 MHz	1.5	1.52	1.57	1.64	1.79	1.7	1.7	1.8	2.0	2.3	
				8 MHz	0.81	0.82	0.87	0.94	1.08	0.9	0.9	1.0	1.2	1.5	
				4 MHz	0.46	0.47	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				2 MHz	0.29	0.3	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				1 MHz	0.2	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				100 kHz	0.12	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	8.53	8.56	8.64	8.74	8.92	9.5	9.6	9.7	9.9	10.3	
				72 MHz	7.7	7.73	7.8	7.9	8.08	8.6	8.6	8.7	8.9	9.3	
				64 MHz	6.86	6.9	6.97	7.06	7.23	7.7	7.7	7.8	8.0	8.3	
				48 MHz	5.13	5.16	5.23	5.32	5.49	5.8	5.8	6.0	6.1	6.5	
				32 MHz	3.46	3.48	3.55	3.64	3.8	3.9	4.0	4.1	4.2	4.6	
				24 MHz	2.63	2.64	2.71	2.79	2.96	3.0	3.0	3.1	3.3	3.6	
				16 MHz	1.8	1.81	1.87	1.96	2.12	2.0	2.1	2.2	2.3	2.7	
I_{DD}(LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	211	230	280	355	506	273.8	301.1	360.4	502.7	815.9	µA
				1 MHz	117	134	179	254	404	154.7	184.6	249.6	398.4	712.4	
				400 kHz	58.5	70.4	116	189	338	80.2	111.5	179.7	330.8	643.4	
				100 kHz	30	41.1	85.2	159	308	46.5	76.6	147.1	299.1	611.2	

1. Guaranteed by characterization results, unless otherwise specified.

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.42	2.43	2.49	2.56	2.71	2.7	2.7	2.8	3.0	3.3	mA
				16 MHz	1.54	1.55	1.6	1.67	1.82	1.7	1.7	1.8	2.0	2.3	
				8 MHz	0.82	0.84	0.88	0.95	1.1	0.9	1.0	1.0	1.2	1.5	
				4 MHz	0.47	0.48	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				2 MHz	0.29	0.3	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				1 MHz	0.2	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				100 kHz	0.12	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	8.63	8.68	8.74	8.84	9.01	9.5	9.6	9.7	9.9	10.2	
				72 MHz	7.79	7.83	7.9	7.99	8.17	8.6	8.6	8.8	8.9	9.3	
				64 MHz	6.95	6.99	7.05	7.15	7.32	7.7	7.7	7.9	8.0	8.4	
				48 MHz	5.19	5.22	5.29	5.38	5.55	5.8	5.8	5.9	6.1	6.5	
				32 MHz	3.51	3.53	3.6	3.68	3.85	3.9	4.0	4.1	4.2	4.6	
				24 MHz	2.66	2.68	2.74	2.83	2.99	3.0	3.0	3.1	3.3	3.6	
				16 MHz	1.82	1.84	1.89	1.98	2.14	2.0	2.1	2.2	2.3	2.7	
I_{DD}(LPRun)	Supply current in low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable FLASH in power-down		2 MHz	205	228	275	352	501	276.5	302.3	358.4	502.5	816.4	µA
				1 MHz	111	126	175	248	397	151.3	180.9	245.3	390.7	703.4	
				400 kHz	49.2	62.7	108	181	330	73.3	104.0	170.8	321.0	632.4	
				100 kHz	21.5	33.3	76.6	151	299	36.4	67.7	137.2	287.8	600.8	

1. Guaranteed by characterization results, unless otherwise specified.

Table 27. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.37	mA	91	µA/MHz
				Coremark	2.69		103	
				Dhrystone 2.1	2.74		105	
				Fibonacci	2.58		99	
				While(1)	2.30		88	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	8.53	mA	107	µA/MHz
				Coremark	9.68		121	
				Dhrystone 2.1	9.76		122	
				Fibonacci	9.27		116	
				While(1)	8.20		103	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	211	µA	106	µA/MHz
				Coremark	251		126	
				Dhrystone 2.1	269		135	
				Fibonacci	230		115	
				While(1)	286		143	

1. Reduced code used for characterization results provided in *Table 24*, *Table 25*, *Table 26*.

Table 30. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.68	0.69	0.74	0.81	0.95	0.8	0.8	0.9	1.0	1.3	mA
				16 MHz	0.46	0.48	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				8 MHz	0.29	0.30	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				4 MHz	0.20	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				2 MHz	0.16	0.17	0.21	0.28	0.42	0.2	0.2	0.3	0.4	0.7	
				1 MHz	0.13	0.15	0.19	0.26	0.40	0.1	0.2	0.3	0.4	0.7	
				100 kHz	0.11	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	2.23	2.25	2.30	2.38	2.54	2.5	2.5	2.6	2.8	3.1	
				72 MHz	2.02	2.04	2.10	2.18	2.34	2.2	2.3	2.4	2.5	2.9	
				64 MHz	1.82	1.84	1.89	1.98	2.14	2.0	2.1	2.1	2.3	2.6	
				48 MHz	1.34	1.36	1.42	1.50	1.66	1.5	1.6	1.7	1.8	2.2	
				32 MHz	0.93	0.95	1.01	1.09	1.25	1.1	1.1	1.2	1.4	1.7	
				24 MHz	0.73	0.75	0.80	0.88	1.04	0.8	0.9	1.0	1.1	1.4	
				16 MHz	0.53	0.55	0.60	0.68	0.84	0.6	0.6	0.7	0.9	1.2	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	71.8	80.7	125	200	350	91.1	122.7	191.3	341.5	653.5	µA
				1 MHz	45.0	57.3	101	176	325	63.2	95.4	165.4	316.5	628.7	
				400 kHz	27.0	40.7	84.6	158	308	43.9	75.8	147.2	297.6	609.2	
				100 kHz	22.8	30.9	63.3	113.2	207.7	35.2	67.9	140.9	290.8	602.4	

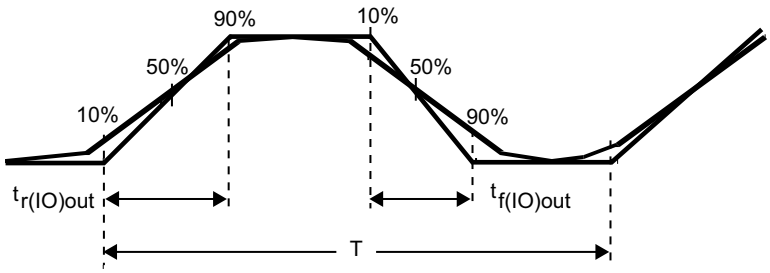
1. Guaranteed by characterization results, unless otherwise specified.

Table 36. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	63	133	522	1 490	4 270	-	-	-	-	-	nA
			2.4 V	165	253	710	1 830	4 980	-	-	-	-	-	
			3 V	316	423	990	2 340	6 050	-	-	-	-	-	
			3.6 V	649	787	1 530	3 220	7 710	-	-	-	-	-	
		RTC clocked by LSE quartz (2) in low drive mode	1.8 V	203	293	700	1 675	-	-	-	-	-	-	
			2.4 V	303	411	880	2 001	-	-	-	-	-	-	
			3 V	448	567	1 136	2 479	-	-	-	-	-	-	
			3.6 V	744	887	1 609	3 256	-	-	-	-	-	-	
I_{DD}(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz. See (3).	3 V	0.780	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 38: Low-power mode wakeup timings*.

Figure 18. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 58: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 59. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7 \times V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Table 61. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

Table 65. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 65. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 66. ADC accuracy - limited test conditions 4(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

SAI characteristics

Unless otherwise specified, the parameters given in *Table 79* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 20: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 79. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter $2.7 \le V_{DD} \le 3.6$ Voltage Range 1	-	18.5	MHz
		Master transmitter $1.71 \le V_{DD} \le 3.6$ Voltage Range 1	-	12.5	
		Master receiver Voltage Range 1	-	25	
		Slave transmitter $2.7 \le V_{DD} \le 3.6$ Voltage Range 1	-	22.5	
		Slave transmitter $1.71 \le V_{DD} \le 3.6$ Voltage Range 1	-	14.5	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	12.5	
$t_{v(FS)}$	FS valid time	Master mode $2.7 \le V_{DD} \le 3.6$	-	22	ns
		Master mode $1.71 \le V_{DD} \le 3.6$	-	40	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2	-	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	2	-	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	2.5	-	