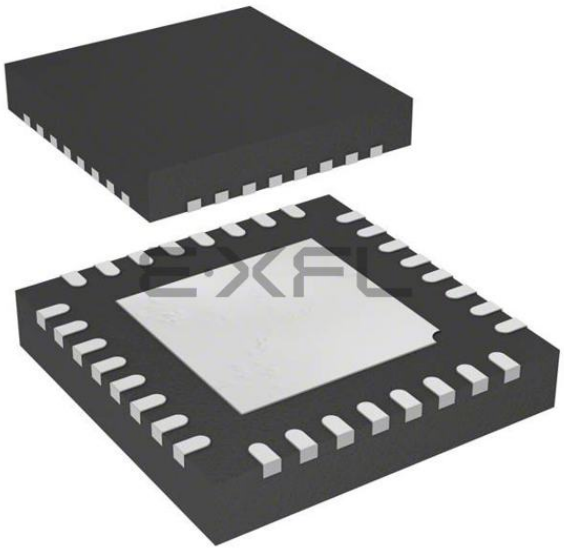

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

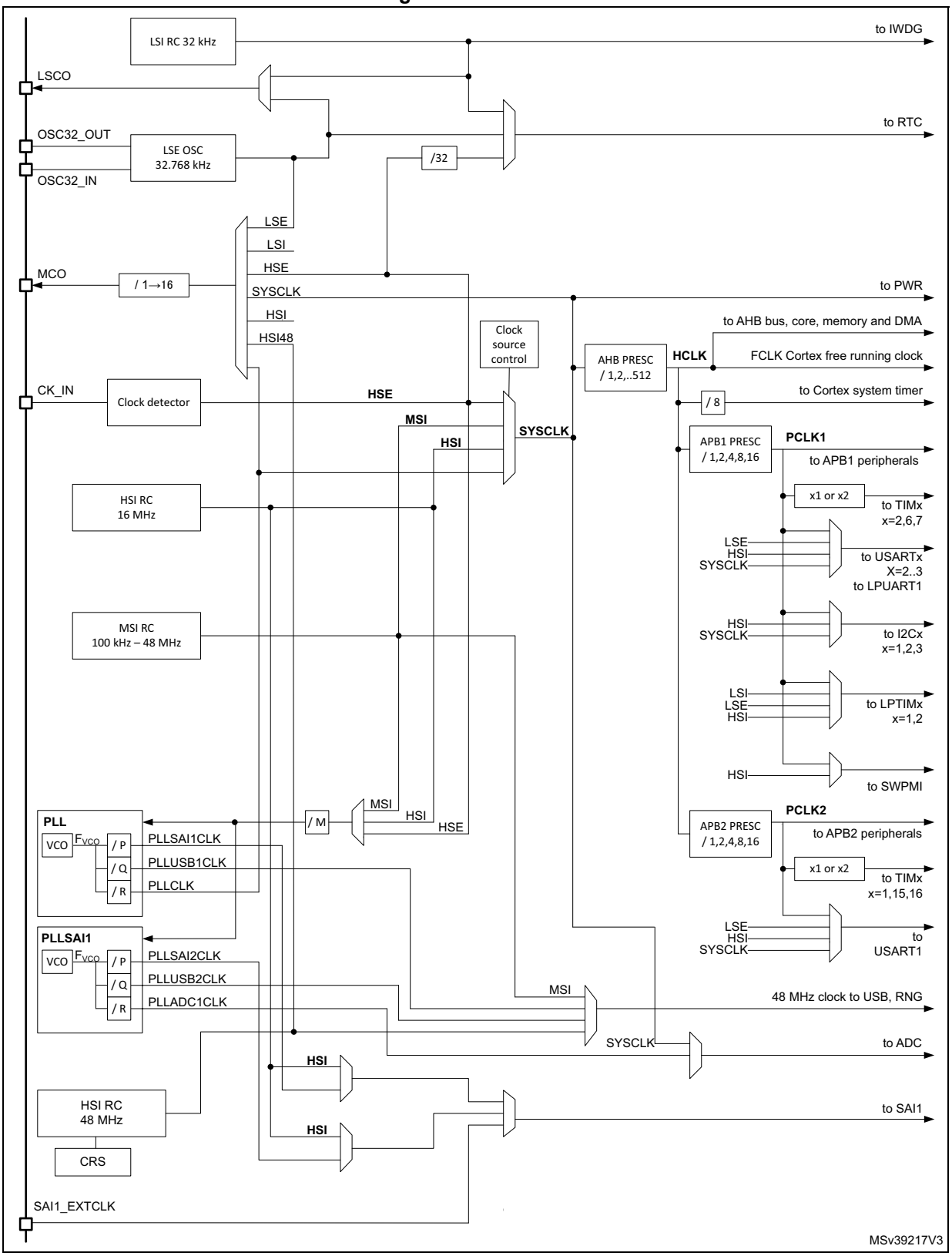
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, QSPI, SAI, SPI, SWPMI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-UFQFPN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l432kbu6tr |

## 3.11 Clocks and startup

The clock controller (see *Figure 3*) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - High Speed External clock (HSE) can supply a PLL.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device. The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- **RC48 with clock recovery system (HSI48)**: internal RC48 MHz clock source can be used to drive the USB or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** Several peripherals (USB, RNG, SAI, USARTs, I2Cs, LPTimers, ADC, SWPMI) have their own independent clock whatever the system clock. Two PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/RNG and the SAI.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.
- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes.

**Figure 3. Clock tree**



This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

### 3.21.5 Infrared interface (IRTIM)

The STM32L432xx includes one infrared interface (IRTIM). It can be used with an infrared LED to perform remote control functions. It uses TIM15 and TIM16 output channels to generate output signal waveforms on IR_OUT pin.

### 3.21.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.21.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

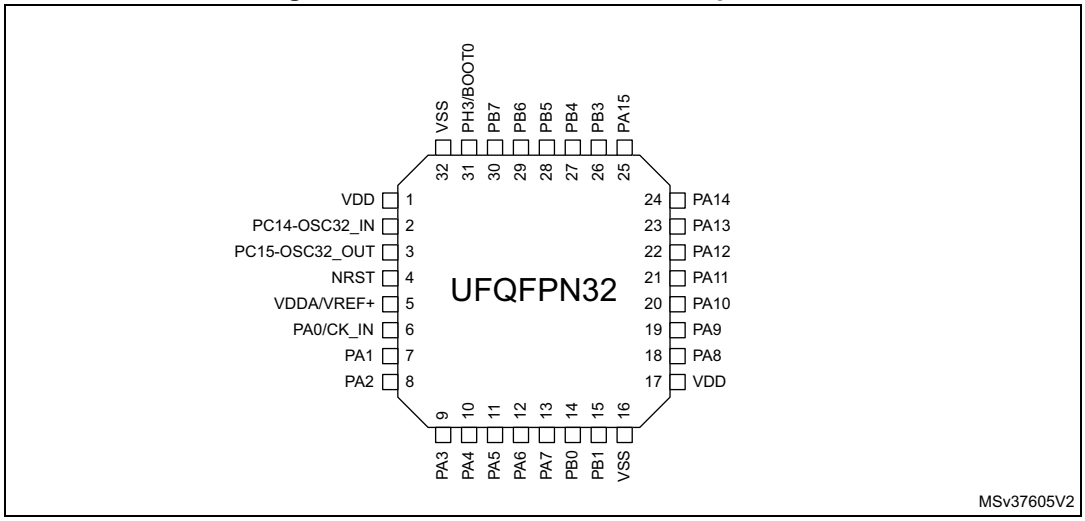
### 3.21.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

# 4 Pinouts and pin description

**Figure 4. STM32L432Kx UFQFPN32 pinout(1)**




1. The above figure shows the package top view.

**Table 12. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V tolerant I/O |
| | | TT | 3.6 V tolerant I/O |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| | | **Option for TT or FT I/Os** | |
| | | _f (1) | I/O, Fm+ capable |
| | | _u (2) | I/O, with USB function supplied by $V_{DDUSB}$ |
| | | _a (3) | I/O, with Analog switch function supplied by $V_{DDA}$ |
| Notes | | Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

1. The related I/O structures in *Table 13* are: FT_f, FT_fa.
2. The related I/O structures in *Table 13* is: FT_u.
3. The related I/O structures in *Table 13* are: FT_a, FT_fa, TT_a.

Table 13. STM32L432xx pin definitions (continued)

| Pin Number | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|
| UFQFPN32 | | | | | Alternate functions | Additional functions |
| 24 | PA14 (JTCK-SWCLK) | I/O | FT | (3) | JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, SWPMI1_RX, SAI1_FS_B, EVENTOUT | - |
| 25 | PA15 (JTDI) | I/O | FT | (3) | JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, TSC_G3_IO1, SWPMI1_SUSPEND, EVENTOUT | - |
| 26 | PB3 (JTDO-TRACE SWO) | I/O | FT_a | (3) | JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, SAI1_SCK_B, EVENTOUT | COMP2_INM |
| 27 | PB4 (NJTRST) | I/O | FT_fa | (3) | NJTRST, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS, TSC_G2_IO1, SAI1_MCLK_B, EVENTOUT | COMP2_INP |
| 28 | PB5 | I/O | FT | - | LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT | - |
| 29 | PB6 | I/O | FT_fa | - | LPTIM1_ETR, I2C1_SCL, USART1_TX, TSC_G2_IO3, SAI1_FS_B, TIM16_CH1N, EVENTOUT | COMP2_INP |
| 30 | PB7 | I/O | FT_fa | - | LPTIM1_IN2, I2C1_SDA, USART1_RX, TSC_G2_IO4, EVENTOUT | COMP2_INM, PVD_IN |
| 31 | PH3/ BOOT0 | I/O | FT | - | EVENTOUT | BOOT0 |
| 32 | VSS | S | - | - | - | - |
| 1 | VDD | S | - | - | - | - |

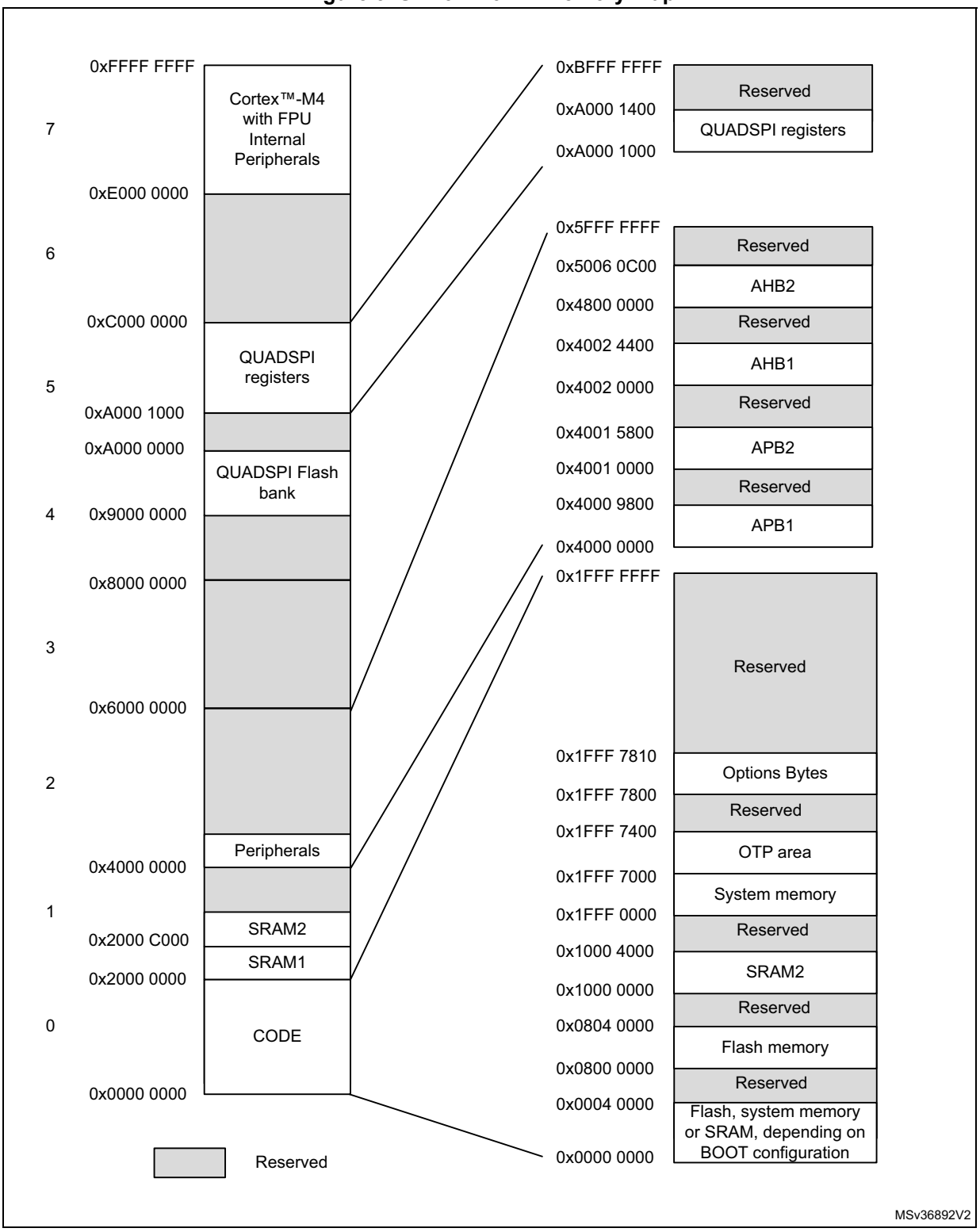
1. PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC14 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0393 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

**Table 15. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 14*)**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | LPUART1 | CAN1/TSC | USB/QUADSPI | - | COMP1/ COMP2/ SWPMI1 | SAI1 | TIM2/TIM15/ TIM16/LPTIM2 | EVENTOUT |
| Port A | PA0 | - | - | - | - | COMP1_OUT | SAI1_EXTCLK | TIM2_ETR | EVENTOUT |
| | PA1 | - | - | - | - | - | - | TIM15_CH1N | EVENTOUT |
| | PA2 | LPUART1_TX | - | QUADSPI_ BK1_NCS | - | COMP2_OUT | - | TIM15_CH1 | EVENTOUT |
| | PA3 | LPUART1_RX | - | QUADSPI_CLK | - | - | SAI1_MCLK_A | TIM15_CH2 | EVENTOUT |
| | PA4 | - | - | - | - | - | SAI1_FS_B | LPTIM2_OUT | EVENTOUT |
| | PA5 | - | - | - | - | - | - | LPTIM2_ETR | EVENTOUT |
| | PA6 | LPUART1_CTS | - | QUADSPI_ BK1_IO3 | - | TIM1_BKIN_ COMP2 | - | TIM16_CH1 | EVENTOUT |
| | PA7 | - | - | QUADSPI_ BK1_IO2 | - | COMP2_OUT | - | - | EVENTOUT |
| | PA8 | - | - | - | - | SWPMI1_IO | SAI1_SCK_A | LPTIM2_OUT | EVENTOUT |
| | PA9 | - | - | - | - | - | SAI1_FS_A | TIM15_BKIN | EVENTOUT |
| | PA10 | - | - | USB_CRS_ SYNC | - | - | SAI1_SD_A | - | EVENTOUT |
| | PA11 | - | CAN1_RX | USB_DM | - | TIM1_BKIN2_ COMP1 | - | - | EVENTOUT |
| | PA12 | - | CAN1_TX | USB_DP | - | - | - | - | EVENTOUT |
| | PA13 | - | - | USB_NOE | - | SWPMI1_TX | SAI1_SD_B | - | EVENTOUT |
| | PA14 | - | - | - | - | SWPMI1_RX | SAI1_FS_B | - | EVENTOUT |
| | PA15 | - | TSC_G3_IO1 | - | - | SWPMI1_ SUSPEND | - | - | EVENTOUT |

# 5 Memory mapping

**Figure 5. STM32L432xx memory map**



# 6.3 Operating conditions

## 6.3.1 General operating conditions

**Table 20. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 80 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 80 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 80 | |
| $V_{DD}$ | Standard operating voltage | - | 1.71 (1) | 3.6 | V |
| $V_{DDA}$ | Analog supply voltage | ADC or COMP used | 1.62 | 3.6 | V |
| | | DAC or OPAMP used | 1.8 | | |
| | | ADC, DAC, OPAMP, COMP not used | 0 | | |
| $V_{DDUSB}$ | USB supply voltage | USB used | 3.0 | 3.6 | V |
| | | USB not used | 0 | 3.6 | |
| $V_{IN}$ | I/O input voltage | TT_xx I/O | -0.3 | $V_{DDIOx}$+0.3 | V |
| | | All I/O except TT_xx | -0.3 | MIN(MIN($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$)+3.6 V, 5.5 V)(2)(3) | |
| $P_D$ | Power dissipation at $T_A$ = 125 °C for suffix 3(4) | UFQFPN32 | - | 128 | mW |
| $P_D$ | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7(4) | UFQFPN32 | - | 523 | mW |
| $T_A$ | Ambient temperature for the suffix 6 version | Maximum power dissipation | –40 | 85 | °C |
| | | Low-power dissipation(5) | –40 | 105 | |
| | Ambient temperature for the suffix 7 version | Maximum power dissipation | –40 | 105 | |
| | | Low-power dissipation(5) | –40 | 125 | |
| | Ambient temperature for the suffix 3 version | Maximum power dissipation | –40 | 125 | |
| | | Low-power dissipation(5) | –40 | 130 | |
| $T_J$ | Junction temperature range | Suffix 6 version | –40 | 105 | °C |
| | | Suffix 7 version | –40 | 125 | |
| | | Suffix 3 version | –40 | 130 | |

1. When RESET is released functionality is guaranteed down to $V_{BOR0}$ Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$)+3.6 V and 5.5V.
3. For operation with voltage higher than Min ($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$ (see *Section 7.2: Thermal characteristics*).

### 6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 9: Current consumption measurement scheme*.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the $f_{HCLK}$ frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0393 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 24* to *Table 36* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

**Table 31. Current consumption in Low-power sleep modes, Flash in power-down**

| Symbol | Parameter | Conditions | | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | Voltage scaling | $f_{HCLK}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$(LPSleep) | Supply current in low-power sleep mode | $f_{HCLK} = f_{MSI}$ all peripherals disable | | 2 MHz | 58.7 | 70.7 | 103.2 | 153.7 | 248.5 | 80 | 113 | 180 | 330 | 641 | µA |
| | | | | 1 MHz | 39.4 | 47.2 | 79.3 | 129.6 | 224.8 | 53 | 86 | 154 | 304 | 616 | |
| | | | | 400 kHz | 20.8 | 30.8 | 62.1 | 112.5 | 207.8 | 35 | 67 | 137 | 286 | 597 | |
| | | | | 100 kHz | 14.3 | 23.1 | 55.1 | 105.7 | 201.5 | 27 | 58 | 130 | 279 | 590 | |

1. Guaranteed by characterization results, unless otherwise specified.

**Table 32. Current consumption in Stop 2 mode**

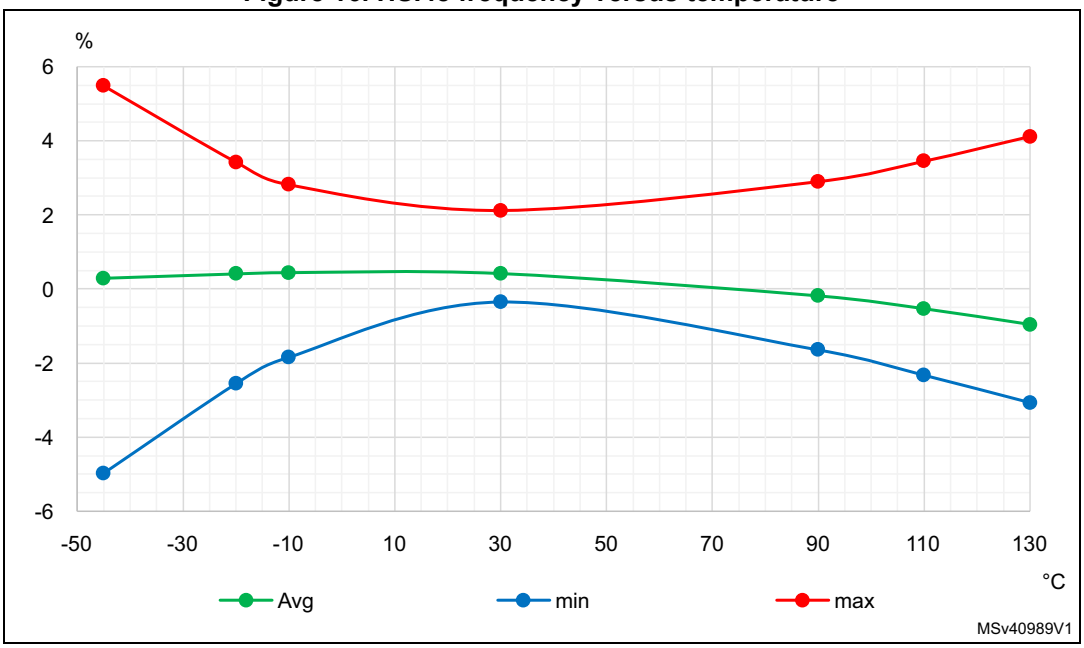
| Symbol | Parameter | Conditions | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | $V_{DD}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$ (Stop 2) | Supply current in Stop 2 mode, RTC disabled | - | 1.8 V | 1 | 2.54 | 8.74 | 19.8 | 43.4 | 2.0 | 5.6 | 21.1 | 50.8 | 116.0 | µA |
| | | | 2.4 V | 1.02 | 2.59 | 8.89 | 20.2 | 44.3 | 2.1 | 5.8 | 21.6 | 52.3 | 119.6 | |
| | | | 3 V | 1.06 | 2.67 | 9.11 | 20.7 | 45.5 | 2.1 | 5.9 | 22.2 | 53.7 | 123.2 | |
| | | | 3.6 V | 1.23 | 2.88 | 9.56 | 21.6 | 47.3 | 2.3 | 6.1 | 23.0 | 55.8 | 127.9 | |
| $I_{DD}$ (Stop 2 with RTC) | Supply current in Stop 2 mode, RTC enabled | RTC clocked by LSI | 1.8 V | 1.3 | 2.82 | 9.02 | 20.1 | 43.6 | 2.5 | 6.2 | 21.6 | 51.3 | 116.3 | µA |
| | | | 2.4 V | 1.39 | 2.95 | 9.24 | 20.5 | 44.6 | 2.8 | 6.4 | 22.3 | 52.8 | 120.0 | |
| | | | 3 V | 1.5 | 3.11 | 9.55 | 21.1 | 45.8 | 3.0 | 6.8 | 23.0 | 54.5 | 123.8 | |
| | | | 3.6 V | 1.76 | 3.42 | 10.1 | 22.1 | 47.8 | 3.3 | 7.2 | 24.1 | 56.7 | 128.7 | |
| | | RTC clocked by LSE bypassed at 32768 Hz | 1.8 V | 1.36 | 2.9 | 9.1 | 20.1 | 43.7 | - | - | - | - | - | |
| | | | 2.4 V | 1.48 | 3.09 | 9.44 | 20.8 | 45 | - | - | - | - | - | |
| | | | 3 V | 1.83 | 3.67 | 10.4 | 22.3 | 47.3 | - | - | - | - | - | |
| | | | 3.6 V | 3.58 | 6.17 | 13.9 | 26.6 | 53 | - | - | - | - | - | |
| | | RTC clocked by LSE quartz(2) in low drive mode | 1.8 V | 1.28 | 2.81 | 9.13 | 20.8 | - | - | - | - | - | - | |
| | | | 2.4 V | 1.39 | 2.93 | 9.34 | 21.3 | - | - | - | - | - | - | |
| | | | 3 V | 1.59 | 3.1 | 9.64 | 21.8 | - | - | - | - | - | - | |
| | | | 3.6 V | 1.86 | 3.45 | 10.2 | 22.8 | - | - | - | - | - | - | |

**Table 46. HSI48 oscillator characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $N_T$ jitter | Next transition jitter<br>Accumulated jitter on 28 cycles(4) | - | - | +/-0.15(2) | - | ns |
| $P_T$ jitter | Paired transition jitter<br>Accumulated jitter on 56 cycles(4) | - | - | +/-0.25(2) | - | ns |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

**Figure 16. HSI48 frequency versus temperature**




## Low-speed internal (LSI) RC oscillator

**Table 47. LSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | LSI Frequency | $V_{DD}$ = 3.0 V, $T_A$ = 30 °C | 31.04 | - | 32.96 | kHz |
| | | $V_{DD}$ = 1.62 to 3.6 V, TA = -40 to 125 °C | 29.5 | - | 34 | |
| $t_{SU}(LSI)$(2) | LSI oscillator start-up time | - | - | 80 | 130 | µs |
| $t_{STAB}(LSI)$(2) | LSI oscillator stabilization time | 5% of final frequency | - | 125 | 180 | µs |
| $I_{DD}(LSI)$(2) | LSI oscillator power consumption | - | - | 110 | 180 | nA |

1. Guaranteed by characterization results.
2. Guaranteed by design.

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 52. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8 MHz/ 80 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, UFQFPN32 package compliant with IEC 61967-2 | 0.1 MHz to 30 MHz | 1 | dBµV |
| | | | 30 MHz to 130 MHz | 0 | |
| | | | 130 MHz to 1 GHz | -1 | |
| | | | 1 GHz to 2 GHz | 7 | |
| | | | EMI Level | 1 | - |

## 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

**Table 53. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1 | C3 | 250 | |

1. Guaranteed by characterization results.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 17: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$, plus the maximum consumption of the MCU sunk on $V_{SS}$, cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 17: Voltage characteristics*).

### Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

**Table 57. Output voltage characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level voltage for an I/O pin | CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}$-0.4 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V | - | 1.3 | |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DDIOx}$-1.3 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.62$ V | - | 0.45 | |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DDIOx}$-0.45 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 2 mA 1.62 V ≥ $V_{DDIOx}$ ≥ 1.08 V | - | $0.35_x V_{DDIOx}$ | |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $0.65_x V_{DDIOx}$ | - | |
| $V_{OLFM+}$(3) | Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option) | $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | |
| | | $\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V | - | 0.4 | |
| | | $\|I_{IO}\|$ = 2 mA 1.62 V ≥ $V_{DDIOx}$ ≥ 1.08 V | - | 0.4 | |

1. The $I_{IO}$ current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\Sigma I_{IO}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 18* and *Table 58*, respectively.

**Table 66. ADC accuracy - limited test conditions 4(1)(2)(3)**

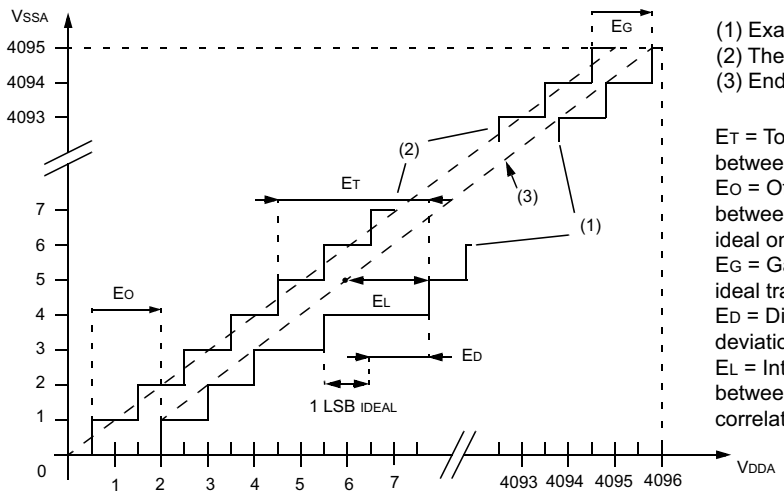
| Sym-bol | Parameter | Conditions(4) | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| ET | Total unadjusted error | ADC clock frequency ≤ 26 MHz, 1.65 V ≤ $V_{DDA}$ = VREF+ ≤ 3.6 V, Voltage scaling Range 2 | Single ended | Fast channel (max speed) | - | 5 | 5.4 | LSB |
| | | | | Slow channel (max speed) | - | 4 | 5 | |
| | | | Differential | Fast channel (max speed) | - | 4 | 5 | |
| | | | | Slow channel (max speed) | - | 3.5 | 4.5 | |
| EO | Offset error | | Single ended | Fast channel (max speed) | - | 2 | 4 | |
| | | | | Slow channel (max speed) | - | 2 | 4 | |
| | | | Differential | Fast channel (max speed) | - | 2 | 3.5 | |
| | | | | Slow channel (max speed) | - | 2 | 3.5 | |
| EG | Gain error | | Single ended | Fast channel (max speed) | - | 4 | 4.5 | |
| | | | | Slow channel (max speed) | - | 4 | 4.5 | |
| | | | Differential | Fast channel (max speed) | - | 3 | 4 | |
| | | | | Slow channel (max speed) | - | 3 | 4 | |
| ED | Differential linearity error | | Single ended | Fast channel (max speed) | - | 1 | 1.5 | |
| | | | | Slow channel (max speed) | - | 1 | 1.5 | |
| | | | Differential | Fast channel (max speed) | - | 1 | 1.2 | |
| | | | | Slow channel (max speed) | - | 1 | 1.2 | |
| EL | Integral linearity error | | Single ended | Fast channel (max speed) | - | 2.5 | 3 | |
| | | | | Slow channel (max speed) | - | 2.5 | 3 | |
| | | | Differential | Fast channel (max speed) | - | 2 | 2.5 | |
| | | | | Slow channel (max speed) | - | 2 | 2.5 | |
| ENOB | Effective number of bits | | Single ended | Fast channel (max speed) | 10.2 | 10.5 | - | bits |
| | | | | Slow channel (max speed) | 10.2 | 10.5 | - | |
| | | | Differential | Fast channel (max speed) | 10.6 | 10.7 | - | |
| | | | | Slow channel (max speed) | 10.6 | 10.7 | - | |
| SINAD | Signal-to-noise and distortion ratio | | Single ended | Fast channel (max speed) | 63 | 65 | - | dB |
| | | | | Slow channel (max speed) | 63 | 65 | - | |
| | | | Differential | Fast channel (max speed) | 65 | 66 | - | |
| | | | | Slow channel (max speed) | 65 | 66 | - | |
| SNR | Signal-to-noise ratio | | Single ended | Fast channel (max speed) | 64 | 65 | - | |
| | | | | Slow channel (max speed) | 64 | 65 | - | |
| | | | Differential | Fast channel (max speed) | 66 | 67 | - | |
| | | | | Slow channel (max speed) | 66 | 67 | - | |

**Table 66. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)**

| Symbol | Parameter | Conditions(4) | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion | ADC clock frequency ≤ 26 MHz, 1.65 V ≤ $V_{DDA}$ = VREF+ ≤ 3.6 V, Voltage scaling Range 2 | Single ended | Fast channel (max speed) | - | -71 | -69 | dB |
| | | | | Slow channel (max speed) | - | -71 | -69 | |
| | | | Differential | Fast channel (max speed) | - | -73 | -72 | |
| | | | | Slow channel (max speed) | - | -73 | -72 | |

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA}$ < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA}$ < 2.4 V). It is disable when $V_{DDA}$ ≥ 2.4 V. No oversampling.

**Figure 20. ADC accuracy characteristics**




(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

$E_T$ = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
$E_O$ = Offset Error: maximum deviation between the first actual transition and the first ideal one.
$E_G$ = Gain Error: deviation between the last ideal transition and the last actual one.
$E_D$ = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
$E_L$ = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

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**Table 67. DAC characteristics(1) (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{SAMP}$ | Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB) | DAC_OUT pin connected | DAC output buffer ON, $C_{SH}$ = 100 nF | - | 0.7 | 3.5 | ms |
| | | | DAC output buffer OFF, $C_{SH}$ = 100 nF | - | 10.5 | 18 | |
| | | DAC_OUT pin not connected (internal connection only) | DAC output buffer OFF | - | 2 | 3.5 | µs |
| $I_{leak}$ | Output leakage current | Sample and hold mode, DAC_OUT pin connected | | - | - | -(3) | nA |
| $CI_{int}$ | Internal sample and hold capacitor | - | | 5.2 | 7 | 8.8 | pF |
| $t_{TRIM}$ | Middle code offset trim time | DAC output buffer ON | | 50 | - | - | µs |
| $V_{offset}$ | Middle code offset for 1 trim code step | $V_{REF+}$ = 3.6 V | | - | 1500 | - | µV |
| | | $V_{REF+}$ = 1.8 V | | - | 750 | - | |
| $I_{DDA}$(DAC) | DAC consumption from $V_{DDA}$ | DAC output buffer ON | No load, middle code (0x800) | - | 315 | 500 | µA |
| | | | No load, worst code (0xF1C) | - | 450 | 670 | |
| | | DAC output buffer OFF | No load, middle code (0x800) | - | - | 0.2 | |
| | | Sample and hold mode, $C_{SH}$ = 100 nF | | - | 315 x Ton/(Ton +Toff) (4) | 670 x Ton/(Ton +Toff) (4) | |
| $I_{DDV}$(DAC) | DAC consumption from $V_{REF+}$ | DAC output buffer ON | No load, middle code (0x800) | - | 185 | 240 | µA |
| | | | No load, worst code (0xF1C) | - | 340 | 400 | |
| | | DAC output buffer OFF | No load, middle code (0x800) | - | 155 | 205 | |
| | | Sample and hold mode, buffer ON, $C_{SH}$ = 100 nF, worst case | | - | 185 x Ton/(Ton +Toff) (4) | 400 x Ton/(Ton +Toff) (4) | |
| | | Sample and hold mode, buffer OFF, $C_{SH}$ = 100 nF, worst case | | - | 155 x Ton/(Ton +Toff) (4) | 205 x Ton/(Ton +Toff) (4) | |

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

**Table 75. I2C analog filter characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50(2) | 260(3) | ns |

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

**Table 79. SAI characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{v(SD\_B\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) 2.7 ≤ $V_{DD}$ ≤ 3.6 | - | 22 | ns |
| | | Slave transmitter (after enable edge) 1.71 ≤ $V_{DD}$ ≤ 3.6 | - | 34 | |
| $t_{h(SD\_B\_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 10 | - | ns |
| $t_{v(SD\_A\_MT)}$ | Data output valid time | Master transmitter (after enable edge) 2.7 ≤ $V_{DD}$ ≤ 3.6 | - | 27 | ns |
| | | Master transmitter (after enable edge) 1.71 ≤ $V_{DD}$ ≤ 3.6 | - | 40 | |
| $t_{h(SD\_A\_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 10 | - | ns |

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

**Figure 28. SAI master timing waveforms**