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Understanding <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

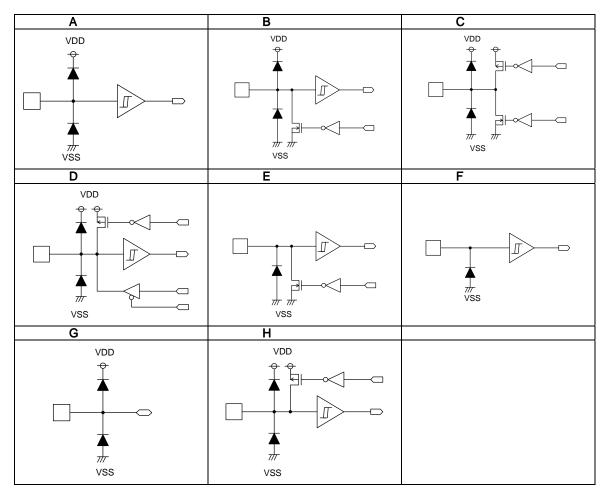
Details

Product Status	Obsolete
Туре	Audio
Interface	I ² C, 2-Wire Serial
Clock Rate	24.576MHz
Non-Volatile Memory	·
On-Chip RAM	1.375КВ
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-25°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-SSOP (0.213", 5.40mm Width)
Supplier Device Package	40-SSOP-B
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/bu9414fv-e2

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

• Pin Equivalent Circuit Diagrams



1.Command interface

I²C bus method is used in command interface with host CPU on BU9414FV.
In BU9414FV, not only writing but read-out is possible except for some registers.
Besides the slave address in BU9414FV, one byte select address can be Specified, written and readout.
The format of I²C bus slave mode is shown below.

	MSB	LSB	5	MSB	LSB		MSB	LSE	3	
S	Slave Address		А	Select Address		А	Data		А	Ρ

S: Start condition

Slave Address: Putting up the bit of read mode (H") or write mode (L") after slave address (7bit) set with ADDR, the data of eight bits in total will be sent. (MSB first)

A: The acknowledge bit in each byte adds into the data when acknowledge is sent and received.

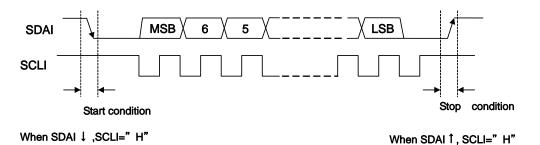
When data is correctly sent and received, "L" will be sent and received.

There was no acknowledge for "H".

Select Address: 1 byte select address is used in BU9414FV. (MSB first)

Data: Data-byte, data(MSB first)sent and received

P: Stop Condition



1-1. Data writing

S S	lave Add	lress	Α	Select	Address		A Dat	а	A P				
ADDR=	.0] : Fr	om maste	r to slave	E Fron	n slav	ve to master		
MSB							LSB	Setting	of BU9414FV sla		ddrees		
A6	A5	A4	A3	A2	A1	A0	R/W		rminal setting		Write-mode		1
1	0	0	0	0	0	0	0		ADDR		Slave-addres		
ADDR=	:1								0		80h		1
MSB							LSB		1		82h		
A6	A5	A4	A3	A2	A1	A0	R/W						-
1	0	0	0	0	0	1	0						
										_			
S SI	lave Add	dress	A Se	lect Add	dress	Α	Data	A	Data	Α	Data	А	Р
(examp	le) 8	80h		20h			00h : Fro	om master to	00h slave: I	From	00h slave to maste	er	

Writing procedure

Step	Clock	Master	Slave(BU9414FV)	Note
1		Start Condition		
2	7	Slave Address		
3	1	R/W (0)		&h80 (&h82)
4	1		Acknowledge	
5	8	Select Address		Writing object register 8 bit
6	1		Acknowledge	
7	8	Data		Writing data 8 bit
8	1		Acknowledge	
9		Stop Condition		

- The select address add +1 by auto increment function when the data is transferred continuously.

Repeat of Step 7~8.

1-2. Data readout

First of all, the readout target address(ex.&h20h) is written in &hD0 address register at the time of readout. In the following stream, data is read out after the slave address. Please do not return the acknowledge when ending the reception.

S	Slave A	ddress	А	Req_Addr	А	Select Ad	dress	А	Ρ						
(ex	(ample	80h		D0h		20h									
S	Slave A	ddress	А	Data 1	А	Data 2		Α				Α	Data N	Ā	Ρ
(ex	ample)	81h		**h		**h							**h		
	: M	aster to s	slave	e, 🗌 :	Slave	o master,	A : Wi	th a	ckno	owledg	ge,	Ā:w	ithout acknowledg	е	

Readout Procedure

Step	Clock	Master	Slave(BU9414FV)	Note
1		Start Condition		
2	7	Slave Address		8600 (8600)
3	1	R/W (0)		&h80 (&h82)
4	1		Acknowledge	
5	8	Req_Addr		Address for I ² C readout &hD0
6	1		Acknowledge	
7	8	Select Address		Readout object register 8 bit
8	1		Acknowledge	
9	1	Stop Condition		
10	1	Start Condition		
11	7	Slave Address		8 h 0 1 (8 h 0 2)
12	1	R/W (1)		&h81 (&h82)
13	1		Acknowledge	
14	8		Data	Readout data 8 bit
15	1	Acknowledge		
16		Stop Condition		

 The select address adds +1 by auto increment function when continuous data is transferred. Repeat Step14~15. Setting 3 of attack recovery detection time

 R_TIME_LOW is the setting of the initiation of P^2 Volume function's transition operation. If the input level above A continues more than continuation R_TIME_LOW in the state of (1), state transition of P2Volume will be started toward the state of (2) or (3).

Default = 0

Select Address	Operational explanation								
&h3B [6:4]	Command	R_TIME_LOW	Command	R_TIME_LOW					
	0	0.5ms	4	3ms					
	1	1ms	5	4ms					
	2	1.5ms	6	5ms					
	3	2ms	7	6ms					

•Scene change detection and High-speed recovery function (functioning only at the time of transition of (2)<->(3))

P²Volume function makes the P²Volume also compatible with large pulse sounds (clapping of hands, fireworks & shooting etc.) in addition to normal P²Volume operation. When large pulse sound is inputted, attack operation (A_RATE) or recovery operation (R_RATE) is performed at 4 or 64 times the speed of normal attack operation or recovery operation. Selection of using the scene change detection function.

Default = 0

Select Address	Value	Operational explanation
&h3C[7]	0	Not using of pulse sound detection function
	1	Using of pulse sound detection function

Selection of operating times of Recovery Time (R_RATE) in the case of using the scene change detection function. (Operating-time selection at the time of R_RATE / scene detection) serves as a recovery time.

Default = 0

	Value
Oper	ational exp
Command	Value
0	4
1	8
2	16
3	64
	Command 0 1 2

Selection of scene change detection time

Select Address	Operational explanation									
&h3C [6:4]		Command	Time	Command	Time					
		0	50ms	4	300ms					
		1	100ms	5	400ms					
		2	150ms	6	500ms					
		3	200ms	7	600ms					
				•						

Selection of frequency (F_0)

Default = 0Eh

Select Address							Opera	ational	explai	nation						
&h45 [5:0]	Comman	Frequency	Command	Frequency												
	00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
	01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
	02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
	03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
	04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
	05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	-
	06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	-
	07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	-

Selection of quality factor (Q)

Default = 4h

Select Address	Operational explanation								
&h46 [3:0]	Command	Quality factor	Command	Quality factor					
	0	0.33	8	2.2					
	1	0.43	9	2.7					
	2	0.56	А	3.3					
	3	0.75	В	3.9					
	4	1.0	С	4.7					
	5	1.2	D	5.6					
	6	1.5	E	6.8					
	7	1.8	F	8.2					

Selection of Gain

Default = 40h

Select Address	Operational explanation		
&h47 [6:0]	Command	Gain	
	1C	-18dB	
	÷	:	
	3E	-1dB	
	3F	-0.5dB	
	40	0dB	
	41	+0.5dB	
	42	+1dB	
	:	:	
	64	+18dB	

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

4-8. TREBLE

TREBLE of TONE Control can use Peaking filter or High-shelf filter.

The setting is converted, in the IC, into digital filter's coefficients (b0, b1, b2, a1, a2) by selecting the F_0 , Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

oTREBLE Control

Selection of filter types

Default = 0

Select Address	Value	Operational explanation
&h48 [7]	0	Peaking filter
	1	High-shelf filter

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation	
&h48 [6]	0	Using smooth transition function	
	1	Not using smooth transition function	

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h48 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h48[0] command, to the coefficient RAM for smooth transition, the alteration of TREBLE's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation	
&h4C [2]	0	TREBLE smooth transition stop	
	1	TREBLE smooth transition start	

What is necessary is the time of waiting, which is more than the time selected by the setting of TREBLE smooth transition time, from the time the TREBLE smooth transition start (\$h4C[2] = "1") is executed until the following command is sent. Please make sure to perform the TREBLE smooth transition stop (\$h4C[2] = "0") after the smooth transition is completed.

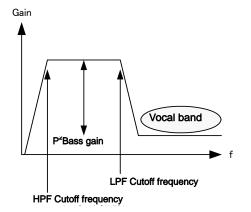
&h4D [0] and &hF4 [0] are set to H during soft transition.(Refer to Chapter 15)

4-9. P²Bass (Perfect Pure Bass : Deep Bass Equalizer)

It is the deep bass equalizer making it possible that even thin-screen TV, by which the enclosure of speaker is restricted, can reproduce the real sound close to powerful deep bass & original sound.

Solid & clear deep bass with little feeling of distortion is realized. Even boosting of bass does not interfere with vocal band,

therefore rich and natural deep band is realized.



ON/OFF of P²Bass function

Select Address	Value	Operational explanation	
&h73 [7]	0	Not using of P ² Bass function	
	1	Using of P ² Bass function	

BU9414FV

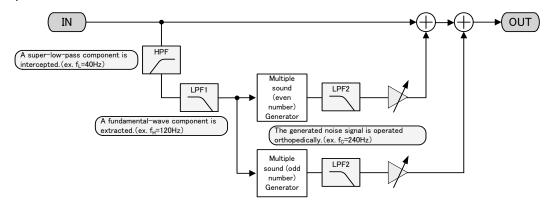
4-10. Pseudo bass (Double sound)

A Pseudo bass function is a function which turns into that it is possible to emphasize low frequency sound effectively also to the low speaker of low-pass reproduction capability.

In order to be audible as the fundamental wave is sounding in false by adding 2 double sound and 3 time sound to a fundamental wave, the reproduction capability of the band of a fundamental wave becomes possible.

Although use independently is also possible for a pseudo bass function, low-pitched sound can be emphasized more by combining with P2Bass function.

Moreover, since it is possible to change the band to emphasize, optimizing to the frequency characteristic of the speaker to be used is possible.



ON/OFF of pseudo bass function

Pseudo bass sound (3 time sound) is used.

Default = 0

Select Address	Value	Operational explanation	
&h7B [7]	0	Not using of pseudo bass(3 time sound) function	
	1	Using of pseudo bass(3 time sound) function	

Pseudo bass sound (2 time sound) is used.

Default = 0

Select Address	Value	Operational explanation
&h7B [6]	0	Not using of pseudo bass(2 time sound) function
	1	Using of pseudo bass(2 time sound) function

Setting of pseudo bass input HPF

Default = 00h

Select Address	Operational explanation				
&h7B [2 : 0]		Command	Frequency	Command	Frequency
		0	OFF	4	50Hz
		1	20Hz	5	60Hz
		2	30Hz	6	70Hz
		3	40Hz	7	80Hz

Setting of order of LPF for 2 or 3 time sound.

Select Address	Value	Operational explanation
&h7C [7]	0	2nd order
	1	4th order

4-12. Scaler

Scaler adjusts the gain in order to prevent the overflow in DSP.

Adjustable range is +24dB to -103dB and can be set by the step of 0.5dB.

Scaler 1 does not incorporate the smooth transition function.

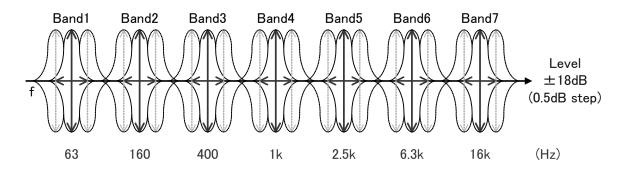
Default = 30h

Select Address	Operat	ional expl
&h24 [7 : 0]	Command	Gain
anz4[7.0]	00	+24dB
	01	+23.5dB
	:	:
	30	0dB
	31	-0.5dB
	32	-1dB
	:	:
	FE	-103dB
	FF	-00

4-13. 7 band • parametric equalizer

7-band parametric equalizer can use Peaking filter, Low-shelf filter or high-shelf filter.

The setting is converted, in the IC, into digital filter's coefficients (b0, b1, b2, a1, a2) by selecting the F, Q and Gain, and transmitted to coefficient RAM. There is no smooth transition function.



Selection of filter types

Default = 0

Select Address	Value	Operational explanation
bit[7:6]	0	Peaking filter
It sets to all band	1	Low-shelf filter
	2	High-shelf filter

Setting of the Start of transmitting to coefficient RAM

It is transmitted to direct coefficient RAM.

Select Address	Value	Operational explanation
bit [0]	0	Coefficient transmission stop
It sets to all band	1	Coefficient transmission start

4-14. Main output EVR (Electronic volume)

Volume is from+24dB to -103dB, and can be selected by the step of 0.5dB.

At the time of switching of Volume, smooth transition is performed. The smooth transition time takes about 22ms in the case of transiting from 0dB. (Fixed)

Setting of Volume

Default = FFh

Select Address	Operational explanation			
&h26 [7 : 0]	Command	Gain		
	00	+24dB		
	01	+23.5dB		
	:	:		
	30	0dB		
	31	-0.5dB		
	32	-1dB		
	:	:		
	FE	-103dB		
	FF	-∞		

4-15. Main output balance

Balance can be attenuated, by the step width of 1dB, from the Volume setting value. At the time of switching, smooth transition is performed. At the time of switching of Balance, smooth transition is performed. The smooth transition time takes about 22ms. (Fixed)

Setting of L/R Balance

Default = 80h

Select Address	Operational explanation				
&h27 [7 : 0]	Command	Lch	Rch		
	00	0dB	-∞		
	01	0dB	-126dB		
	:	:	:		
	7E	0dB	-1dB		
	7F	0dB	0dB		
	80	0dB	0dB		
	81	-1dB	0dB		
	:	:	:		
	FE	-126dB	0dB		
	FF	-∞	0dB		

4-16. Main output postscaler

It performs the level adjustment when the data calculated in the 32-bit-width DSP is outputted in the form of 24bitwidth. Adjustable range is from +24dB to -103dB and can be set by the step of 0.5dB.

There is no smooth transition function in Postscaler.

Default = 30h

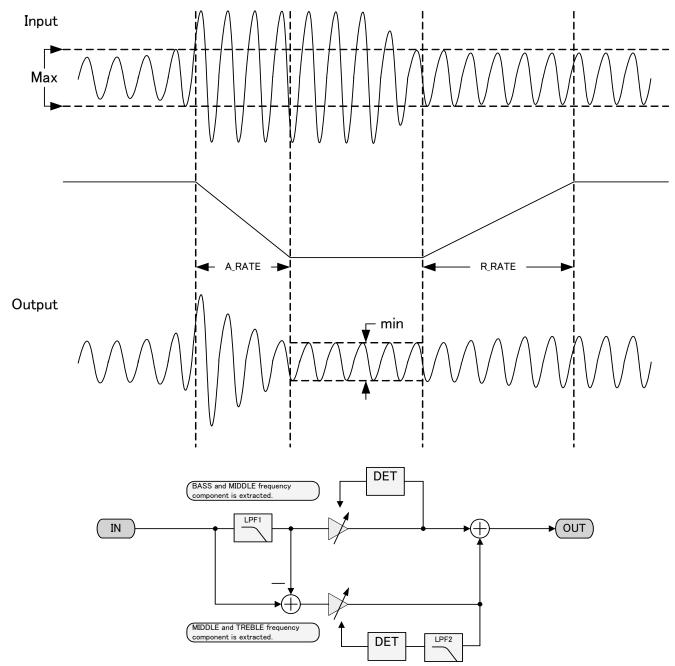
Select Address	Operational explanation				
&h28 [7 : 0]	Command Gain	n			
	00 +24dE	IB			
	01 +23.5d	dB			
	: : :				
	30 0dB	3			
	31 –0.5d	βB			
	32 -1 dB	В			
	: : :				
	FE -103d	dB			
	FF –∞)			

4-17. 2 Band dynamic range compression

Like the explosion in TV commercials or a movie, it is the function to control volume automatically and to adjust volume so that a televiewer may not be surprised, when sound becomes large suddenly.

Compression operation is performed about each two band of low-pass and a high region.

Moreover, the high region builds in LPF for preventing the incorrect reaction to the pilot signal of an image.



ON/OFF low frequency DRC .

Select Address	Value	Operational explanation
&h18 [7]	0	Use low frequency DRC
	1	Not use low frequency DRC

ON/OFF high frequency DRC .

Default = 0

	Select Address	Value	Operational explanation
ſ	&h18 [6]	0	Use high frequency DRC
		1	Not use high frequency DRC

Setting of LPF(LPF2) .

Default = 0

Select Address	Value	Operational explanation
&h19 [5:4]	0	OFF
	1	1st order
	2	2nd order

Setting of LPF(LPF1) .

Default = 00h

Select Address	Operational explanation				
&h19[3:0]	Command	Frequency	Command	Frequency	
	0	スルー	8	1600Hz	
	1	200Hz	9	1800Hz	
	2	400Hz	A	2000Hz	
	3	600Hz	В	-	
	4	800Hz	С	-	
	5	1000Hz	D	-	
	6	1200Hz	E	-	
	7	1400Hz	F	-	

Setting of low frequency A_RATE.

Default = 0h

Select Address	Operational explanation				
&h1A [6 : 4]	Γ	Command	Time	Command	Time
	Γ	0	1ms	4	5ms
		1	2ms	5	10ms
		2	3ms	6	20ms
		3	4ms	7	40ms

Setting of low frequency R_RATE.

Default = 0h

Select Address	Operational explanation				
&h1A [3 : 0]					
	Command	R_RATE	Command	R_RATE	
	0	0.25s	8	3s	
	1	0.5s	9	4s	
	2	0.75s	A	5s	
	3	1s	В	6s	
	4	1.25s	С	7s	
	5	1.5s	D	8s	
	6	2s	E	9s	
	7	2.5s	F	10s	

4-20. Sub output EVR (electronic volume)

The volume for sub output can select with 0.5dB step from +24dB to -103dB.

When changing volume, smooth transition is done. Smooth transition duration is required approximately 22ms when it is from 0dB. (Fixed)

Volume setting

Default = FFh

Select Address	Operating explanation				
&h2C [7 : 0]	Comma	and	Gain		
····=•[···•]	00		+24dB		
	01		+23.5dB		
	:		÷		
	30		0dB		
	31		-0.5dB		
	32		−1dB		
	:		÷		
	FE		-103dB		
	FF		-∞		

4-21. Sub output balance

As for sub output balance, it is possible to be attenuated at 1dB step width from volume setting value. When changing, smooth transition is done.

When changing balance, smooth transition is done. Smooth transition duration is required approximately 22ms. (Fixed) L/R Balance setting

Default = 80h

Select Address	Operating	explanat	ion
&h2D [7 : 0]	Command	Lch	Rch
	00	0dB	-∞
	01	0dB	-126dB
	:	÷	÷
	7E	0dB	−1dB
	7F	0dB	0dB
	80	0dB	0dB
	81	−1dB	0dB
	:	÷	÷
	FE	-126dB	0dB
	FF	-∞	0dB

4-22. Sub output post scaler

The occasion when the data which is calculated with DSP of 32bit width is output at 24bit width, level adjustment is done.

The adjustment range can be set with 0.5dB step from +24dB to -103dB.

There is no smooth transition function in the sub output post scaler.

Default = 30h

Select Address	Operating explanation			
&h2E [7 : 0]	Command	Gain		
	00	+24dB		
	01	+23.5dB		
	:	:		
	30	0dB		
	31	-0.5dB		
	32	-1dB		
	:	:		
	FE	-103dB		
	FF	-∞		

4-28. About the automatic renewal of five coefficients of b0, b1, b2, a1 and a2 of Bi-quad Filter

BASS, MIDDLE, TREBLE, main output 7 bands Parametric Equalizer and sub output 3 band Parametric Equalizer have used coefficient RAM. As for this coefficient RAM, because direct access is not possible from the micro-computer, it cannot refresh the register efficiently.

There is an automatic renewal function of coefficient RAM in this DSP, the automatic write-in renewal of coefficient RAM is possible by using this function. However when 4-26 [[] the function of direct setting a coefficient RAM] is utilized, it is not possible to utilize automatic write-in renewal.

Selection of using the automatic write-in renewal function

Default = 0

Select Address	Value	Operating explanation	
&h6D [0]	0	Automatic write-in renewal function is used	
	1	Automatic write-in renewal function is not used	

The separate setting of Filter of automatic write-in renewal function

Default = 00h

Select Address	Filter	Operating explanation	
&h6E [0]	BASS	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6E [1]	MIDDLE	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6E [2]	TREBLE	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6F [0]	Main MAND1	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6F [1]	Main MAND2	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6F [2]	Main MAND3	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6F [3]	Main MAND4	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6F [4]	Main MAND5	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6F [5]	Main MAND6	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	
&h6F [6]	Main MAND7	0 : Automatic renewal function OFF	
		1 : Automatic renewal function ON	

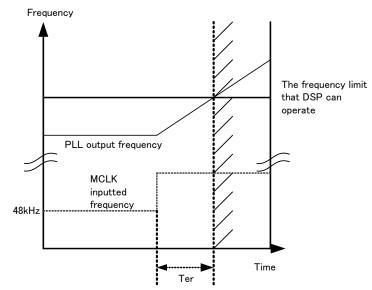
12. When the clock which exceeded the specification range from MCLK is inputted

When the frequency beyond fs=48kHz is inputted from MCLK in the state where it was set as &h08 [5:4] =1, since PLL follows inputted MCLK, as shown in the right figure, when it exceeds Time Ter, it will exceed the frequency in which DSP can operate.

In this case, an allophone may carry out irrespective of the existence of data.

When you change into such a state, please carry out the mute of the DAC immediately, apply reset (RESETB=L), and do the work after reset release of Chapter 8.

The time of Ter serves as about 70 usec.



13. Audio Interface Signal Specification

 $\circ \textsc{Electric}$ specification and timing of MCK, BCK, LRCK, and SDATA1 and SDATA2

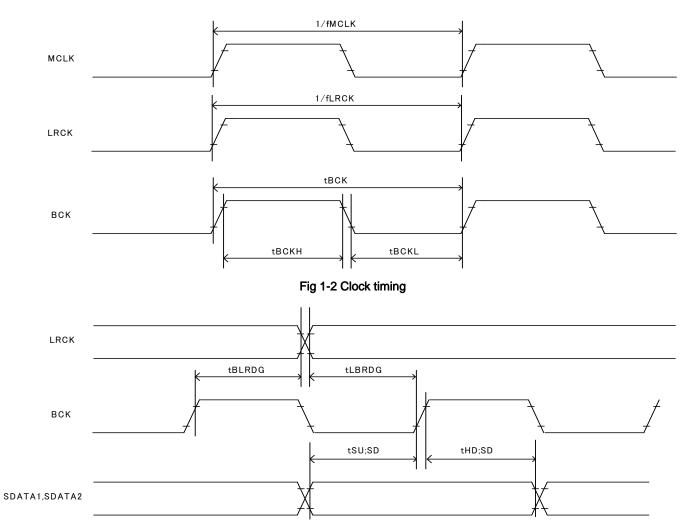


Fig 1-3 Audio interface timing

Parameter		Sign	Min.	Max.	Unit	
1	MOK	Frequency	fSCLK	4.096	24.576	MHz
2	2 MCK	DUTY	dSCLK	40	60	%
3		Frequency	fLRCK	32	48	kHz
4		DUTY	dLRCK	40	60	%
5	BCK	Cycle	tBCK	325	—	ns
6		H width	tBCKH	130	_	ns
7		L width	tBCKL	130	_	ns
8	8 It is time to the edge of LRCK from a BCK rising edge.*1		tBLRDG	20	_	ns
9	9 It is time to a BCK rising edge from the edge of LRCK.*1		tLBRDG	20	-	ns
10 Setup time of SDATA		tSU;SD	20	-	ns	
11	11 Hold time of SDATA		tHD;SD	20	_	ns

*1 This standard value has specified that the edge of LRCK and the rising edge of BCK do not overlap.

14. Notes at the Time of Reset

Since the state of IC is not decided, please make it into RESETX=L at the time of a power supply injection, and surely apply reset.

Reset of BU9414FV is performing noise removal by MCLK.

Therefore, in order to apply reset, a MCLK clock pulse is required of the state of RESETX=L more than 10 times.

The power-on reset after a power supply injection, and when you usually apply reset at the time of operation, please be sure to carry out in the state where the clock is inputted, from MCLK.

15. Read-out of Soft Transition Flag

It is set to &hF4[0] =H, &hFD[0]=H when BASS, MIDDLE, TREBLE or P2Bass, and P2Treble are soft transiting.

It is possible to check whether soft transition is completed by reading &hF4 [0]or &hFD[0]

Soft transition will be completed if the read-out result of &hF4 [0] or &hFD [0] is L.

16. Data taking-in position adjustment circuit

There is a circuit which adjusts the position of data taking in so that data can be received, even when the incoming signal is shaking by jitter.

DSP clock use multiplied input clock by PLL.

Even when I2S signal inputted is shaking by jitter, the taking-in position of data is adjusted to the position which has a margin most so that take data and they may not be spilt.

Adjust a data taking-in position by making it &hAA[7] =H.

The read-out value of &hAA[7] is set to H during adjustment of a data taking-in position.

It reads, after adjustment of a data taking-in position finishes, and a value is set to L.

The reset release back, the time of an input sampling rate change, etc. adjust, when the lock state of PLL changes.

Please refer to the recommendation procedure of Chapter 8 and Chapter 11 for details.

When there is no margin in the data taking-in position of DSP, the read-out value of &hAA[3] is set to H.

& Once hAA [3] is set to H, it will read until it adjusts a data taking-in position or writes 0 in &hAA[3], and a value will not be set to L.

Operational Notes

(1) ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur and break mode (open or short) can not be specified if power supply, operating temperature, and those of ABSOLUTE MAXIMUM RATINGS are exceeded. If such a special condition is expected, components for safety such as fuse must be used.

(2)Regarding of SCLI and SDAI terminals

ŠCLI and the SDAI terminal do not support 5 V-tolerant. Please use it within absolute maximum rating (4.5V).

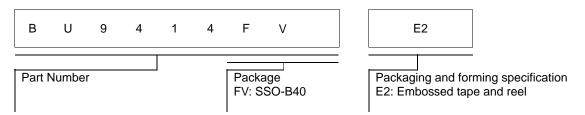
(3) Power Supply

Power and Ground line must be designed as low impedance in the PCB. Print patterns if digital power supply and analog power supply must be separated even if these have same voltage level. Print patterns for ground must be designed as same as power supply. These considerations avoid analog circuits from the digital circuit noise. All pair of power supply and ground must have their own de-coupling capacitor. Those capacitor should be checked about their specification, etc. (nominal electrolytic capacitor degrades its capacity at low temperature) and choose the constant of an electrolytic capacitor.

- (4) Functionality in the strong electro-magnetic field
- Malfunction may occur if in the strong electro-magnetic field.
- (5) Input terminals

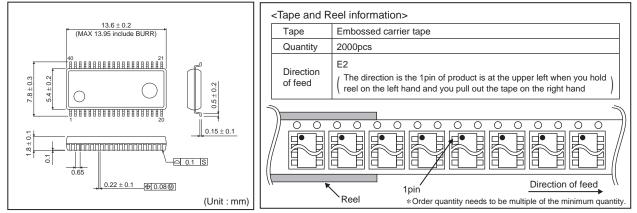
All LSI contain parasitic components. Some are junctions which normally reverse bias. When these junctions forward bias, currents flows on unwanted path, malfunction or device damage may occur. To prevent this, all input terminal voltage must be between ground and power supply, or in the range of guaranteed value in the Electrical characteristics. And no voltage should be supplied to all input terminal when power is not supplied.

Ordering Information

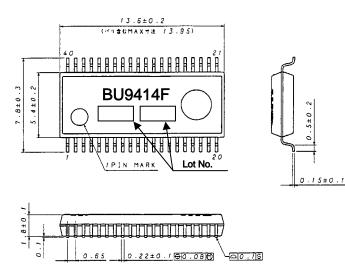


Physical Dimension Tape and Reel Information

SSOP-B40



Marking Diagram(s)(TOP VIEW)



General Precaution

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