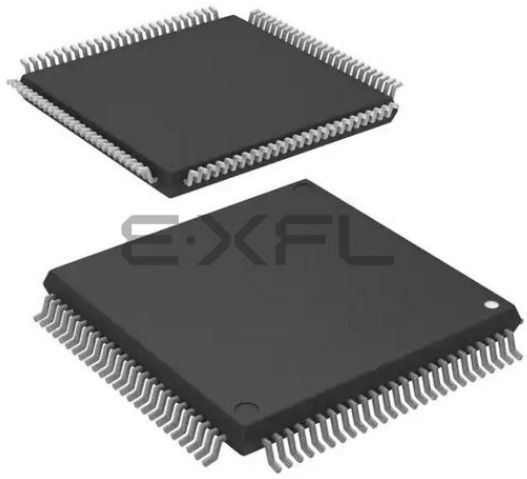
Renesas Electronics America Inc - M30880FWTGP#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30880fwtgp-u0

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/88 Group (1) (T version, M32C/88T) **As of October, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30882FJTGP (D)	PLQP0144KA-A (144P6Q-A)	512K+4K	18K	Flash Memory T version (High-reliability 85° C)
M30880FJTGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FHTGP (D)	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30880FHTGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FWTGP (D)	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30880FWTGP (D)	PLQP0100KB-A (100P6Q-A)			

(D): Under development

Table 1.3 M32C/88 Group (2) (U version, M32C/88T) **As of October, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30882FJUGP (D)	PLQP0144KA-A (144P6Q-A)	512K+4K	18K	Flash Memory U version (High-reliability 105° C)
M30880FJUGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FHUGP (D)	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30880FHUGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FWUGP (D)	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30880FWUGP (D)	PLQP0100KB-A (100P6Q-A)			

(D): Under development

NOTE:

Contact our sales office if you are interested in the V version.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
49		$P13_6$					
50		$P13_5$					
51		$P13_4$					
52		$P5_7$					
53		$P5_6$					
54		$P5_5$					
55		$P5_4$					
56		$P13_3$					
57	V_{SS}						
58		$P13_2$					
59	V_{CC}						
60		$P13_1$					
61		$P13_0$					
62		$P5_3$					
63		$P5_2$					
64		$P5_1$					
65		$P5_0$					
66		$P12_7$					
67		$P12_6$					
68		$P12_5$					
69		$P4_7$					
70		$P4_6$					
71		$P4_5$					
72		$P4_4$					
73	V_{CC}	$P4_3$					
74							
75	V_{SS}	$P4_2$					
76							
77		$P4_1$					
78		$P4_0$					
79		$P3_7$					
80		$P3_6$					
81		$P3_5$					
82		$P3_4$					
83		$P3_3$					
84		$P3_2$					
85		$P3_1$					
86		$P12_4$					
87		$P12_3$					
88		$P12_2$					
89		$P12_1$					
90	V_{CC}	$P12_0$					
91	V_{SS}						
92		$P3_0$					
93							
94		$P2_7$					$AN2_7$
95		$P2_6$					$AN2_6$
96		$P2_5$					$AN2_5$

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Function
Reference Voltage Input	V_{REF}	I	Applies reference voltage to the A/D converter and D/A converter
A/D Converter	AN_0 to AN_7 $AN0_0$ to $AN0_7$ $AN2_0$ to $AN2_7$	I	Analog input pins for the A/D converter
	$\overline{ADTRG}$	I	Input pin for an external A/D trigger
	ANEX0	I/O	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	Extended analog input pin for the A/D converter
D/A Converter	DA0, DA1	O	Output pin for the D/A converter
Intelligent I/O	$INPC1_0$ to $INPC1_7$	I	Input pins for the time measurement function
	$OUTC1_0$ to $OUTC1_7$	O	Output pins for the waveform generating function ($OUTC1_6$ and $OUTC1_7$ assigned to $P7_0$ and $P7_1$ are pins for the N-channel open drain output.)
	ISCLK0	I/O	Inputs and outputs the clock for the intelligent I/O communication function
	ISCLK1		
	ISRXD0	I	Inputs data for the intelligent I/O communication function
	ISRXD1		
	ISTXD0	O	Outputs data for the intelligent I/O communication function
	ISTXD1		
	$BE1_{IN}$	I	Inputs data for the intelligent I/O communication function
	$BE1_{OUT}$	O	Outputs data for the intelligent I/O communication function
CAN	$CAN0_{IN}$	I	Input pin for the CAN communication function
	$CAN02_{IN}$		
	$CAN1_{IN}$		
	$CAN2_{IN}$		
	$CAN0_{OUT}$	O	Output pin for the CAN communication function
	$CAN02_{OUT}$		
	$CAN1_{OUT}$		
	$CAN2_{OUT}$		
	$\overline{CAN1WU}$	I	Input pin for the CANi wake-up interrupt (i=1, 2)
	$\overline{CAN2WU}$		
I/O Ports	$P0_0$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$	I/O	8-bit I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P9_0$ to $P9_7$ $P10_0$ to $P10_7$	I/O	I/O ports having equivalent functions to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
	$P8_0$ to $P8_4$ $P8_6$, $P8_7$	I/O	I/O ports having equivalent functions to P0
Input Port	$P8_5$	I	Shares a pin with $\overline{NMI}$. $\overline{NMI}$ input state can be got by reading $P8_5$

I : Input O : Output I/O : Input and output

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

4. Special Function Registers (SFRs)

Address	Register	Symbol	Value after RESET
000016			
000116			
000216			
000316			
000416	Processor Mode Register(1)	PM0	1000 00002(CNVss pin ="L")
000516	Processor Mode Register 1	PM1	0016
000616	System Clock Control Register 0	CM0	0000 10002
000716	System Clock Control Register 1	CM1	0010 00002
000816			
000916	Address Match Interrupt Enable Register	AIER	0016
000A16	Protect Register	PRCR	XXXX 00002
000B16			
000C16	Main Clock Division Register	MCD	XXX0 10002
000D16	Oscillation Stop Detection Register	CM2	0016
000E16	Watchdog Timer Start Register	WDTS	XX16
000F16	Watchdog Timer Control Register	WDC	000X XXXX2
001016 001116 001216	Address Match Interrupt Register 0	RMAD0	00000016
001316	Processor Mode Register 2	PM2	0016
001416 001516 001616	Address Match Interrupt Register 1	RMAD1	00000016
001716			
001816 001916 001A16	Address Match Interrupt Register 2	RMAD2	00000016
001B16			
001C16 001D16 001E16	Address Match Interrupt Register 3	RMAD3	00000016
001F16			
002016			
002116			
002216			
002316			
002416			
002516			
002616	PLL Control Register 0	PLC0	0001 X0102
002716	PLL Control Register 1	PLC1	000X 00002
002816 002916 002A16	Address Match Interrupt Register 4	RMAD4	00000016
002B16			
002C16 002D16 002E16	Address Match Interrupt Register 5	RMAD5	00000016
002F16			

X: Indeterminate
Blank spaces are reserved. No access is allowed.
NOTE:
1. The PM01 and PM00 bits in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
006016			
003016			
003116			
003216			
003316			
003416			
003516			
003616			
003716			
003816 003916 003A16	Address Match Interrupt Register 6	RMAD6	00000016
003B16			
003C16 003D16 003E16	Address Match Interrupt Register 7	RMAD7	00000016
003F16			
004016			
004116			
004216			
004316			
004416			
004516			
004616			
004716			
004816			
004916			
004A16			
004B16			
004C16			
004D16			
004E16			
004F16			
005016			
005116			
005216			
005316			
005416			
005516	Flash Memory Control Register 1	FMR1	0000 01012
005616			
005716	Flash Memory Control Register 0	FMR0	0000 00012
005816			
005916			
005A16			
005B16			
005C16			
005D16			
005E16			
005F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
021016 021116	CAN0 Slot Interrupt Mask Register	C0SIMKR	0016(2) 0016(2)
021216			
021316			
021416	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X0002(2)
021516	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X0002(2)
021616	CAN0 Error Cause Register	C0EFR	0016(2)
021716	CAN0 Baud Rate Prescaler	C0BRP	0000 00012(2)
021816			
021916	CAN0 Mode Register	C0MDR	XXXX XX002(2)
021A16			
021B16			
021C16			
021D16			
021E16			
021F16			
022016 022116	CAN0 Single Shot Control Register	C0SSCTLR	0016(2) 0016(2)
022216			
022316			
022416 022516	CAN0 Single Shot Status Register	C0SSSTR	0016(2) 0016(2)
022616			
022716			
022816	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 00002(2)
022916	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 00002(2)
022A16	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 00002(2)
022B16	CAN0 Global Mask Register Extended ID1	C0GMR3	0016(2)
022C16	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 00002(2)
022D16			
022E16			
022F16			
023016	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 00002(2) XXX0 00002(2)
023116	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 00002(2) XX00 00002(2)
023216	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 00002(2) XXXX 00002(2)
023316	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	0016(2) 0016(2)
023416	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 00002(2) XX00 00002(2)
023516	CAN0 Message Slot 5 Control Register	C0MCTL5	0016(2)
023616	CAN0 Message Slot 6 Control Register	C0MCTL6	0016(2)
023716	CAN0 Message Slot 7 Control Register	C0MCTL7	0016(2)
023816	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 00002(2) XXX0 00002(2)
023916	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
02BA16	CAN1 Message Slot 10 Control Register / CAN1 Local Mask Register B Extended ID0	C1MCTL10/ C1LMBR2	0000 00002(2) XXXX 00002(2)
02BB16	CAN1 Message Slot 11 Control Register / CAN1 Local Mask Register B Extended ID1	C1MCTL11/ C1LMBR3	0016(2) 0016(2)
02BC16	CAN1 Message Slot 12 Control Register / CAN1 Local Mask Register B Extended ID2	C1MCTL12/ C1LMBR4	0000 00002(2) XX00 00002(2)
02BD16	CAN1 Message Slot 13 Control Register	C1MCTL13	0016(2)
02BE16	CAN1 Message Slot 14 Control Register	C1MCTL14	0016(2)
02BF16	CAN1 Message Slot 15 Control Register	C1MCTL15	0016(2)
02C016 02C116	X0 Register Y0 Register	X0R,Y0R	XX16 XX16
02C216 02C316	X1 Register Y1 Register	X1R,Y1R	XX16 XX16
02C416 02C516	X2 Register Y2 Register	X2R,Y2R	XX16 XX16
02C616 02C716	X3 Register Y3 Register	X3R,Y3R	XX16 XX16
02C816 02C916	X4 Register Y4 Register	X4R,Y4R	XX16 XX16
02CA16 02CB16	X5 Register Y5 Register	X5R,Y5R	XX16 XX16
02CC16 02CD16	X6 Register Y6 Register	X6R,Y6R	XX16 XX16
02CE16 02CF16	X7 Register Y7 Register	X7R,Y7R	XX16 XX16
02D016 02D116	X8 Register Y8 Register	X8R,Y8R	XX16 XX16
02D216 02D316	X9 Register Y9 Register	X9R,Y9R	XX16 XX16
02D416 02D516	X10 Register Y10 Register	X10R,Y10R	XX16 XX16
02D616 02D716	X11 Register Y11 Register	X11R,Y11R	XX16 XX16
02D816 02D916	X12 Register Y12 Register	X12R,Y12R	XX16 XX16
02DA16 02DB16	X13 Register Y13 Register	X13R,Y13R	XX16 XX16
02DC16 02DD16	X14 Register Y14 Register	X14R,Y14R	XX16 XX16
02DE16 02DF16	X15 Register Y15 Register	X15R,Y15R	XX16 XX16

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C1CTLR1 register switches functions for addresses 02A016 to 02BF16.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
02E0₁₆	X/Y Control Register	XYC	XXXX XX00₂
02E1₁₆			
02E2₁₆			
02E3₁₆			
02E4₁₆	UART1 Special Mode Register 4	U1SMR4	00₁₆
02E5₁₆	UART1 Special Mode Register 3	U1SMR3	00₁₆
02E6₁₆	UART1 Special Mode Register 2	U1SMR2	00₁₆
02E7₁₆	UART1 Special Mode Register	U1SMR	00₁₆
02E8₁₆	UART1 Transmit/Receive Mode Register	U1MR	00₁₆
02E9₁₆	UART1 Bit Rate Register	U1BRG	XX₁₆
02EA₁₆ 02EB₁₆	UART1 Transmit Buffer Register	U1TB	XX₁₆ XX₁₆
02EC₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000₂
02ED₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010₂
02EE₁₆ 02EF₁₆	UART1 Receive Buffer Register	U1RB	XX₁₆ XX₁₆
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Bit Rate Register	U4BRG	XX₁₆
02FA₁₆ 02FB₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆ XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆ 02FF₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆ XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆ 0303₁₆	Timer A1-1 Register	TA11	XX₁₆ XX₁₆
0304₁₆ 0305₁₆	Timer A2-1 Register	TA21	XX₁₆ XX₁₆
0306₁₆ 0307₁₆	Timer A4-1 Register	TA41	XX₁₆ XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
037016			
037116			
037216			
037316			
037416			
037516			
037616			
037716			
037816	DMA0 Request Source Select Register	DM0SL	0X00 00002
037916	DMA1 Request Source Select Register	DM1SL	0X00 00002
037A16	DMA2 Request Source Select Register	DM2SL	0X00 00002
037B16	DMA3 Request Source Select Register	DM3SL	0X00 00002
037C16 037D16	CRC Data Register	CRCD	XX16 XX16
037E16	CRC Input Register	CRCIN	XX16
037F16			
038016 038116	A/D0 Register 0	AD00	XXXX XXXX2 0000 00002
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216	A/D0 Control Register 4	AD0CON4	XXXX 00XX2
039316			
039416	A/D0 Control Register 2	AD0CON2	XX0X X0002
039516	A/D0 Control Register 3	AD0CON3	XXXX X0002
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$	Function Select Register A8	PS8	X000 0000$_2$
03A1$_{16}$	Function Select Register A9	PS9	00$_{16}$
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$	Function Select Register A5	PS5	XXX0 0000$_2$
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$	Port P11 Register	P11	XX$_{16}$
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Port P11 Direction Register	PD11	XXX0 0000$_2$
03CC$_{16}$	Port P12 Register	P12	XX$_{16}$
03CD$_{16}$	Port P13 Register	P13	XX$_{16}$
03CE$_{16}$	Port P12 Direction Register	PD12	00$_{16}$
03CF$_{16}$	Port P13 Direction Register	PD13	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Set default value to "FF$_{16}$"		
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$	Set default value to "FF$_{16}$"		
03CF$_{16}$	Set default value to "FF$_{16}$"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter			Condition	Value	Unit
V_{CC}	Supply Voltage			V_{CC}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog Supply Voltage			V_{CC}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}			-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$			-0.3 to 6.0	
V_O	Output Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}			-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$			-0.3 to 6.0	
Pd	Power Dissipation		T version	Topr=25° C	500	mW
			U version		400	
Topr	Operating Ambient Temperature	during CPU operation	T version		-40 to 85	° C
			U version		-40 to 105	
		during flash memory program and erase operation			0 to 60	
Tstg	Storage Temperature				-65 to 150	° C

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

Table 5.2 Recommended Operating Conditions

(Vcc=4.2 to 5.5V, Vss=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply Voltage		4.2	5.0	5.5	V
AV_{CC}	Analog Supply Voltage			V_{CC}		V
V_{SS}	Supply Voltage			0		V
AV_{SS}	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4), $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC}		V_{CC}	V
		$P7_0$, $P7_1$	0.8V_{CC}		6.0	
V_{IL}	Input Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4), $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC}	V
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100 ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80 mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80 mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40 mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40 mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40 mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. Ports P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

Table 5.4 Electrical Characteristics

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5 mA	V_{CC}-2.0		V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200 µA	V_{CC}-0.3		V_{CC}	V
		X_{OUT}	I_{OH}=-1 mA	3.0			V
		X_{COUT} High Power	No load applied		2.5		V
		X_{COUT} Low Power	No load applied		1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200 µA			0.45	V
		X_{OUT}	I_{OL}=1 mA			2.0	V
		X_{COUT} High Power	No load applied		0		V
		X_{COUT} Low Power	No load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5 V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0 V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0 V	30	50	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM Standby Voltage	In stop mode		2.0			V

NOTE:

1. Ports P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

Table 5.5 A/D Conversion Characteristics

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	V_{REF}=V_{CC}				10	Bits
INL	Integral Nonlinearity Error	V_{REF}=V_{CC}=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	V_{REF}=V_{CC}		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.6 D/A Conversion Characteristics

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTE:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

VCC=5V

Timing Requirements

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

Table 5.15 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 5.16 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.17 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.18 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Pulse Width	125		ns

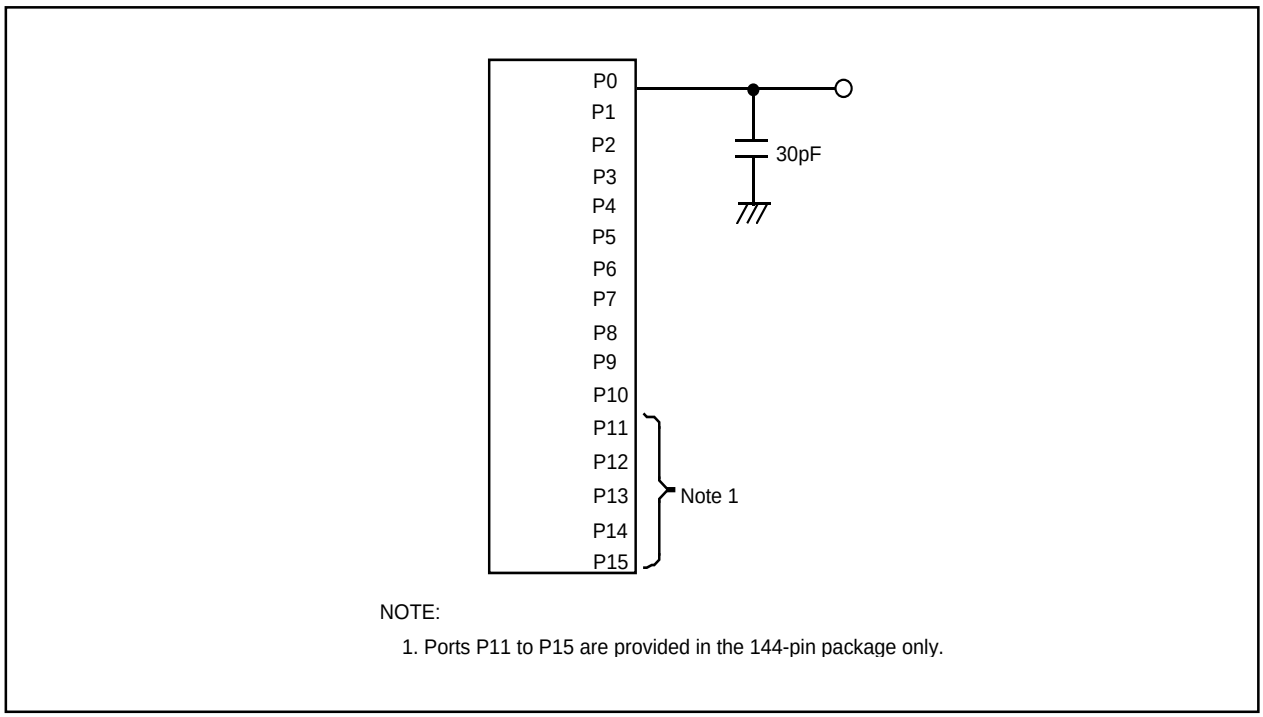
Table 5.19 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.20 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

Vcc=5V

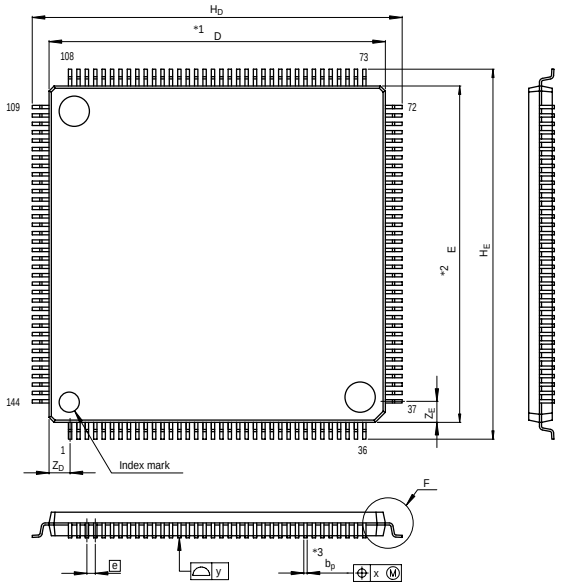


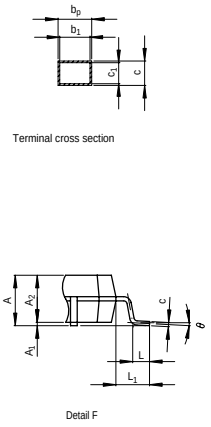
NOTE:
1. Ports P11 to P15 are provided in the 144-pin package only.

Figure 5.2 P0 to P15 Measurement Circuit

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g

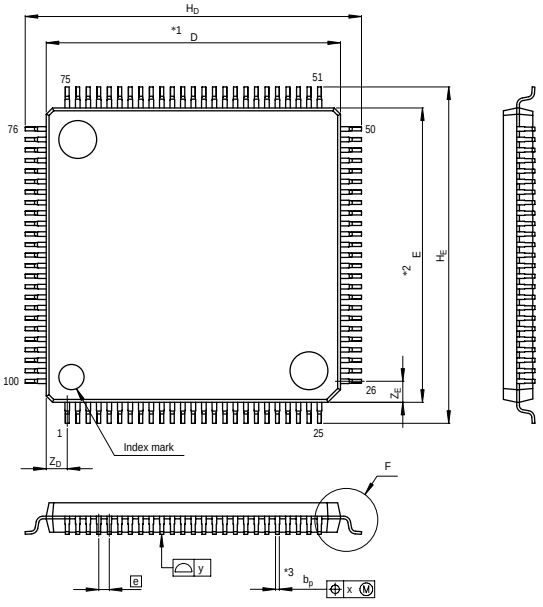


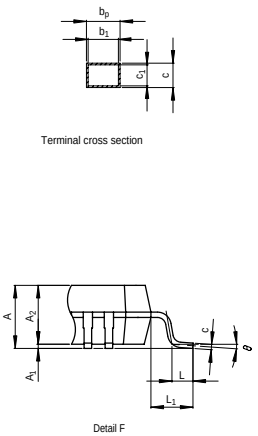


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

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http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon .3.0