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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f16ka302-e-ml

PIC24FV32KA304 FAMILY

NOTES:

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2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 μF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF .

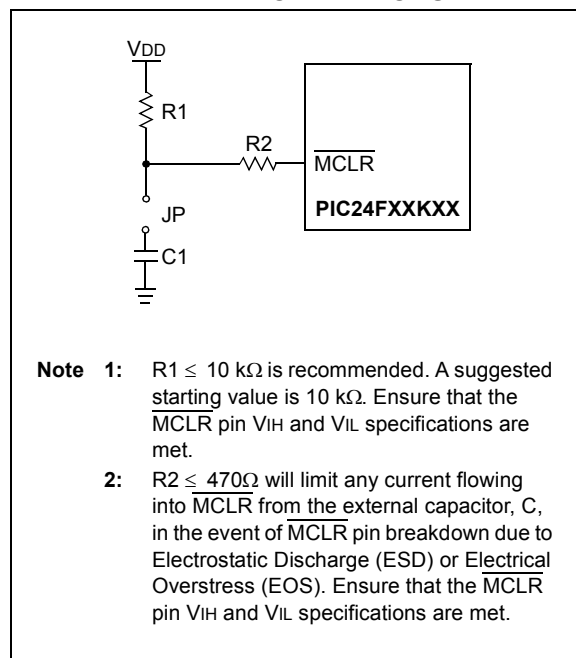
2.3 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the MCLR pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS



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8.3 Interrupt Control and Status Registers

The PIC24FV32KA304 family of devices implements a total of 23 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFS0, IFS1, IFS3 and IFS4
- IEC0, IEC1, IEC3 and IEC4
- IPC0 through IPC5, IPC7 and IPC15 through IPC19
- INTTREG

Global Interrupt Enable (GIE) control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the AIVT.

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals, or external signal, and is cleared via software.

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<6:0>) and the Interrupt Level (ILR<3:0>) bit fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence listed in Table 8-2. For example, the INT0 (External Interrupt 0) is depicted as having a vector number and a natural order priority of 0. The INT0IF status bit is found in IFS0<0>, the INT0IE enable bit in IEC0<0> and the INT0IP<2:0> priority bits are in the first position of IPC0 (IPC0<2:0>).

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. The ALU STATUS Register (SR) contains the IPL<2:0> bits (SR<7:5>). These indicate the current CPU Interrupt Priority Level. The user may change the current CPU Interrupt Priority Level by writing to the IPLx bits.

The CORCON register contains the IPL3 bit, which together with IPL<2:0>, also indicates the current CPU Interrupt Priority Level. IPL3 is a read-only bit so that the trap events cannot be masked by the user's software.

All Interrupt registers are described in Register 8-1 through Register 8-33, in the following sections.

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9.3 Control Registers

The operation of the oscillator is controlled by three Special Function Registers (SFRs):

- OSCCON
- CLKDIV
- OSCTUN

The OSCCON register (Register 9-1) is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources.

The Clock Divider register (Register 9-2) controls the features associated with Doze mode, as well as the postscaler for the FRC oscillator.

The FRC Oscillator Tune register (Register 9-3) allows the user to fine tune the FRC oscillator over a range of approximately $\pm 5.25\%$. Each bit increment or decrement changes the factory calibrated frequency of the FRC oscillator by a fixed amount.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R-0, HSC	R-0, HSC	R-0, HSC	U-0	R/W-x ⁽¹⁾	R/W-x ⁽¹⁾	R/W-x ⁽¹⁾
—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0
bit 15							bit 8
R/SO-0, HSC	U-0	R-0, HSC ⁽²⁾	U-0	R/CO-0, HS	R/W-0 ⁽³⁾	R/W-0	R/W-0
CLKLOCK	—	LOCK	—	CF	SOSCDRV	SOSCEN	OSWEN
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
HS = Hardware Settable bit	CO = Clearable Only bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits

- 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = 8 MHz FRC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits⁽¹⁾

- 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = 8 MHz FRC Oscillator (FRC)

Note 1: Reset values for these bits are determined by the FNOSC_x Configuration bits.

2: This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

3: When SOSC is selected to run from a digital clock input, rather than an external crystal (SOSC_{SRC} = 0), this bit has no effect.

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REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

- bit 7 **CLKLOCK**: Clock Selection Lock Enabled bit
 If FSCM is enabled (FCKSM1 = 1):
 1 = Clock and PLL selections are locked
 0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
 If FSCM is disabled (FCKSM1 = 0):
 Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.
- bit 6 **Unimplemented**: Read as '0'
- bit 5 **LOCK**: PLL Lock Status bit⁽²⁾
 1 = PLL module is in lock or PLL module start-up timer is satisfied
 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled
- bit 4 **Unimplemented**: Read as '0'
- bit 3 **CF**: Clock Fail Detect bit
 1 = FSCM has detected a clock failure
 0 = No clock failure has been detected
- bit 2 **SOSCDRV**: Secondary Oscillator Drive Strength bit⁽³⁾
 1 = High-power SOSC circuit is selected
 0 = Low/high-power select is done via the SOSCSRC Configuration bit
- bit 1 **SOSCEN**: 32 kHz Secondary Oscillator (SOSC) Enable bit
 1 = Enables the secondary oscillator
 0 = Disables the secondary oscillator
- bit 0 **OSWEN**: Oscillator Switch Enable bit
 1 = Initiates an oscillator switch to the clock source specified by the NOSC<2:0> bits
 0 = Oscillator switch is complete

- Note 1:** Reset values for these bits are determined by the FNOSC_x Configuration bits.
- 2:** This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.
- 3:** When SOSC is selected to run from a digital clock input, rather than an external crystal (SOSCSRC = 0), this bit has no effect.

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10.5 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default.

It is also possible to use Doze mode to selectively reduce power consumption in event driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption. Meanwhile, the CPU Idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

10.6 Selective Peripheral Module Control

Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume power. There may be cases where the application needs what these modes do not provide: the allocation of power resources to CPU processing, with minimal power consumption from the peripherals.

PIC24F devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- The Peripheral Enable bit, generically named, “XXXEN”, located in the module’s main control SFR.
- The Peripheral Module Disable (PMD) bit, generically named, “XXXMD”, located in one of the PMD Control registers.

Both bits have similar functions in enabling or disabling its associated module. Setting the PMDx bits for a module disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect, and read values will be invalid. Many peripheral modules have a corresponding PMDx bit.

In contrast, disabling a module by clearing its XXXEN bit, disables its functionality, but leaves its registers available to be read and written to. Power consumption is reduced, but not by as much as the PMDx bits are used. Most peripheral modules have an enable bit; exceptions include capture, compare and RTCC.

To achieve more selective power savings, peripheral modules can also be selectively disabled when the device enters Idle mode. This is done through the control bit of the generic name format, “XXXIDL”. By default, all modules that can operate during Idle mode will do so. Using the disable on Idle feature disables the module while in Idle mode, allowing further reduction of power consumption during Idle mode, enhancing power savings for extremely critical power applications.

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15.4 Subcycle Resolution

The DCBx bits (OCxCON2<10:9>) provide for resolution better than one instruction cycle. When used, they delay the falling edge generated from a match event by a portion of an instruction cycle.

For example, setting DCB<1:0> = 10 causes the falling edge to occur halfway through the instruction cycle in which the match event occurs, instead of at the beginning. These bits cannot be used when OCM<2:0> = 001. When operating the module in PWM mode (OCM<2:0> = 110 or 111), the DCBx bits will be double-buffered.

The DCBx bits are intended for use with a clock source identical to the system clock. When an OCx module with enabled prescaler is used, the falling edge delay caused by the DCBx bits will be referenced to the system clock period, rather than the OCx module's period.

TABLE 15-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 4 MIPS (Fcy = 4 MHz)⁽¹⁾

PWM Frequency	7.6 Hz	61 Hz	122 Hz	977 Hz	3.9 kHz	31.3 kHz	125 kHz
Prescaler Ratio	8	1	1	1	1	1	1
Period Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on Fcy = Fosc/2; Doze mode and PLL are disabled.

TABLE 15-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 16 MIPS (Fcy = 16 MHz)⁽¹⁾

PWM Frequency	30.5 Hz	244 Hz	488 Hz	3.9 kHz	15.6 kHz	125 kHz	500 kHz
Prescaler Ratio	8	1	1	1	1	1	1
Period Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on Fcy = Fosc/2; Doze mode and PLL are disabled.

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18.1 UARTx Baud Rate Generator (BRG)

The UARTx module includes a dedicated 16-bit Baud Rate Generator (BRG). The UxBRG register controls the period of a free-running, 16-bit timer. Equation 18-1 provides the formula for computation of the baud rate with BRGH = 0.

EQUATION 18-1: UARTx BAUD RATE WITH BRGH = 0⁽¹⁾

$$\text{Baud Rate} = \frac{\text{FCY}}{16 \cdot (\text{UxBRG} + 1)}$$
$$\text{UxBRG} = \frac{\text{FCY}}{16 \cdot \text{Baud Rate}} - 1$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

Example 18-1 provides the calculation of the baud rate error for the following conditions:

- FCY = 4 MHz
- Desired Baud Rate = 9600

EXAMPLE 18-1: BAUD RATE ERROR CALCULATION (BRGH = 0)⁽¹⁾

$$\begin{aligned}\text{Desired Baud Rate} &= \text{FCY}/(16 (\text{UxBRG} + 1)) \\ \text{Solving for UxBRG value:} \\ \text{UxBRG} &= ((\text{FCY}/\text{Desired Baud Rate})/16) - 1 \\ \text{UxBRG} &= ((4000000/9600)/16) - 1 \\ \text{UxBRG} &= 25 \\ \text{Calculated Baud Rate} &= 4000000/(16 (25 + 1)) \\ &= 9615 \\ \text{Error} &= (\text{Calculated Baud Rate} - \text{Desired Baud Rate}) \\ &\quad \text{Desired Baud Rate} \\ &= (9615 - 9600)/9600 \\ &= 0.16\%\end{aligned}$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

The maximum baud rate (BRGH = 0) possible is FCY/16 (for UxBRG = 0) and the minimum baud rate possible is FCY/(16 * 65536).

Equation 18-2 shows the formula for computation of the baud rate with BRGH = 1.

EQUATION 18-2: UARTx BAUD RATE WITH BRGH = 1⁽¹⁾

$$\text{Baud Rate} = \frac{\text{FCY}}{4 \cdot (\text{UxBRG} + 1)}$$
$$\text{UxBRG} = \frac{\text{FCY}}{4 \cdot \text{Baud Rate}} - 1$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

The maximum baud rate (BRGH = 1) possible is FCY/4 (for UxBRG = 0) and the minimum baud rate possible is FCY/(4 * 65536).

Writing a new value to the UxBRG register causes the BRG timer to be reset (cleared). This ensures the BRG does not wait for a timer overflow before generating the new baud rate.

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19.2.6 ALRMVAL REGISTER MAPPINGS

REGISTER 19-8: ALMTHDY: ALARM MONTH AND DAY VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							
							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							
							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of '0' or '1'.
- bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.
- bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 19-9: ALWDHR: ALARM WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							
							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							
							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.
- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

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REGISTER 22-10: AD1CTMUENH: A/D CTMU ENABLE REGISTER (HIGH WORD)⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CTMEN17	CTMEN16
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'.

bit 1-0 **CTMEN<17:16>:** CTMU Enabled During Conversion bits

1 = CTMU is enabled and connected to the selected channel during conversion

0 = CTMU is not connected to this channel

Note 1: Unimplemented channels are read as '0'.

REGISTER 22-11: AD1CTMUENL: A/D CTMU ENABLE REGISTER (LOW WORD)⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN15	CTMEN14	CTMEN13	CTMEN12	CTMUEN11	CTMEN10	CTMEN9	CTMEN8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN7	CTMEN6	CTMEN5	CTMEN4	CTMEN3	CTMEN2	CTMEN1	CTMEN0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CTMEN<15:0>:** CTMU Enabled During Conversion bits

1 = CTMU is enabled and connected to the selected channel during conversion

0 = CTMU is not connected to this channel

Note 1: Unimplemented channels are read as '0'.

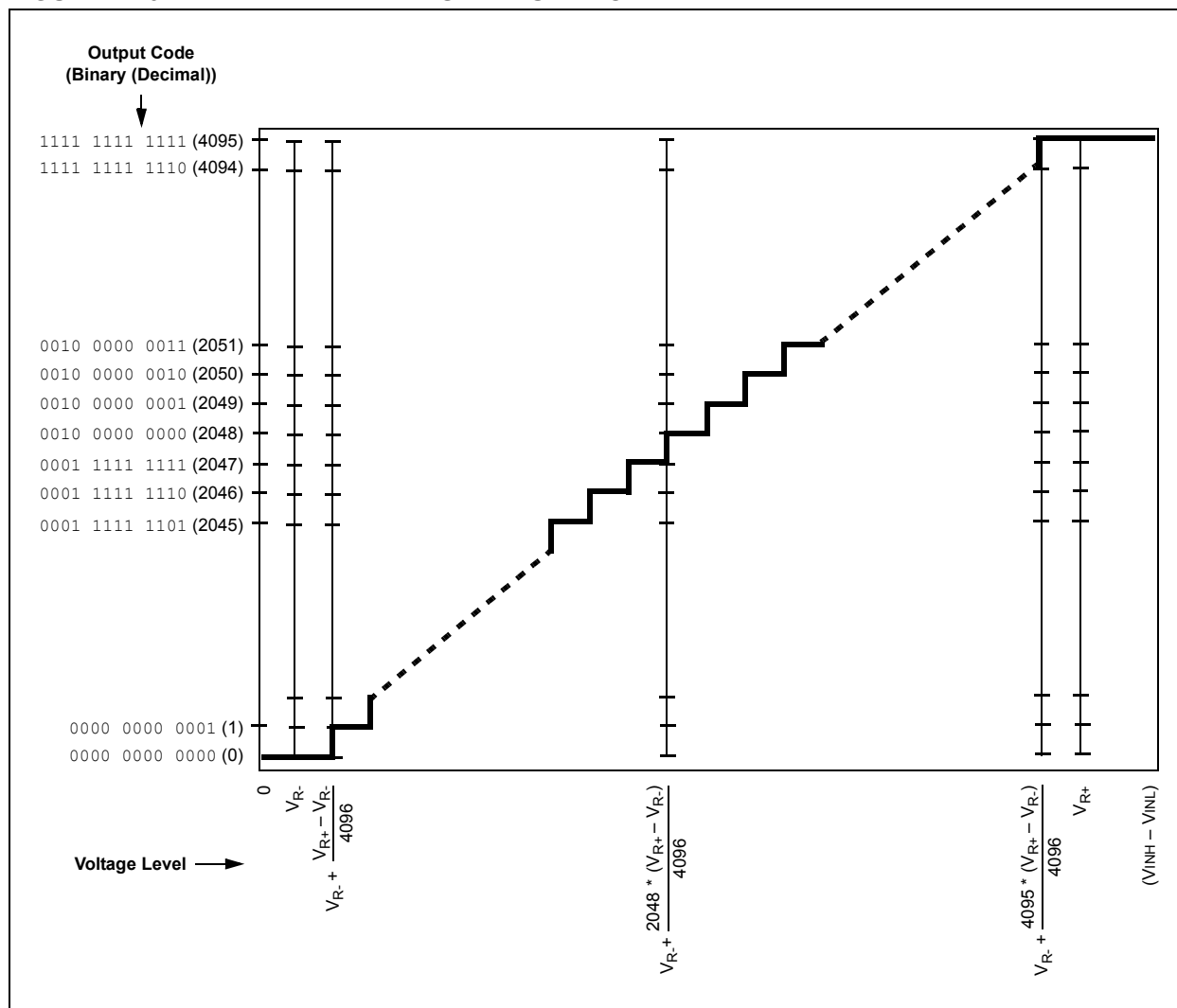
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22.3 Transfer Function

The transfer functions of the A/D Converter in 12-bit resolution are shown in Figure 22-3. The difference of the input voltages, ($V_{INH} - V_{INL}$), is compared to the reference, $((V_{R+}) - (V_{R-}))$.

- The first code transition occurs when the input voltage is $((V_{R+}) - (V_{R-}))/4096$ or 1.0 LSB.
- The 0000 0000 0001 code is centered at $V_{R-} + (1.5 * ((V_{R+}) - (V_{R-}))/4096)$.
- The '0010 0000 0000' code is centered at $V_{REFL} + (2048.5 * ((V_{R+}) - (V_{R-}))/4096)$.
- An input voltage less than $V_{R-} + (((V_{R-}) - (V_{R-}))/4096)$ converts as '0000 0000 0000'.
- An input voltage greater than $(V_{R-}) + (4095 * ((V_{R+}) - (V_{R-}))/4096)$ converts as '1111 1111 1111'.

FIGURE 22-3: 12-BIT A/D TRANSFER FUNCTION



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25.3 Pulse Generation and Delay

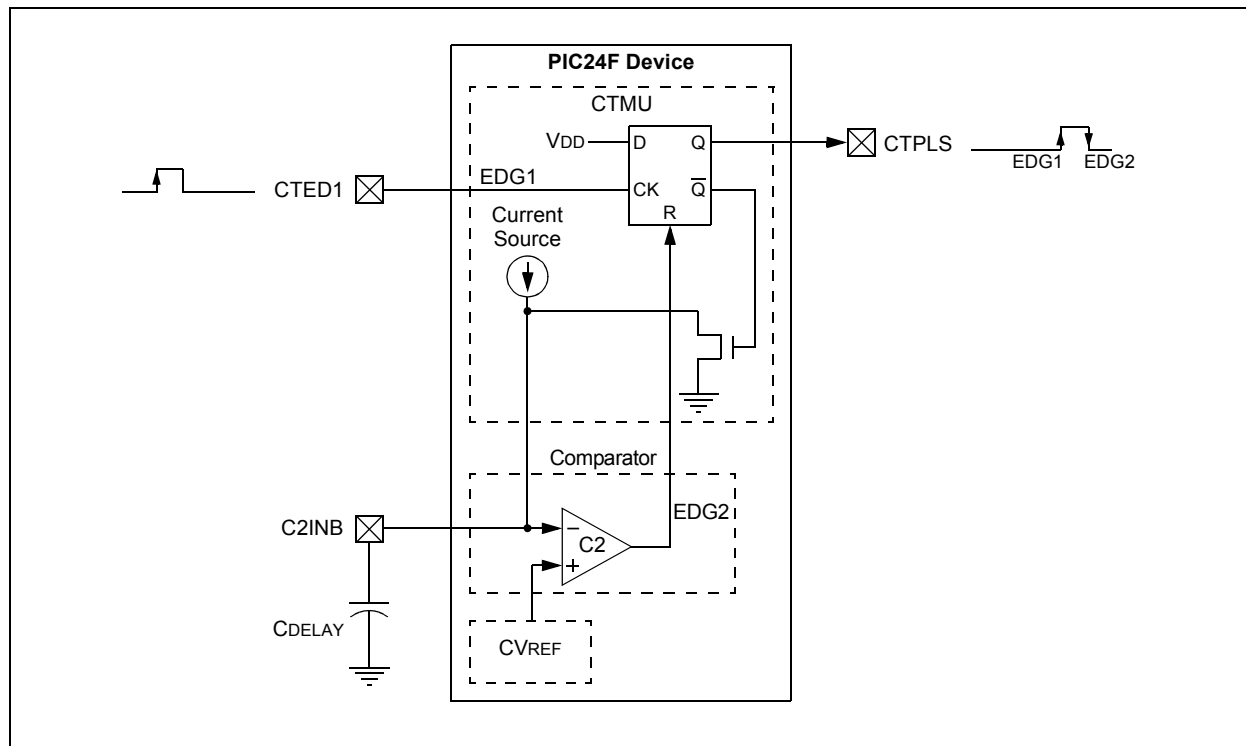
The CTMU module can also generate an output pulse with edges that are not synchronous with the device's system clock. More specifically, it can generate a pulse with a programmable delay from an edge event input to the module.

When the module is configured for pulse generation delay by setting the TGEN bit (CTMUCON<12>), the internal current source is connected to the B input of Comparator 2. A capacitor (CDELAY) is connected to the Comparator 2 pin, C2INB, and the Comparator Voltage Reference, CVREF, is connected to C2INA. CVREF is then configured for a specific trip point. The module begins to charge CDELAY when an edge event is detected. While CVREF is greater than the voltage on CDELAY, CTPLS is high. When the voltage on CDELAY equals CVREF, CTPLS goes low. With Comparator 2 configured as the second edge, this stops the CTMU from charging. In this state event, the CTMU automatically connects to ground. The IDISSEN bit doesn't need to be set and cleared before the next CTPLS cycle.

When the voltage on CDELAY equals CVREF, CTPLS goes low. With Comparator 2 configured as the second edge, this stops the CTMU from charging. In this state event, the CTMU automatically connects to ground. The IDISSEN bit doesn't need to be set and cleared before the next CTPLS cycle.

Figure 25-3 illustrates the external connections for pulse generation, as well as the relationship of the different analog modules required. While CTED1 is shown as the input pulse source, other options are available. A detailed discussion on pulse generation with the CTMU module is provided in the "PIC24F Family Reference Manual".

FIGURE 25-3: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR PULSE DELAY GENERATION



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TABLE 29-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Operating Junction Temperature Range	T _J	-40	—	+140	°C
Operating Ambient Temperature Range	T _A	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$	P _D	P _{INT} + P _{I/O}			W
Maximum Allowed Power Dissipation	P _D MAX	(T _J – T _A)/θ _{JA}			W

TABLE 29-2: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 20-Pin SPDIP	θ _{JA}	62.4	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θ _{JA}	60	—	°C/W	1
Package Thermal Resistance, 20-Pin SSOP	θ _{JA}	108	—	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θ _{JA}	71	—	°C/W	1
Package Thermal Resistance, 20-Pin SOIC	θ _{JA}	75	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ _{JA}	80.2	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN	θ _{JA}	32	—	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θ _{JA}	29	—	°C/W	1
Package Thermal Resistance, 48-Pin UQFN	θ _{JA}	—	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

TABLE 29-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX				
			Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial -40°C ≤ T _A ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DC10	V _{DD}	Supply Voltage	1.8	—	3.6	V	For F devices
			2.0	—	5.5	V	For FV devices
DC12	V _{DR}	RAM Data Retention Voltage⁽²⁾	1.5	—	—	V	For F devices
			1.7	—	—	V	For FV devices
DC16	V _{POR}	V_{DD} Start Voltage to Ensure Internal Power-on Reset Signal	V _{SS}	—	0.7	V	
DC17	SV _{DD}	V_{DD} Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 0.1s 0-2.5V in 60 ms

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which V_{DD} can be lowered without losing RAM data.

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TABLE 29-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX								
		Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended								
Parameter No.	Device	Typical ⁽¹⁾	Max	Units	Conditions					
Power-Down Current (IPD)										
DC60	PIC24FV32KA3XX	6.0	—	μA	-40°C	2.0V	Sleep Mode ⁽²⁾			
			8.0		+25°C					
			8.5		+60°C					
			9.0		+85°C					
		—	15		+125°C					
		6.0	—	μA	-40°C	5.0V				
			8.0		+25°C					
			9.0		+60°C					
			10.0		+85°C					
		—	15		+125°C					
			PIC24F32KA3XX	0.025	—	μA		-40°C	1.8V	
					0.80			+25°C		
					1.5			+60°C		
					2.0			+85°C		
—	7.5				+125°C					
0.040	—			μA	-40°C	3.3V				
	1.0				+25°C					
	2.0				+60°C					
	3.0				+85°C					
—	7.5				+125°C					
DC61	PIC24FV32KA3XX			0.25	—	μA		-40°C	2.0V	Low-Voltage Sleep Mode ⁽²⁾
				0.35	3.0	μA		+85°C	5.0V	
				—	7.5	μA		+125°C	5.0V	
DC70	PIC24FV32KA3XX			0.03	—	μA		-40°C	2.0V	Deep Sleep Mode
		0.10	2.0	μA	+85°C	5.0V				
		—	6.0	μA	+125°C	5.0V				
	PIC24F32KA3XX	0.02	—	μA	-40°C	1.8V				
		0.08	1.2	μA	+85°C	3.3V				
		—	1.2	μA	+125°C	3.3V				

Legend: Unshaded rows represent PIC24F32KA3XX devices and shaded rows represent PIC24FV32KA3XX devices.

Note 1: Data in the Typical column is at 3.3V, +25°C (PIC24F32KA3XX) or 5.0V, +25°C (PIC24FV32KA3XX) unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low, PMSLP is set to '0' and WDT, etc., are all switched off.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

4: This current applies to Sleep only.

5: This current applies to Sleep and Deep Sleep.

6: This current applies to Deep Sleep only.

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TABLE 29-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX					
		Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Parameter No.	Device	Typical ⁽¹⁾	Max	Units	Conditions		
Module Differential Current (ΔIPD) ⁽³⁾							
DC71	PIC24FV32KA3XX	0.50	—	μA	-40°C	2.0V	Watchdog Timer Current: ΔIWDT ⁽⁴⁾
		0.70	1.5	μA	+85°C	5.0V	
		—	1.5	μA	+125°C	5.0V	
	PIC24F32KA3XX	0.50	—	μA	-40°C	1.8V	
		0.70	1.5	μA	+85°C	3.3V	
		—	1.5	μA	+125°C	3.3V	
DC72	PIC24FV32KA3XX	0.80	—	μA	-40°C	2.0V	32 kHz Crystal with RTCC, DSWDT or Timer1: ΔISOSC (SOSCSEL = 0) ⁽⁵⁾
		1.50	2.0	μA	+85°C	5.0V	
		—	2.0	μA	+125°C	5.0V	
	PIC24F32KA3XX	0.70	—	μA	-40°C	1.8V	
		1.0	1.5	μA	+85°C	3.3V	
		—	1.5	μA	+125°C	3.3V	
DC75	PIC24FV32KA3XX	5.4	—	μA	-40°C	2.0V	ΔIHLVD ⁽⁴⁾
		8.1	14.0	μA	+85°C	5.0V	
		—	14.0	μA	+125°C	5.0V	
	PIC24F32KA3XX	4.9	—	μA	-40°C	1.8V	
		7.5	14.0	μA	+85°C	3.3V	
		—	14.0	μA	+125°C	3.3V	
DC76	PIC24FV32KA3XX	5.6	—	μA	-40°C	2.0V	ΔIBOR ⁽⁴⁾
		6.5	11.2	μA	-40°C	5.0V	
		—	11.2	μA	+125°C	5.0V	
	PIC24F32KA3XX	5.6	—	μA	-40°C	1.8V	
		6.0	11.2	μA	+85°C	3.3V	
		—	11.2	μA	+125°C	3.3V	

Legend: Unshaded rows represent PIC24F32KA3XX devices and shaded rows represent PIC24FV32KA3XX devices.

- Note 1:** Data in the Typical column is at 3.3V, +25°C (PIC24F32KA3XX) or 5.0V, +25°C (PIC24FV32KA3XX) unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** Base I_{PD} is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low, PMSLP is set to '0' and WDT, etc., are all switched off.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.
- 4:** This current applies to Sleep only.
- 5:** This current applies to Sleep and Deep Sleep.
- 6:** This current applies to Deep Sleep only.

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FIGURE 29-7: BROWN-OUT RESET CHARACTERISTICS

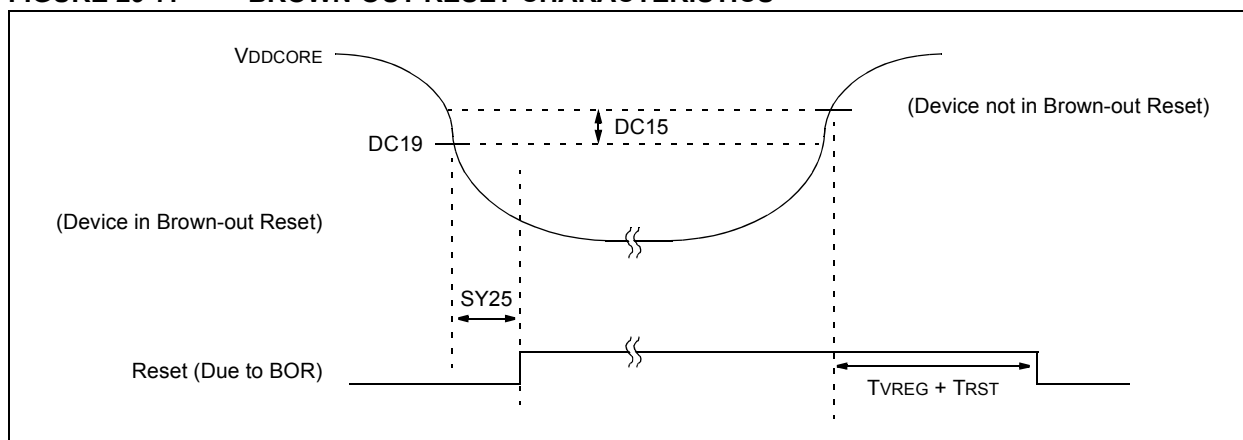


TABLE 29-26: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX				
			Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
SY10	TmCL	MCLR Pulse Width (low)	2	—	—	μs	
SY11	TPWRT	Power-up Timer Period	50	64	90	ms	
SY12	TPOR	Power-on Reset Delay	1	5	10	μs	
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	—	100	ns	
SY20	TWDT	Watchdog Timer Time-out Period	0.85	1.0	1.15	ms	1.32 prescaler
			3.4	4.0	4.6	ms	1:128 prescaler
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	μs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	2.0	2.3	μs	
SY45	TRST	Internal State Reset Time	—	5	—	μs	
SY50	TVREG	On-Chip Voltage Regulator Output Delay	—	10	—	μs	(Note 2)
SY55	TLOCK	PLL Start-up Time	—	100	—	μs	
SY65	TOST	Oscillator Start-up Time	—	1024	—	TOSC	
SY70	TDSWU	Wake-up from Deep Sleep Time	—	100	—	μs	Based on full discharge of 10 μF capacitor on VCAP; includes TPOR and TRST
SY71	TPM	Program Memory Wake-up Time	—	1	—	μs	Sleep wake-up with PMSLP = 0
SY72	TLVR	Retention Regulator Wake-up Time	—	250	—	μs	
SY73	THVLD	HVLD Interrupt Response Time	—	2	—	μs	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: This applies to PIC24FV32KA3XX devices only.

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FIGURE 30-44: TYPICAL AND MAXIMUM I_{PD} vs. V_{DD} (DEEP SLEEP MODE)

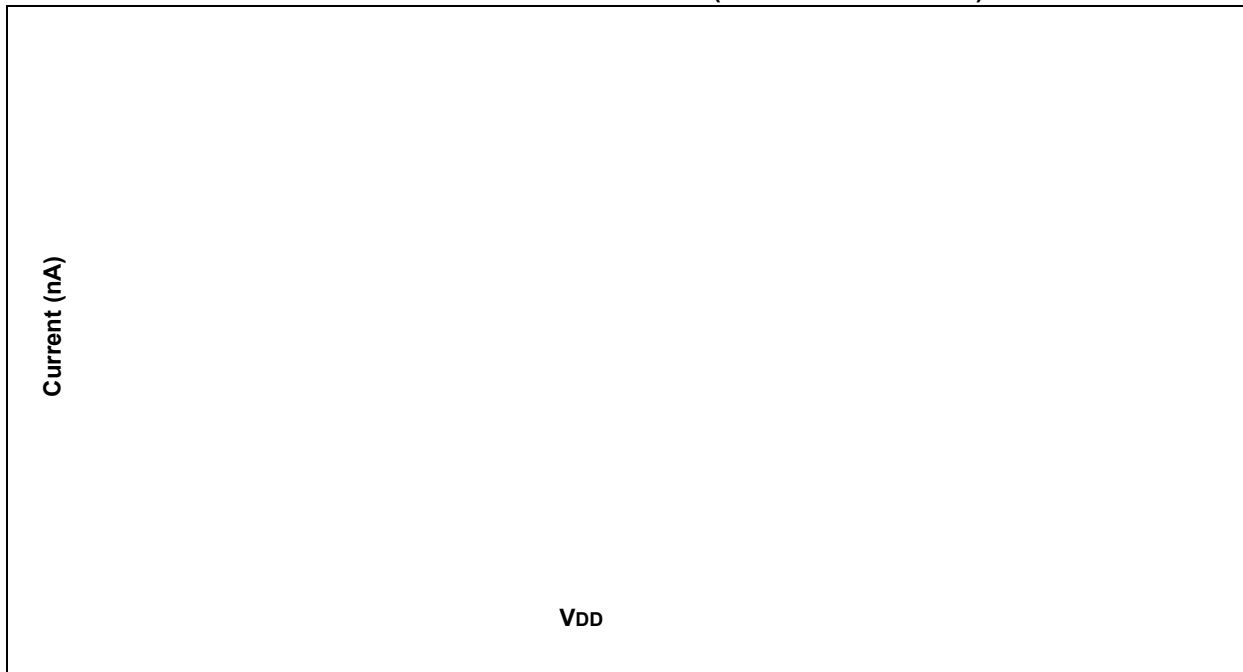
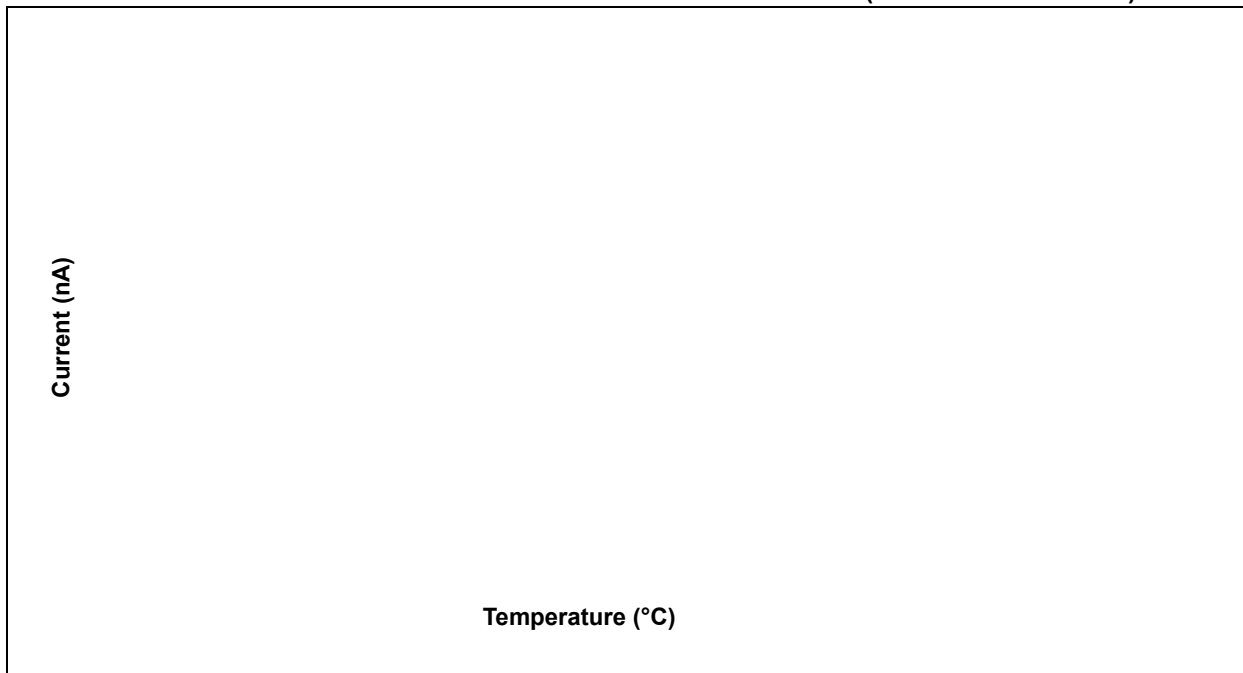


FIGURE 30-45: TYPICAL AND MAXIMUM I_{PD} vs. TEMPERATURE (DEEP SLEEP MODE)



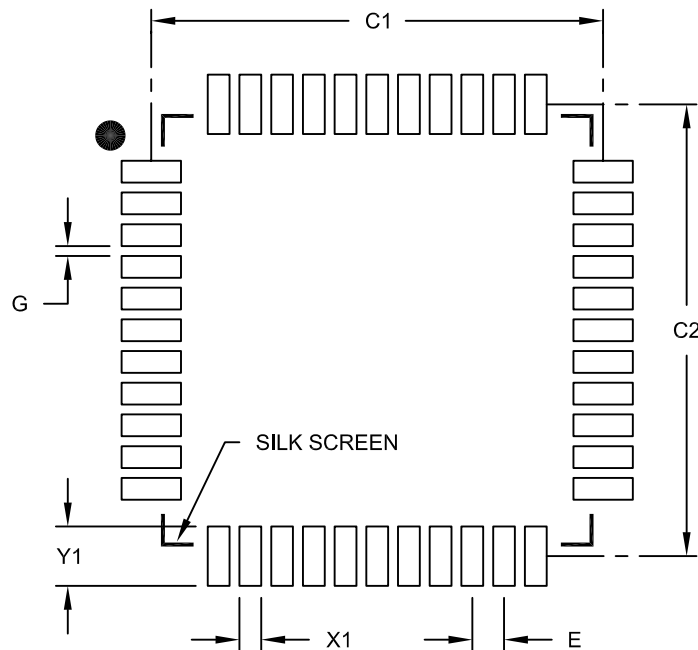
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NOTES:

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44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B