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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f16ka304-i-mv

TABLE 4-24: NVM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets ⁽¹⁾
NVMCON	0760	WR	WREN	WRERR	PGMONLY	—	—	—	—	—	ERASE	NVMOP5	NVMOP4	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000
NVMKEY	0766	—	—	—	—	—	—	—	—	NVMKEY								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset value shown is for POR only. The value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

TABLE 4-25: ULTRA LOW-POWER WAKE-UP REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ULPWCON	0768	ULPEN	—	ULPSIDL	—	—	—	—	ULPSINK	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PMD REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	ADC1MD	0000
PMD2	0772	—	—	—	—	—	IC3MD	IC2MD	IC1MD	—	—	—	—	—	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	RTCCMD	—	CRCPMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	ULPWUMD	—	—	EEMD	REFOMD	CTMUMD	HLVDMD	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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6.4.1 ERASE DATA EEPROM

The data EEPROM can be fully erased, or can be partially erased, at three different sizes: one word, four words or eight words. The bits, NVMOP<1:0> (NVMCON<1:0>), decide the number of words to be erased. To erase partially from the data EEPROM, the following sequence must be followed:

1. Configure NVMCON to erase the required number of words: one, four or eight.
2. Load TBLPAG and WREG with the EEPROM address to be erased.
3. Clear the NVMIF status bit and enable the NVM interrupt (optional).
4. Write the key sequence to NVMKEY.
5. Set the WR bit to begin the erase cycle.
6. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical erase sequence is provided in Example 6-2. This example shows how to do a one-word erase. Similarly, a four-word erase and an eight-word erase can be done. This example uses C library procedures to manage the Table Pointer (`builtin_tblpage` and `builtin_tbloffset`) and the Erase Page Pointer (`builtin_tblwtl`). The memory unlock sequence (`builtin_write_NVM`) also sets the WR bit to initiate the operation and returns control when complete.

EXAMPLE 6-2: SINGLE-WORD ERASE

```
int __attribute__((space(eedata))) eeData = 0x1234;
/*-----
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the erase
-----*/
unsigned int offset;

// Set up NVMCON to erase one word of data EEPROM
NVMCON = 0x4058;

// Set up a pointer to the EEPROM location to be erased
TBLPAG = __builtin_tblpage(&eeData);           // Initialize EE Data page pointer
offset = __builtin_tbloffset(&eeData);          // Initizlize lower word of address
__builtin_tblwtl(offset, 0);                    // Write EEPROM data to write latch

asm volatile ("disi #5");                       // Disable Interrupts For 5 Instructions
__builtin_write_NVM();                          // Issue Unlock Sequence & Start Write Cycle
while (NVMCONbits.WR=1);                       // Optional: Poll WR bit to wait for
                                              // write sequence to complete
```

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7.5.2 DETECTING BOR

When BOR is enabled, the BOR bit (RCON<1>) is always reset to '1' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR and BOR bits are reset to '0' in the software immediately after any POR event. If the BOR bit is '1' while POR is '0', it can be reliably assumed that a BOR event has occurred.

Note: Even when the device exits from Deep Sleep mode, both the POR and BOR bits are set.
--

7.5.3 DISABLING BOR IN SLEEP MODE

When BOREN<1:0> = 10, BOR remains under hardware control and operates as previously described. However, whenever the device enters Sleep mode, BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

Note: BOR levels differ depending on device type; PIC24FV32KA3XX devices are at different levels than those of PIC24F32KA3XX devices. See Section 29.0 “Electrical Characteristics” for BOR voltage levels.

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8.3 Interrupt Control and Status Registers

The PIC24FV32KA304 family of devices implements a total of 23 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFS0, IFS1, IFS3 and IFS4
- IEC0, IEC1, IEC3 and IEC4
- IPC0 through IPC5, IPC7 and IPC15 through IPC19
- INTTREG

Global Interrupt Enable (GIE) control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the AIVT.

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals, or external signal, and is cleared via software.

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<6:0>) and the Interrupt Level (ILR<3:0>) bit fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence listed in Table 8-2. For example, the INTO (External Interrupt 0) is depicted as having a vector number and a natural order priority of 0. The INTOIF status bit is found in IFS0<0>, the INTOIE enable bit in IEC0<0> and the INTOIP<2:0> priority bits are in the first position of IPC0 (IPC0<2:0>).

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. The ALU STATUS Register (SR) contains the IPL<2:0> bits (SR<7:5>). These indicate the current CPU Interrupt Priority Level. The user may change the current CPU Interrupt Priority Level by writing to the IPLx bits.

The CORCON register contains the IPL3 bit, which together with IPL<2:0>, also indicates the current CPU Interrupt Priority Level. IPL3 is a read-only bit so that the trap events cannot be masked by the user's software.

All Interrupt registers are described in Register 8-1 through Register 8-33, in the following sections.

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REGISTER 8-16: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ULPWUIE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1

Unimplemented: Read as '0'

bit 0

ULPWUIE: Ultra Low-Power Wake-up Interrupt Enable Bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

9.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMDx Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the FOSC Configuration register must be programmed to '0'. (Refer to **Section 26.0 "Special Features"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and FSCM function are disabled. This is the default setting.

The NOSCx control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSCx bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSCx bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSCx bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically, as follows:

1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT, FSCM or RTCC with LPRC as a clock source is enabled) or SOSC (if SOSSEN remains enabled).

Note 1: The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

- 2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

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REGISTER 9-4: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ROEN:** Reference Oscillator Output Enable bit

1 = Reference oscillator is enabled on REFO pin

0 = Reference oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Output Stop in Sleep bit

1 = Reference oscillator continues to run in Sleep

0 = Reference oscillator is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit

1 = Primary oscillator is used as the base clock⁽¹⁾

0 = System clock is used as the base clock; base clock reflects any clock switching of the device

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divisor Select bits

1111 = Base clock value divided by 32,768

1110 = Base clock value divided by 16,384

1101 = Base clock value divided by 8,192

1100 = Base clock value divided by 4,096

1011 = Base clock value divided by 2,048

1010 = Base clock value divided by 1,024

1001 = Base clock value divided by 512

1000 = Base clock value divided by 256

0111 = Base clock value divided by 128

0110 = Base clock value divided by 64

0101 = Base clock value divided by 32

0100 = Base clock value divided by 16

0011 = Base clock value divided by 8

0010 = Base clock value divided by 4

0001 = Base clock value divided by 2

0000 = Base clock value

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The crystal oscillator must be enabled using the FOSC<2:0> bits; the crystal maintains the operation in Sleep mode.

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10.2.2 IDLE MODE

Idle mode has these features:

- The CPU will stop executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.6 “Selective Peripheral Module Control”**).
- If the WDT or FSCM is enabled, the LPRC will also remain active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle, the clock is re-applied to the CPU and instruction execution begins immediately, starting with the instruction following the `PWRSAB` instruction or the first instruction in the ISR.

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSAB` instruction will be held off until entry into Sleep or Idle mode has completed. The device will then wake-up from Sleep or Idle mode.

10.2.4 DEEP SLEEP MODE

In PIC24FV32KA304 family devices, Deep Sleep mode is intended to provide the lowest levels of power consumption available without requiring the use of external switches to completely remove all power from the device. Entry into Deep Sleep mode is completely under software control. Exit from Deep Sleep mode can be triggered from any of the following events:

- POR Event
- `MCLR` Event
- RTCC Alarm (if the RTCC is present)
- External Interrupt 0
- Deep Sleep Watchdog Timer (DSWDT) Time-out
- Ultra Low-Power Wake-up (ULPWU) Event

In Deep Sleep mode, it is possible to keep the device Real-Time Clock and Calendar (RTCC) running without the loss of clock cycles.

The device has a dedicated Deep Sleep Brown-out Reset (DSBOR) and a Deep Sleep Watchdog Timer Reset (DSWDT) for monitoring voltage and time-out events. The DSBOR and DSWDT are independent of the standard BOR and WDT used with other power-managed modes (Sleep, Idle and Doze).

10.2.4.1 Entering Deep Sleep Mode

Deep Sleep mode is entered by setting the DSEN bit in the DSCON register and then executing a Sleep command (`PWRSAB #SLEEP_MODE`). An unlock sequence is required to set the DSEN bit. Once the DSEN bit has been set, there is no time limit before the `SLEEP` command can be executed. The DSEN bit is automatically cleared when exiting the Deep Sleep mode.

Note: To re-enter Deep Sleep after a Deep Sleep wake-up, allow a delay of at least 3 T_{CY} after clearing the RELEASE bit.

The sequence to enter Deep Sleep mode is:

1. If the application requires the Deep Sleep WDT, enable it and configure its clock source. For more information on Deep Sleep WDT, see **Section 10.2.4.5 “Deep Sleep WDT”**.
2. If the application requires Deep Sleep BOR, enable it by programming the DSLPBOR Configuration bit (`FDS<6>`).
3. If the application requires wake-up from Deep Sleep on RTCC alarm, enable and configure the RTCC module. For more information on RTCC, see **Section 19.0 “Real-Time Clock and Calendar (RTCC)”**.
4. If needed, save any critical application context data by writing it to the DSGPR0 and DSGPR1 registers (optional).
5. Enable Deep Sleep mode by setting the DSEN bit (`DSCON<15>`).

Note: An unlock sequence is required to set the DSEN bit.

6. Enter Deep Sleep mode by issuing a `PWRSAB #0` instruction.

Any time the DSEN bit is set, all bits in the DSWAKE register will be automatically cleared.

To set the DSEN bit, the unlock sequence in Example 10-2 is required:

EXAMPLE 10-2: THE UNLOCK SEQUENCE

```
//Disable Interrupts For 5 instructions
asm volatile("disi #5");
//Issue Unlock Sequence
asm volatile
mov    #0x55, W0;
mov    W0, NVMKEY;
mov    #0xAA, W1;
mov    W1, NVMKEY;
bset   DSCON, #DSEN
```

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REGISTER 18-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
- bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity
- bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

Note 1: This feature is only available for the 16x BRG mode (BRGH = 0).

2: The bit availability depends on the pin availability.

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20.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, Section 41. “32-Bit Programmable Cyclic Redundancy Check (CRC)” (DS39729).

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 20-1. A simple version of the CRC shift engine is shown in Figure 20-2.

FIGURE 20-1: CRC BLOCK DIAGRAM

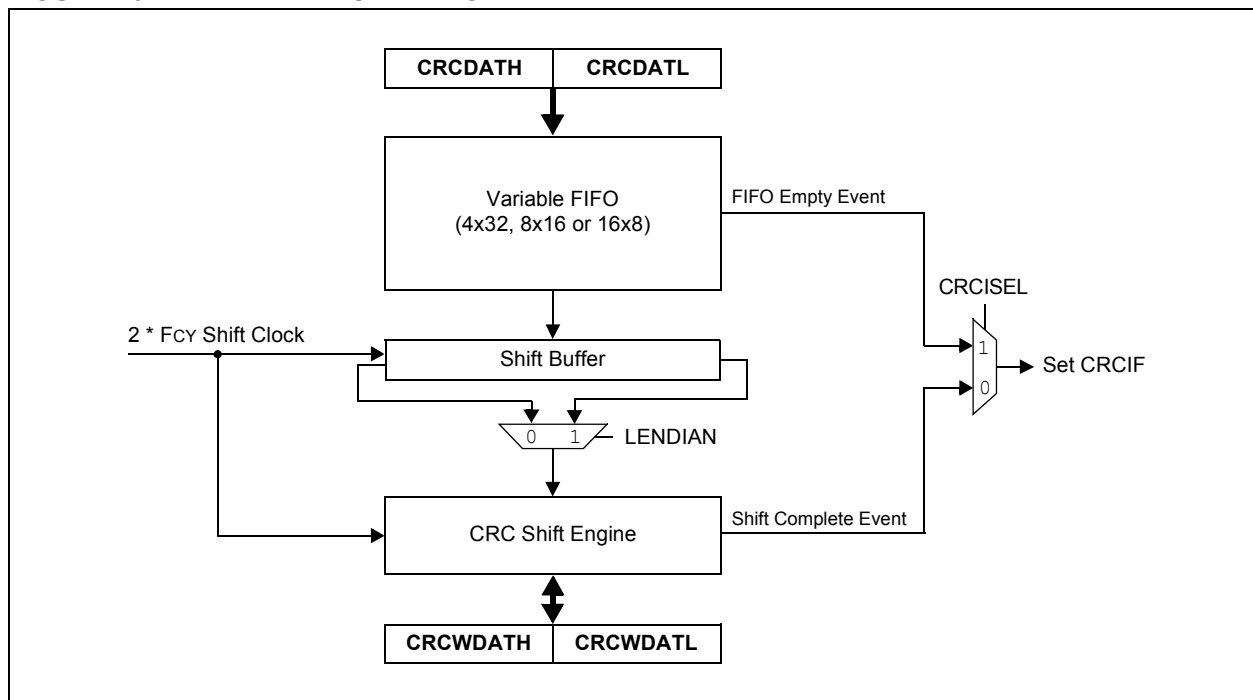
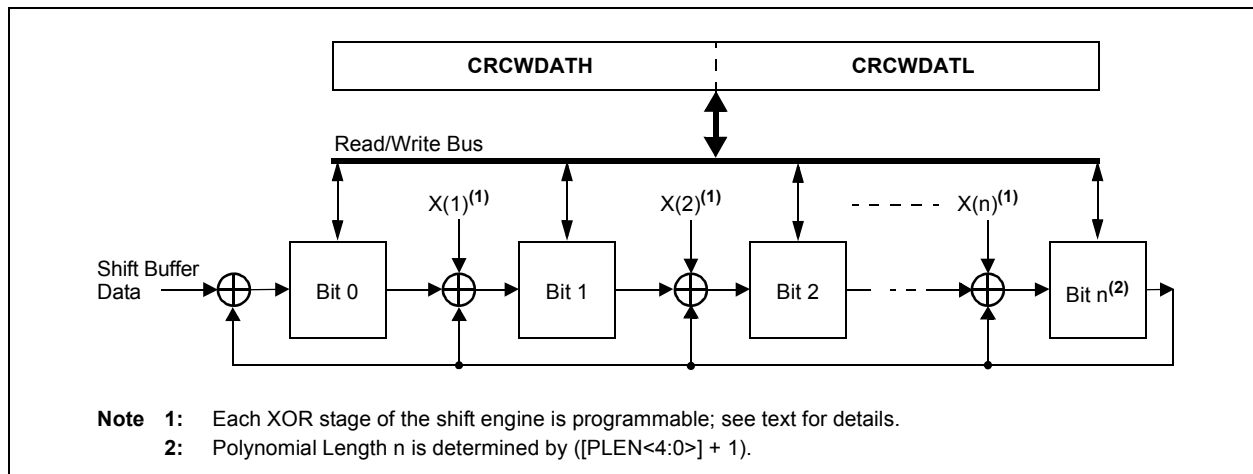


FIGURE 20-2: CRC SHIFT ENGINE DETAIL



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22.2 A/D Sampling Requirements

The analog input model of the 12-bit A/D Converter is shown in Figure 22-2. The total sampling time for the A/D is a function of the holding capacitor charge time.

For the A/D Converter to meet its specified accuracy, the Charge Holding Capacitor (CHOLD) must be allowed to fully charge to the voltage level on the analog input pin. The Source (R_s) impedance, the Interconnect (R_{ic}) impedance and the internal Sampling Switch (R_{ss}) impedance combine to directly affect the time required to charge CHOLD. The combined impedance of the analog sources must, therefore, be small enough to fully charge the holding capacitor within the chosen sample time. To minimize the effects of pin leakage currents on the accuracy of the A/D Converter, the maximum recommended Source impedance, R_s , is 2.5 k Ω . After the analog input channel is selected (changed), this

sampling function must be completed prior to starting the conversion. The internal holding capacitor will be in a discharged state prior to each sample operation.

At least 1 T_{AD} time period should be allowed between conversions for the sample time. For more details, see **Section 29.0 “Electrical Characteristics”**.

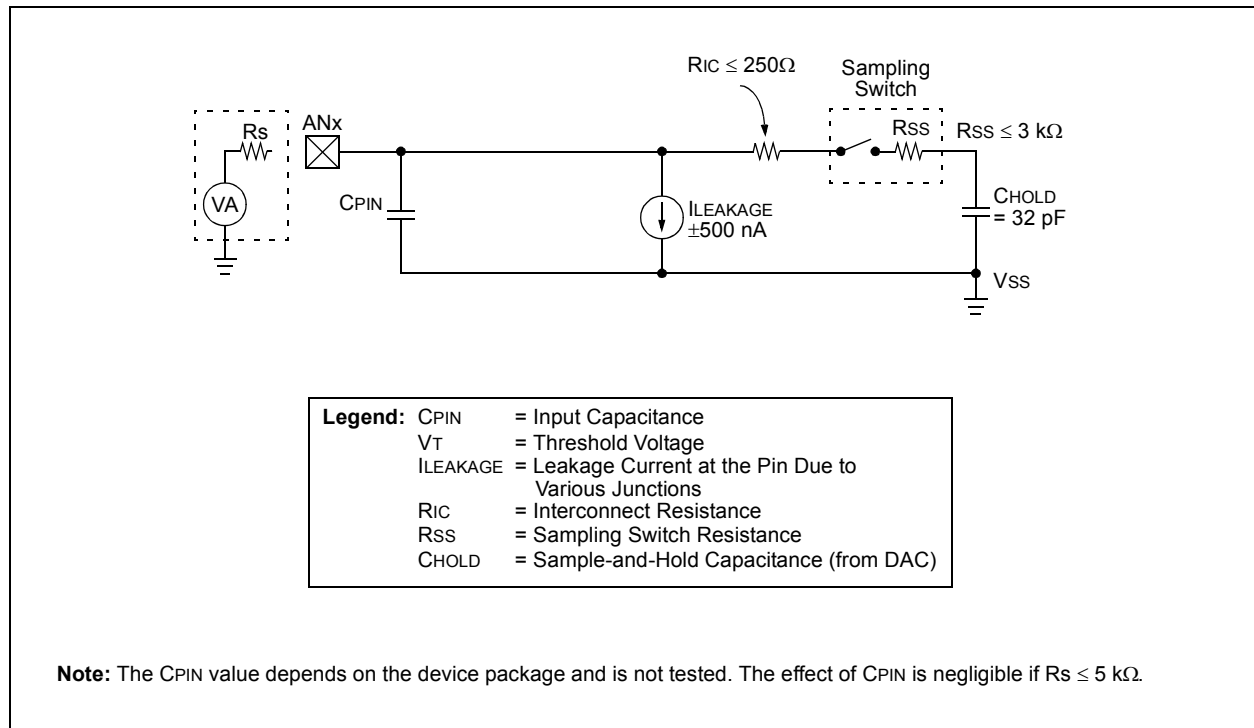
EQUATION 22-1: A/D CONVERSION CLOCK PERIOD

$$T_{AD} = T_{CY}(ADCS + 1)$$

$$ADCS = \frac{T_{AD}}{T_{CY}} - 1$$

Note: Based on $T_{CY} = 2/F_{OSC}$; Doze mode and PLL are disabled.

FIGURE 22-2: 12-BIT A/D CONVERTER ANALOG INPUT MODEL



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REGISTER 25-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CTMUEN:** CTMU Enable bit
 1 = Module is enabled
 0 = Module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **TGEN:** Time Generation Enable bit
 1 = Enables edge delay generation
 0 = Disables edge delay generation
- bit 11 **EDGEN:** Edge Enable bit
 1 = Edges are not blocked
 0 = Edges are blocked
- bit 10 **EDGSEQEN:** Edge Sequence Enable bit
 1 = Edge 1 event must occur before Edge 2 event can occur
 0 = No edge sequence is needed
- bit 9 **IDISSEN:** Analog Current Source Control bit
 1 = Analog current source output is grounded
 0 = Analog current source output is not grounded
- bit 8 **CTTRIG:** CTMU Trigger Control bit
 1 = Trigger output is enabled
 0 = Trigger output is disabled
- bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 26-10: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23				bit 16			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV3	REV2	REV1	REV0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 23-4 **Unimplemented:** Read as '0'

bit 3-0 **REV<3:0>:** Minor Revision Identifier bits

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29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC24FV32KA304 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FV32KA304 family devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings^(†)

Ambient temperature under bias	-40°C to +135°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS (PIC24FVXXKA30X)	-0.3V to +6.5V
Voltage on VDD with respect to VSS (PIC24FXXKA30X)	-0.3V to +4.5V
Voltage on any combined analog and digital pin with respect to VSS	-0.3V to (VDD + 0.3V)
Voltage on any digital only pin with respect to VSS	-0.3V to (VDD + 0.3V)
Voltage on MCLR/VPP pin with respect to VSS	-0.3V to +9.0V
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin ⁽¹⁾	250 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports ⁽¹⁾	200 mA

Note 1: Maximum allowable current is a function of the device maximum power dissipation (see Table 29-1).

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 29-4: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX								
Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended								
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0000 ⁽²⁾	—	—	1.90	V	
			HLVDL<3:0> = 0001	1.86	—	2.13	V	
			HLVDL<3:0> = 0010	2.08	—	2.35	V	
			HLVDL<3:0> = 0011	2.22	—	2.53	V	
			HLVDL<3:0> = 0100	2.30	—	2.62	V	
			HLVDL<3:0> = 0101	2.49	—	2.84	V	
			HLVDL<3:0> = 0110	2.73	—	3.10	V	
			HLVDL<3:0> = 0111	2.86	—	3.25	V	
			HLVDL<3:0> = 1000	3.00	—	3.41	V	
			HLVDL<3:0> = 1001	3.16	—	3.59	V	
			HLVDL<3:0> = 1010 ⁽¹⁾	3.33	—	3.79	V	
			HLVDL<3:0> = 1011 ⁽¹⁾	3.53	—	4.01	V	
			HLVDL<3:0> = 1100 ⁽¹⁾	3.74	—	4.26	V	
			HLVDL<3:0> = 1101 ⁽¹⁾	4.00	—	4.55	V	
			HLVDL<3:0> = 1110 ⁽¹⁾	4.28	—	4.87	V	

Note 1: These trip points should not be used on PIC24FXXKA30X devices.

Note 2: This trip point should not be used on PIC24FVXXKA30X devices.

TABLE 29-5: BOR TRIP POINTS

Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX								
Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended								
Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
DC15		BOR Hysteresis		—	5	—	mV	
DC19		BOR Voltage on VDD Transition	BORV<1:0> = 00	—	—	—	—	Valid for LPBOR and DSBOR (Note 1)
			BORV<1:0> = 01	2.90	3	3.38	V	
			BORV<1:0> = 10	2.53	2.7	3.07	V	
			BORV<1:0> = 11	1.75	1.85	2.05	V	(Note 2)
			BORV<1:0> = 11	1.95	2.05	2.16	V	(Note 3)

Note 1: LPBOR re-arms the POR circuit but does not cause a BOR.

Note 2: This is valid for PIC24F (3.3V) devices.

Note 3: This is valid for PIC24FV (5V) devices.

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TABLE 29-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: $-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ (unless otherwise stated)							
Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
DVR10	V _{BG}	Band Gap Reference Voltage	0.973	1.024	1.075	V	
DVR11	T _{BG}	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	V _{RGOUT}	Regulator Output Voltage	3.1	3.3	3.6	V	$-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$
			3.0	3.19	3.6	V	$-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$
DVR21	C _{EFC}	External Filter Capacitor Value	4.7	10	—	μF	Series resistance < 3 Ohm recommended; < 5 Ohm is required.
DVR30	V _{LVR}	Retention Regulator Output Voltage	—	2.6	—	V	

TABLE 29-16: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX					
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Comments	Conditions
DCT10	I _{OUT1}	CTMU Current Source, Base Range	—	550	—	nA	CTMUICON<9:8> = 01	2.5V < V _{DD} < V _{DDMAX}
DCT11	I _{OUT2}	CTMU Current Source, 10x Range	—	5.5	—	μA	CTMUICON<9:8> = 10	
DCT12	I _{OUT3}	CTMU Current Source, 100x Range	—	55	—	μA	CTMUICON<9:8> = 11	
DCT13	I _{OUT4}	CTMU Current Source, 1000x Range	—	550	—	μA	CTMUICON<9:8> = 00 (Note 2)	
DCT20	V _F	Temperature Diode Forward Voltage	—	.76	—	V		
DCT21	V _Δ	Voltage Change per Degree Celsius	—	1.6	—	mV/°C		

Note 1: Nominal value at the center point of the current trim range (CTMUICON<7:2> = 000000). On PIC24F32KA parts, the current output is limited to the typical current value when I_{OUT4} is chosen.

2: Do not use this current range with a temperature sensing diode.

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FIGURE 29-10: OUTPUT COMPARE x TIMINGS

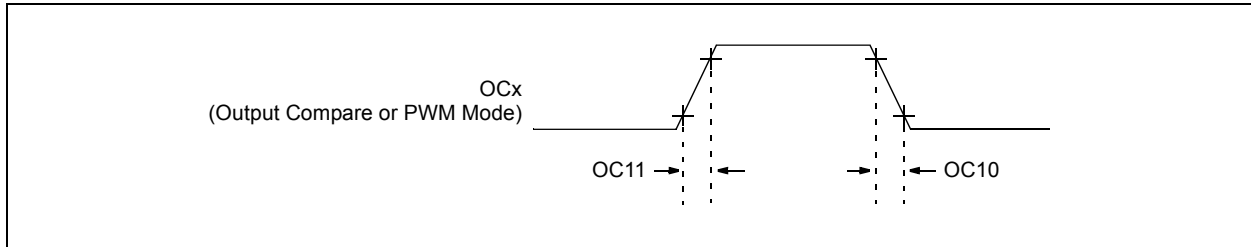


TABLE 29-29: OUTPUT CAPTURE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
OC11	TccR	OC1 Output Rise Time	—	10	ns	
			—	—	ns	
OC10	TccF	OC1 Output Fall Time	—	10	ns	
			—	—	ns	

FIGURE 29-11: PWM MODULE TIMING REQUIREMENTS

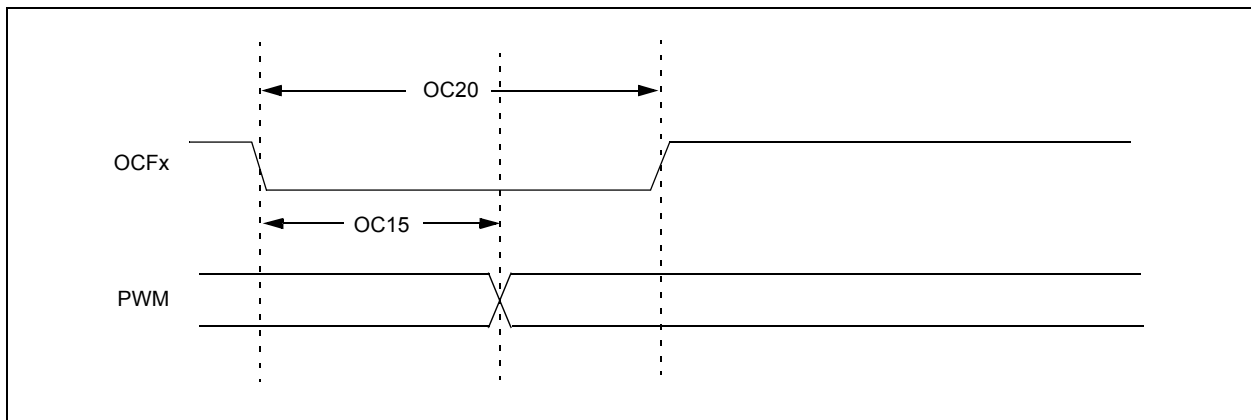


TABLE 29-30: PWM TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
OC15	TfD	Fault Input to PWM I/O Change	—	—	25	ns	VDD = 3.0V, -40°C to +125°C
OC20	TfH	Fault Input Pulse Width	50	—	—	ns	VDD = 3.0V, -40°C to +125°C

† Data in "Typ" column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 29-16: UARTx BAUD RATE GENERATOR OUTPUT TIMING

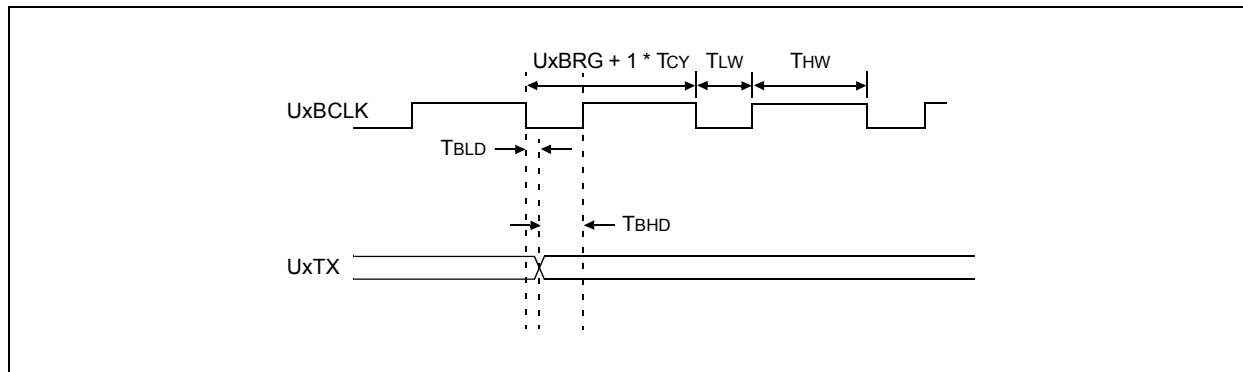


FIGURE 29-17: UARTx START BIT EDGE DETECTION

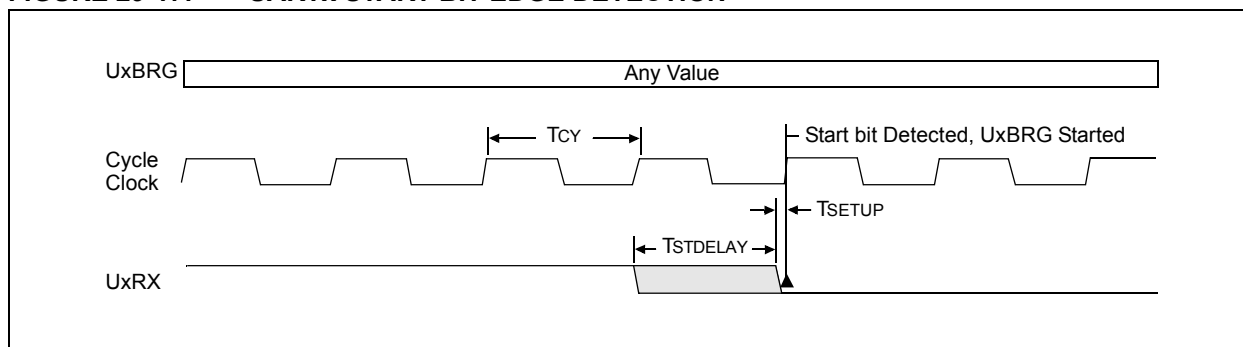


TABLE 29-35: UARTx TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (Industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (Extended)			
Symbol	Characteristics	Min	Typ	Max	Units
TLW	UxBCLK High Time	20	$T_{cy}/2$	—	ns
THW	UxBCLK Low Time	20	$(T_{cy} * UxBRG) + T_{cy}/2$	—	ns
TBLD	UxBCLK Falling Edge Delay from UxTX	-50	—	50	ns
TBHD	UxBCLK Rising Edge Delay from UxTX	$T_{cy}/2 - 50$	—	$T_{cy}/2 + 50$	ns
TWAK	Minimum Low on UxRX Line to Cause Wake-up	—	1	—	μs
TCTS	Minimum Low on \overline{UxCTS} Line to Start Transmission	T_{cy}	—	—	ns
TSETUP	Start bit Falling Edge to System Clock Rising Edge Setup Time	3	—	—	ns
TSTDELAY	Maximum Delay in the Detection of the Start bit Falling Edge	—	—	$T_{cy} + TSETUP$	ns

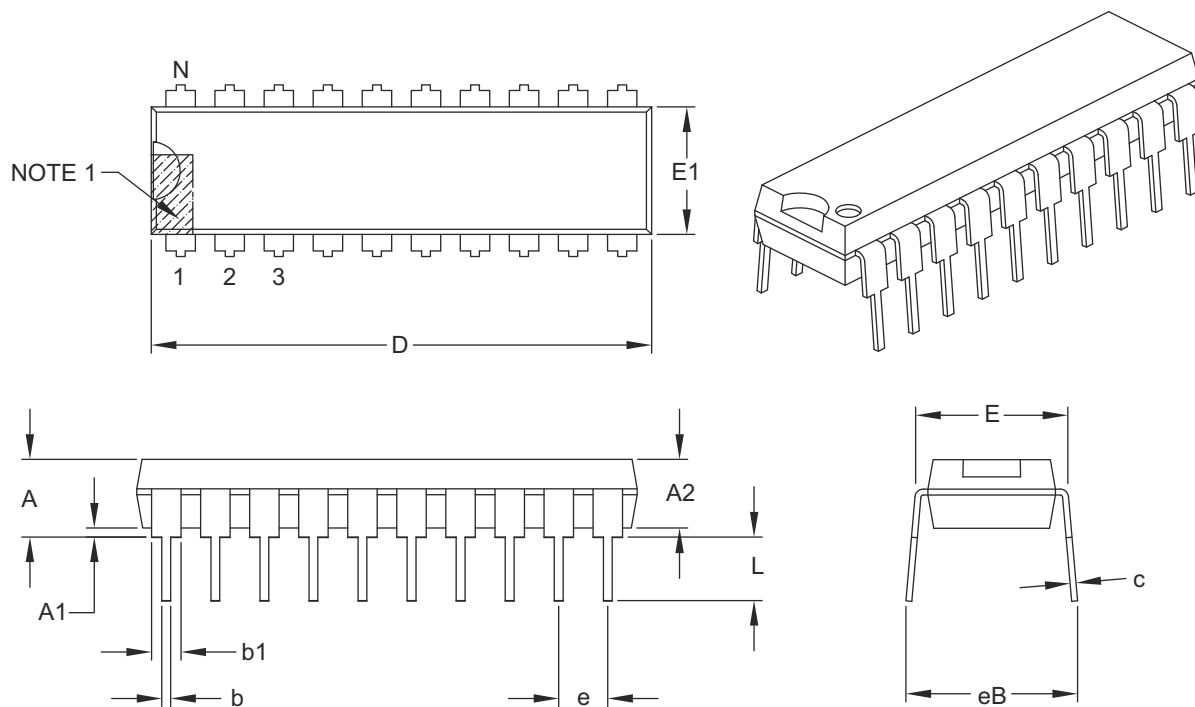
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31.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

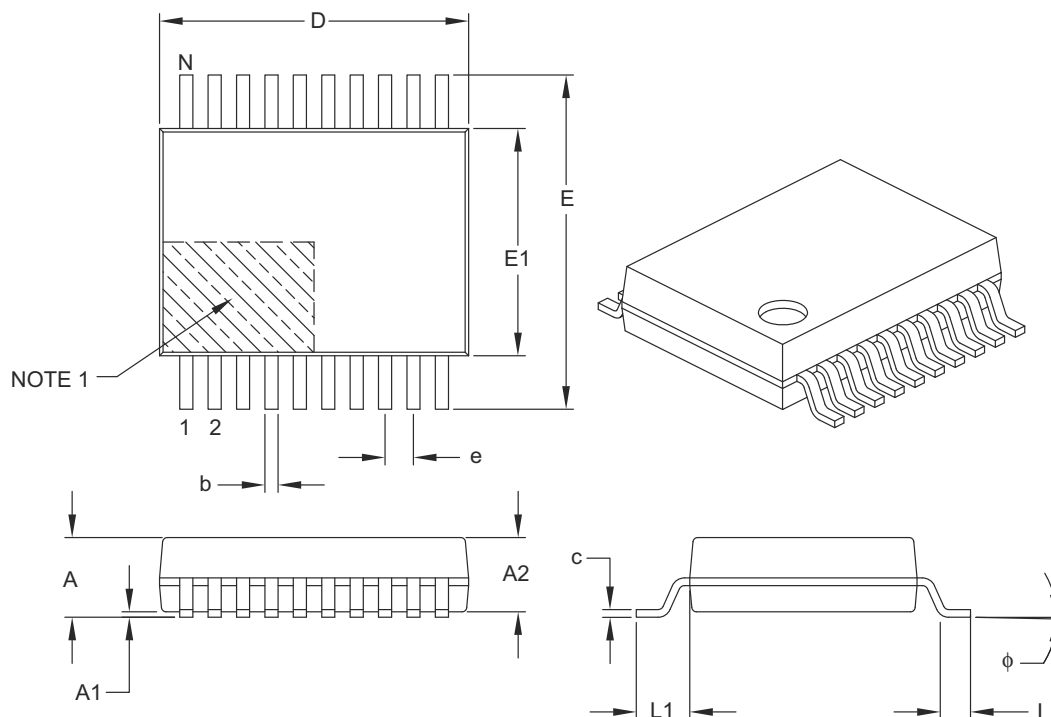
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

PIC24FV32KA304 FAMILY

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B