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#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24f32ka301-i-so">https://www.e-xfl.com/product-detail/microchip-technology/pic24f32ka301-i-so</a>

# PIC24FV32KA304 FAMILY

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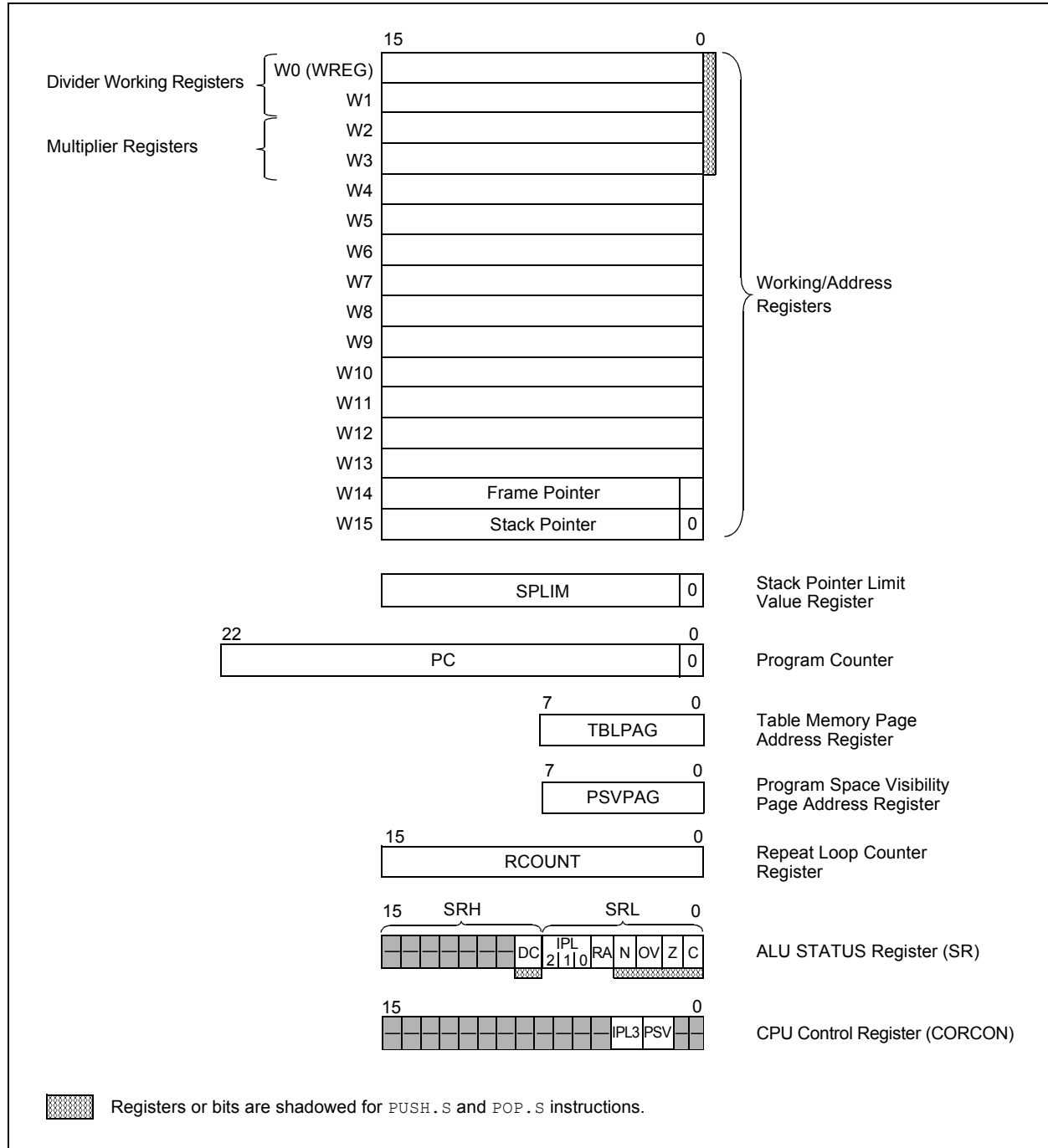
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**TABLE 1-3: PIC24FV32KA304 FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
CN23	11	16	13	43	47	11	16	13	43	47	I	ST	Interrupt-on-Change Inputs
CN24	—	15	12	42	46	—	15	12	42	46	I	ST	
CN25	—	—	—	37	40	—	—	—	37	40	I	ST	
CN26	—	—	—	38	41	—	—	—	38	41	I	ST	
CN27	—	14	11	41	45	—	14	11	41	45	I	ST	
CN28	—	—	—	36	39	—	—	—	36	39	I	ST	
CN29	8	10	7	31	34	8	10	7	31	34	I	ST	
CN30	7	9	6	30	33	7	9	6	30	33	I	ST	
CN31	—	—	—	26	28	—	—	—	26	28	I	ST	
CN32	—	—	—	25	27	—	—	—	25	27	I	ST	
CN33	—	—	—	32	35	—	—	—	32	35	I	ST	
CN34	—	—	—	35	38	—	—	—	35	38	I	ST	
CN35	—	—	—	12	13	—	—	—	12	13	I	ST	
CN36	—	—	—	13	14	—	—	—	13	14	I	ST	
CVREF	17	25	22	14	15	17	25	22	14	15	I	ANA	Comparator Voltage Reference Output
CVREF+	2	2	27	19	21	2	2	27	19	21	I	ANA	Comparator Reference Positive Input Voltage
CVREF-	3	3	28	20	22	3	3	28	20	22	I	ANA	Comparator Reference Negative Input Voltage
CTCMP	4	4	1	21	23	4	4	1	21	23	I	ANA	CTMU Comparator Input
CTED1	14	20	17	7	7	11	2	27	19	21	I	ST	CTMU Trigger Edge Inputs
CTED2	15	23	20	10	11	15	23	20	10	11	I	ST	
CTED3	—	19	16	6	6	—	19	16	6	6	I	ST	
CTED4	13	18	15	1	1	13	18	15	1	1	I	ST	
CTED5	17	25	22	14	15	17	25	22	14	15	I	ST	
CTED6	18	26	23	15	16	18	26	23	15	16	I	ST	
CTED7	—	—	—	5	5	—	—	—	5	5	I	ST	
CTED8	—	—	—	13	14	—	—	—	13	14	I	ST	
CTED9	—	22	19	9	10	—	22	19	9	10	I	ST	
CTED10	12	17	14	44	48	12	17	14	44	48	I	ST	
CTED11	—	21	18	8	9	—	21	18	8	9	I	ST	
CTED12	5	5	2	22	24	5	5	2	22	24	I	ST	
CTED13	6	6	3	23	25	6	6	3	23	25	I	ST	

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**FIGURE 3-2: PROGRAMMER'S MODEL**



# PIC24FV32KA304 FAMILY

## 4.3.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into a 16K word page (in PIC24FV16KA3XX devices) and a 32K word page (in PIC24FV32KA3XX devices) of the program space. This provides transparent access of stored constant data from the data space without the need to use special instructions (i.e., TBLRD/L/H).

Program space access through the data space occurs if the MSb of the data space EA is '1' and PSV is enabled by setting the PSV bit in the CPU Control (CORCON<2>) register. The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page Address (PSVPAG) register. This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits.

By incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads from this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address, 8000h and higher, maps directly into a corresponding program memory address (see Figure 4-7), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space location used as data should be programmed with '1111 1111' or '0000 0000' to force a NOE. This prevents possible issues should the area of code ever be accidentally executed.

**Note:** PSV access is temporarily disabled during table reads/writes.

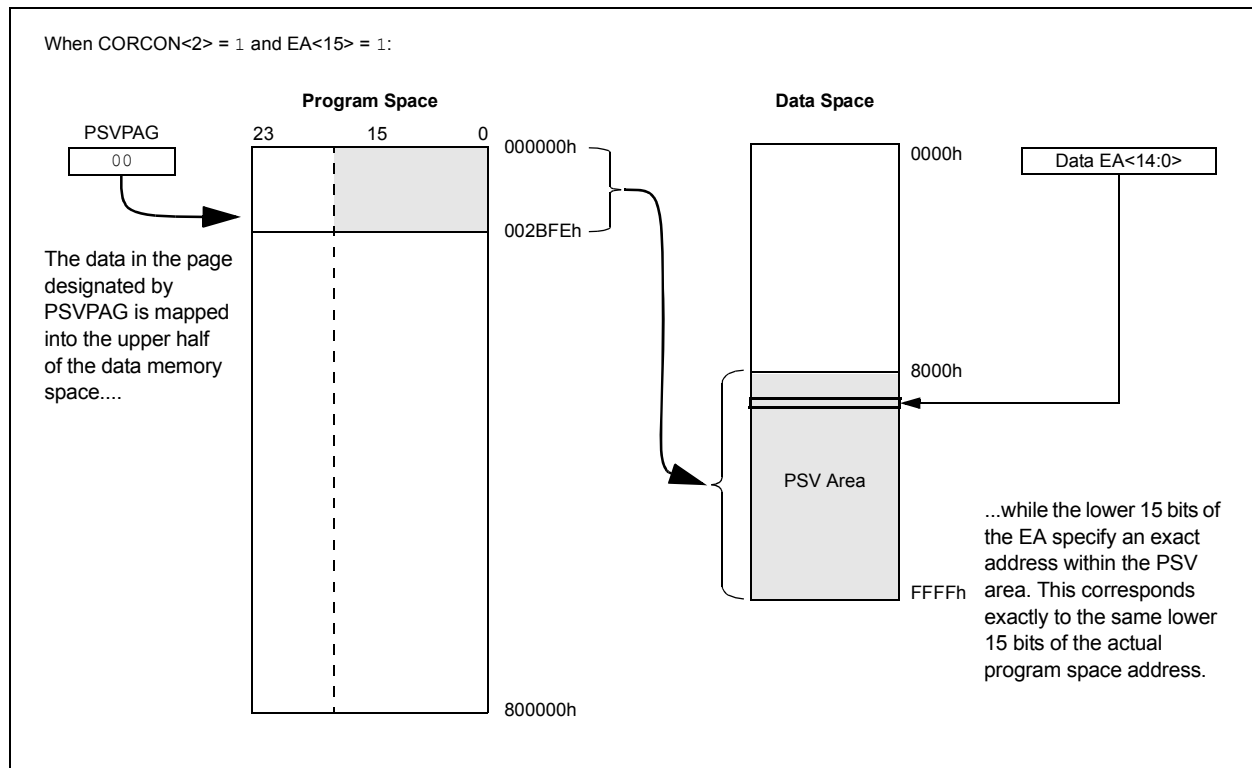
For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions will require one instruction cycle in addition to the specified execution time. All other instructions will require two instruction cycles in addition to the specified execution time.

For operations that use PSV, which are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction accessing data, using PSV, to execute in a single cycle.

**FIGURE 4-7: PROGRAM SPACE VISIBILITY OPERATION**



## 6.0 DATA EEPROM MEMORY

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Data EEPROM, refer to the “PIC24F Family Reference Manual”, Section 5. “Data EEPROM” (DS39720).

The data EEPROM memory is a Nonvolatile Memory (NVM), separate from the program and volatile data RAM. Data EEPROM memory is based on the same Flash technology as program memory, and is optimized for both long retention and a higher number of erase/write cycles.

The data EEPROM is mapped to the top of the user program memory space, with the top address at program memory address, 7FFE00h to 7FFFFFFh. The size of the data EEPROM is 256 words in the PIC24FV32KA304 family devices.

The data EEPROM is organized as 16-bit wide memory. Each word is directly addressable, and is readable and writable during normal operation over the entire VDD range.

Unlike the Flash program memory, normal program execution is not stopped during a data EEPROM program or erase operation.

The data EEPROM programming operations are controlled using the three NVM Control registers:

- NVMCON: Nonvolatile Memory Control Register
- NVMKEY: Nonvolatile Memory Key Register
- NVMADR: Nonvolatile Memory Address Register

## 6.1 NVMCON Register

The NVMCON register (Register 6-1) is also the primary control register for data EEPROM program/erase operations. The upper byte contains the control bits used to start the program or erase cycle, and the flag bit to indicate if the operation was successfully performed. The lower byte of NVMCOM configures the type of NVM operation that will be performed.

## 6.2 NVMKEY Register

The NVMKEY is a write-only register that is used to prevent accidental writes or erasures of data EEPROM locations.

To start any programming or erase sequence, the following instructions must be executed first, in the exact order provided:

1. Write 55h to NVMKEY.
2. Write AAh to NVMKEY.

After this sequence, a write will be allowed to the NVMCON register for one instruction cycle. In most cases, the user will simply need to set the WR bit in the NVMCON register to start the program or erase cycle. Interrupts should be disabled during the unlock sequence.

The MPLAB® C30 C compiler provides a defined library procedure (`builtin_write_nvm`) to perform the unlock sequence. Example 6-1 illustrates how the unlock sequence can be performed with in-line assembly.

### EXAMPLE 6-1: DATA EEPROM UNLOCK SEQUENCE

```
//Disable Interrupts For 5 instructions
asm volatile ("disi #5");
//Issue Unlock Sequence
asm volatile ("mov #0x55, W0    \n"
              "mov W0, NVMKEY    \n"
              "mov #0xAA, W1     \n"
              "mov W1, NVMKEY    \n");
// Perform Write/Erase operations
asm volatile ("bset NVMCON, #WR  \n"
              "nop                \n"
              "nop                \n");
```

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## REGISTER 8-21: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1P2	MI2C1P1	MI2C1P0	—	SI2C1P2	SI2C1P1	SI2C1P0
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CNIP<2:0>:** Input Change Notification Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

.

.

.

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

.

.

.

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MI2C1P<2:0>:** Master I2C1 Event Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

.

.

.

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **SI2C1P<2:0>:** Slave I2C1 Event Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

.

.

.

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

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REGISTER 8-26: IPC9: INTERRUPT PRIORITY CONTROL REGISTER 9

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	IC3IP2	IC3IP1	IC3IP0	—	—	—	—
bit 7							bit 0

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-7      **Unimplemented:** Read as '0'
- bit 6-4      **IC3IP<2:0>:** Input Capture Channel 3 Event Interrupt Priority bits  
111 = Interrupt is Priority 7 (highest priority interrupt)  
.  
.  
.  
001 = Interrupt is Priority 1  
000 = Interrupt source is disabled
- bit 3-0      **Unimplemented:** Read as '0'

# PIC24FV32KA304 FAMILY

## 9.3 Control Registers

The operation of the oscillator is controlled by three Special Function Registers (SFRs):

- OSCCON
- CLKDIV
- OSCTUN

The OSCCON register (Register 9-1) is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources.

The Clock Divider register (Register 9-2) controls the features associated with Doze mode, as well as the postscaler for the FRC oscillator.

The FRC Oscillator Tune register (Register 9-3) allows the user to fine tune the FRC oscillator over a range of approximately  $\pm 5.25\%$ . Each bit increment or decrement changes the factory calibrated frequency of the FRC oscillator by a fixed amount.

### REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R-0, HSC	R-0, HSC	R-0, HSC	U-0	R/W-x <sup>(1)</sup>	R/W-x <sup>(1)</sup>	R/W-x <sup>(1)</sup>
—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0
bit 15				bit 8			

R/SO-0, HSC	U-0	R-0, HSC <sup>(2)</sup>	U-0	R/CO-0, HS	R/W-0 <sup>(3)</sup>	R/W-0	R/W-0
CLKLOCK	—	LOCK	—	CF	SOSCDRV	SOSCEN	OSWEN
bit 7				bit 0			

<b>Legend:</b>	HSC = Hardware Settable/Clearable bit		
HS = Hardware Settable bit	CO = Clearable Only bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits

- 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = 8 MHz FRC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits<sup>(1)</sup>

- 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = 8 MHz FRC Oscillator (FRC)

**Note 1:** Reset values for these bits are determined by the FNOSC<sub>x</sub> Configuration bits.

**2:** This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

**3:** When SOSC is selected to run from a digital clock input, rather than an external crystal (SOSC<sub>SRC</sub> = 0), this bit has no effect.

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The following code sequence for a clock switch is recommended:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON<15:8>, in two back-to-back instructions.
3. Write new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON<7:0>, in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock-sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'. If it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of failure.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1.

## EXAMPLE 9-1: BASIC CODE SEQUENCE FOR CLOCK SWITCHING

```
;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
MOV    #OSCCONH, w1
MOV    #0x78, w2
MOV    #0x9A, w3
MOV.b  w2, [w1]
MOV.b  w3, [w1]
;Set new oscillator selection
MOV.b  WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV    #OSCCONL, w1
MOV    #0x46, w2
MOV    #0x57, w3
MOV.b  w2, [w1]
MOV.b  w3, [w1]
;Start oscillator switch operation
BSET   OSCCON, #0
```

## 9.5 Reference Clock Output

In addition to the CLK0 output ( $F_{osc}/2$ ) available in certain oscillator modes, the device clock in the PIC24FV32KA304 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCON register (Register 9-4). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The RODIVx bits (REFOCON<11:8>) enable the selection of 16 different clock divider options.

The ROSSLP and ROSEL bits (REFOCON<13:12>) control the availability of the reference output during Sleep mode. The ROSEL bit determines if the oscillator on OSC1 and OSC2, or the current system clock source, is used for the reference clock output. The ROSSLP bit determines if the reference source is available on REFO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSSLP and ROSEL bits must be set. The device clock must also be configured for one of the primary modes (EC, HS or XT); otherwise, if the ROSEL bit is not also set, the oscillator on OSC1 and OSC2 will be powered down when the device enters Sleep mode. Clearing the ROSEL bit allows the reference output frequency to change as the system clock changes during any clock switches.

# PIC24FV32KA304 FAMILY

## 14.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own 16-bit timer. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module (ICx) provides the Least Significant 16 bits of the 32-bit register pairs, and the even numbered module (ICy) provides the Most Significant 16 bits. Wraparounds of the ICx registers cause an increment of their corresponding ICy registers.

Cascaded operation is configured in hardware by setting the IC32 bit (ICxCON2<8>) for both modules.

## 14.2 Capture Operations

The input capture module can be configured to capture timer values and generate interrupts on rising edges on ICx or all transitions on ICx. Captures can be configured to occur on all rising edges or just some (every 4th or 16th). Interrupts can be independently configured to generate on each event or a subset of events.

To set up the module for capture operations:

1. If Synchronous mode is to be used, disable the Sync source before proceeding.
2. Make sure that any previous data has been removed from the FIFO by reading ICxBUF until the ICBNE bit (ICxCON1<3>) is cleared.
3. Set the SYNCSELx bits (ICxCON2<4:0>) to the desired Sync/trigger source.
4. Set the ICTSELx bits (ICxCON1<12:10>) for the desired clock source. If the desired clock source is running, set the ICTSELx bits before the input capture module is enabled, for proper synchronization with the desired clock source.
5. Set the ICLx bits (ICxCON1<6:5>) to the desired interrupt frequency.
6. Select Synchronous or Trigger mode operation:
  - a) Check that the SYNCSELx bits are not set to '00000'.
  - b) For Synchronous mode, clear the ICTRIG bit (ICxCON2<7>).
  - c) For Trigger mode, set ICTRIG and clear the TRIGSTAT bit (ICxCON2<6>).
7. Set the ICMx bits (ICxCON1<2:0>) to the desired operational mode.
8. Enable the selected Sync/trigger source.

For 32-bit cascaded operations, the setup procedure is slightly different:

1. Set the IC32 bits for both modules (ICyCON2<8> and ICxCON2<8>), enabling the even numbered module first. This ensures the modules will start functioning in unison.
2. Set the ICTSELx and SYNCSELx bits for both modules to select the same Sync/trigger and time base source. Set the even module first, then the odd module. Both modules must use the same ICTSELx and SYNCSELx bit settings.
3. Clear the ICTRIG bit of the even module (ICyCON2<7>). This forces the module to run in Synchronous mode with the odd module, regardless of its trigger setting.
4. Use the odd module's ICLx bits (ICxCON1<6:5>) to the desired interrupt frequency.
5. Use the ICTRIG bit of the odd module (ICxCON2<7>) to configure Trigger or Synchronous mode operation.

**Note:** For Synchronous mode operation, enable the Sync source as the last step. Both input capture modules are held in Reset until the Sync source is enabled.

6. Use the ICMx bits of the odd module (ICxCON1<2:0>) to set the desired capture mode.

The module is ready to capture events when the time base and the Sync/trigger source are enabled. When the ICBNE bit (ICxCON1<3>) becomes set, at least one capture value is available in the FIFO. Read input capture values from the FIFO until the ICBNE clears to '0'.

For 32-bit operation, read both the ICxBUF and ICyBUF for the full 32-bit timer value (ICxBUF for the lsw, ICyBUF for the msw). At least one capture value is available in the FIFO buffer when the odd module's ICBNE bit (ICxCON1<3>) becomes set. Continue to read the buffer registers until ICBNE is cleared (performed automatically by hardware).

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## REGISTER 21-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	HLSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **HLVDEN:** High/Low-Voltage Detect Power Enable bit

1 = HLVD is enabled

0 = HLVD is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **HLSIDL:** HLVD Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **VDIR:** Voltage Change Direction Select bit

1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)

0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 6 **BGVST:** Band Gap Voltage Stable Flag bit

1 = Indicates that the band gap voltage is stable

0 = Indicates that the band gap voltage is unstable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit

1 = Indicates that the internal reference voltage is stable and the high-voltage detect logic generates the interrupt flag at the specified voltage range

0 = Indicates that the internal reference voltage is unstable and the high-voltage detect logic will not generate the interrupt flag at the specified voltage range, and the HLVD interrupt should not be enabled

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the HLVDIN pin)

1110 = Trip Point 1<sup>(1)</sup>

1101 = Trip Point 2<sup>(1)</sup>

1100 = Trip Point 3<sup>(1)</sup>

.

.

.

0000 = Trip Point 15<sup>(1)</sup>

**Note 1:** For the actual trip point, see Section 29.0 "Electrical Characteristics".

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## 22.1 A/D Control Registers

The 12-bit A/D Converter module uses up to 43 registers for its operation. All registers are mapped in the data memory space.

### 22.1.1 CONTROL REGISTERS

Depending on the specific device, the module has up to eleven control and status registers:

- AD1CON1: A/D Control Register 1
- AD1CON2: A/D Control Register 2
- AD1CON3: A/D Control Register 3
- AD1CON5: A/D Control Register 5
- AD1CHS: A/D Sample Select Register
- AD1CHITH and AD1CHITL: A/D Scan Compare Hit Registers
- AD1CSSL and AD1CSSH: A/D Input Scan Select Registers
- AD1CTMUENH and AD1CTMUENL: CTMU Enable Registers

The AD1CON1, AD1CON2 and AD1CON3 registers (Register 22-1, Register 22-2 and Register 22-3) control the overall operation of the A/D module. This includes enabling the module, configuring the conversion clock and voltage reference sources, selecting the sampling and conversion triggers, and manually controlling the sample/convert sequences. The AD1CON5 register (Register 22-4) specifically controls features of the Threshold Detect operation, including its function in power-saving modes.

The AD1CHS register (Register 22-5) selects the input channels to be connected to the S/H amplifier. It also allows the choice of input multiplexers and the selection of a reference source for differential sampling.

The AD1CHITH and AD1CHITL registers (Register 22-6 and Register 22-7) are semaphore registers used with Threshold Detect operations. The status of individual bits, or bit pairs in some cases,

indicate if a match condition has occurred. AD1CHITL is always implemented, whereas AD1CHITH may not be implemented in devices with 16 or fewer channels.

The AD1CSSH/L registers (Register 22-8 and Register 22-9) select the channels to be included for sequential scanning.

The AD1CTMUENH/L registers (Register 22-10 and Register 22-11) select the channel(s) to be used by the CTMU during conversions. Selecting a particular channel allows the A/D Converter to control the CTMU (particularly, its current source) and read its data through that channel. AD1CTMUENL is always implemented, whereas AD1CTMUENH may not be implemented in devices with 16 or fewer channels.

### 22.1.2 A/D RESULT BUFFERS

The module incorporates a multi-word, dual port RAM, called ADC1BUF. The buffer is composed of at least the same number of word locations as there are external analog channels for a particular device, with a maximum number of 32. The number of buffer addresses is always even. Each of the locations is mapped into the data memory space and is separately addressable. The buffer locations are referred to as ADC1BUF0 through ADC1BUFn (up to 31).

The A/D result buffers are both readable and writable. When the module is active (AD1CON<15> = 1), the buffers are read-only, and store the results of A/D conversions. When the module is inactive (AD1CON<15> = 0), the buffers are both readable and writable. In this state, writing to a buffer location programs a conversion threshold for Threshold Detect operations.

Buffer contents are not cleared when the module is deactivated with the ADON bit (AD1CON1<15>). Conversion results and any programmed threshold values are maintained when ADON is set or cleared.

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**REGISTER 26-8: FDS: DEEP SLEEP CONFIGURATION REGISTER**

R/P-1	R/P-1	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
DSWDTEN	DSBORN	—	DSWDTOSC	DSWDTPS3	DSWDTPS2	DSWDTPS1	DSWDTPS0
bit 7							bit 0

**Legend:**

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit

1 = DSWDT is enabled

0 = DSWDT is disabled

bit 6 **DSBORN:** Deep Sleep/Low-Power BOR Enable bit  
(does not affect operation in non Deep Sleep modes)

1 = Deep Sleep BOR is enabled in Deep Sleep

0 = Deep Sleep BOR is disabled in Deep Sleep

bit 5 **Unimplemented:** Read as '0'

bit 4 **DSWDTOSC:** DSWDT Reference Clock Select bit

1 = DSWDT uses LPRC as the reference clock

0 = DSWDT uses SOSC as the reference clock

bit 3-0 **DSWDTPS<3:0>:** Deep Sleep Watchdog Timer Postscale Select bits

The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms.

1111 = 1:2,147,483,648 (25.7 days) nominal

1110 = 1:536,870,912 (6.4 days) nominal

1101 = 1:134,217,728 (38.5 hours) nominal

1100 = 1:33,554,432 (9.6 hours) nominal

1011 = 1:8,388,608 (2.4 hours) nominal

1010 = 1:2,097,152 (36 minutes) nominal

1001 = 1:524,288 (9 minutes) nominal

1000 = 1:131,072 (135 seconds) nominal

0111 = 1:32,768 (34 seconds) nominal

0110 = 1:8,192 (8.5 seconds) nominal

0101 = 1:2,048 (2.1 seconds) nominal

0100 = 1:512 (528 ms) nominal

0011 = 1:128 (132 ms) nominal

0010 = 1:32 (33 ms) nominal

0001 = 1:8 (8.3 ms) nominal

0000 = 1:2 (2.1 ms) nominal

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## REGISTER 26-10: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23				bit 16			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV3	REV2	REV1	REV0
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 23-4      **Unimplemented:** Read as '0'

bit 3-0      **REV<3:0>:** Minor Revision Identifier bits

## 27.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C® for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICKit™ 3 Debug Express
- Device Programmers
  - PICKit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

## 27.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

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## 27.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 27.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

## 27.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta A/D, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

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**TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
PWRSV	PWRSV #lit1	Go into Sleep or Idle mode	1	1	WDTO, Sleep
RCALL	RCALL Expr	Relative Call	1	2	None
	RCALL Wn	Computed Call	1	2	None
REPEAT	REPEAT #lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
	REPEAT Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
RESET	RESET	Software Device Reset	1	1	None
RETFIE	RETFIE	Return from Interrupt	1	3 (2)	None
RETLW	RETLW #lit10,Wn	Return with Literal in Wn	1	3 (2)	None
RETURN	RETURN	Return from Subroutine	1	3 (2)	None
RLC	RLC f	f = Rotate Left through Carry f	1	1	C, N, Z
	RLC f, WREG	WREG = Rotate Left through Carry f	1	1	C, N, Z
	RLC Ws, Wd	Wd = Rotate Left through Carry Ws	1	1	C, N, Z
RLNC	RLNC f	f = Rotate Left (No Carry) f	1	1	N, Z
	RLNC f, WREG	WREG = Rotate Left (No Carry) f	1	1	N, Z
	RLNC Ws, Wd	Wd = Rotate Left (No Carry) Ws	1	1	N, Z
RRC	RRC f	f = Rotate Right through Carry f	1	1	C, N, Z
	RRC f, WREG	WREG = Rotate Right through Carry f	1	1	C, N, Z
	RRC Ws, Wd	Wd = Rotate Right through Carry Ws	1	1	C, N, Z
RRNC	RRNC f	f = Rotate Right (No Carry) f	1	1	N, Z
	RRNC f, WREG	WREG = Rotate Right (No Carry) f	1	1	N, Z
	RRNC Ws, Wd	Wd = Rotate Right (No Carry) Ws	1	1	N, Z
SE	SE Ws, Wnd	Wnd = Sign-Extended Ws	1	1	C, N, Z
SETM	SETM f	f = FFFFh	1	1	None
	SETM WREG	WREG = FFFFh	1	1	None
	SETM Ws	Ws = FFFFh	1	1	None
SL	SL f	f = Left Shift f	1	1	C, N, OV, Z
	SL f, WREG	WREG = Left Shift f	1	1	C, N, OV, Z
	SL Ws, Wd	Wd = Left Shift Ws	1	1	C, N, OV, Z
	SL Wb, Wns, Wnd	Wnd = Left Shift Wb by Wns	1	1	N, Z
	SL Wb, #lit5, Wnd	Wnd = Left Shift Wb by lit5	1	1	N, Z
SUB	SUB f	f = f – WREG	1	1	C, DC, N, OV, Z
	SUB f, WREG	WREG = f – WREG	1	1	C, DC, N, OV, Z
	SUB #lit10, Wn	Wn = Wn – lit10	1	1	C, DC, N, OV, Z
	SUB Wb, Ws, Wd	Wd = Wb – Ws	1	1	C, DC, N, OV, Z
	SUB Wb, #lit5, Wd	Wd = Wb – lit5	1	1	C, DC, N, OV, Z
SUBB	SUBB f	f = f – WREG – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
	SUBB f, WREG	WREG = f – WREG – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
	SUBB #lit10, Wn	Wn = Wn – lit10 – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
	SUBB Wb, Ws, Wd	Wd = Wb – Ws – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
	SUBB Wb, #lit5, Wd	Wd = Wb – lit5 – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
SUBR	SUBR f	f = WREG – f	1	1	C, DC, N, OV, Z
	SUBR f, WREG	WREG = WREG – f	1	1	C, DC, N, OV, Z
	SUBR Wb, Ws, Wd	Wd = Ws – Wb	1	1	C, DC, N, OV, Z
	SUBR Wb, #lit5, Wd	Wd = lit5 – Wb	1	1	C, DC, N, OV, Z
SUBBR	SUBBR f	f = WREG – f – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
	SUBBR f, WREG	WREG = WREG – f – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
	SUBBR Wb, Ws, Wd	Wd = Ws – Wb – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
	SUBBR Wb, #lit5, Wd	Wd = lit5 – Wb – ( $\overline{C}$ )	1	1	C, DC, N, OV, Z
SWAP	SWAP.b Wn	Wn = Nibble Swap Wn	1	1	None
	SWAP Wn	Wn = Byte Swap Wn	1	1	None
TBLRDH	TBLRDH Ws, Wd	Read Prog<23:16> to Wd<7:0>	1	2	None

# PIC24FV32KA304 FAMILY

**TABLE 29-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS**

Operating Conditions: $-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ (unless otherwise stated)							
Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
DVR10	V <sub>BG</sub>	Band Gap Reference Voltage	0.973	1.024	1.075	V	
DVR11	T <sub>BG</sub>	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	V <sub>RGOUT</sub>	Regulator Output Voltage	3.1	3.3	3.6	V	$-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$
			3.0	3.19	3.6	V	$-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$
DVR21	C <sub>EFC</sub>	External Filter Capacitor Value	4.7	10	—	μF	Series resistance < 3 Ohm recommended; < 5 Ohm is required.
DVR30	V <sub>LVR</sub>	Retention Regulator Output Voltage	—	2.6	—	V	

**TABLE 29-16: CTMU CURRENT SOURCE SPECIFICATIONS**

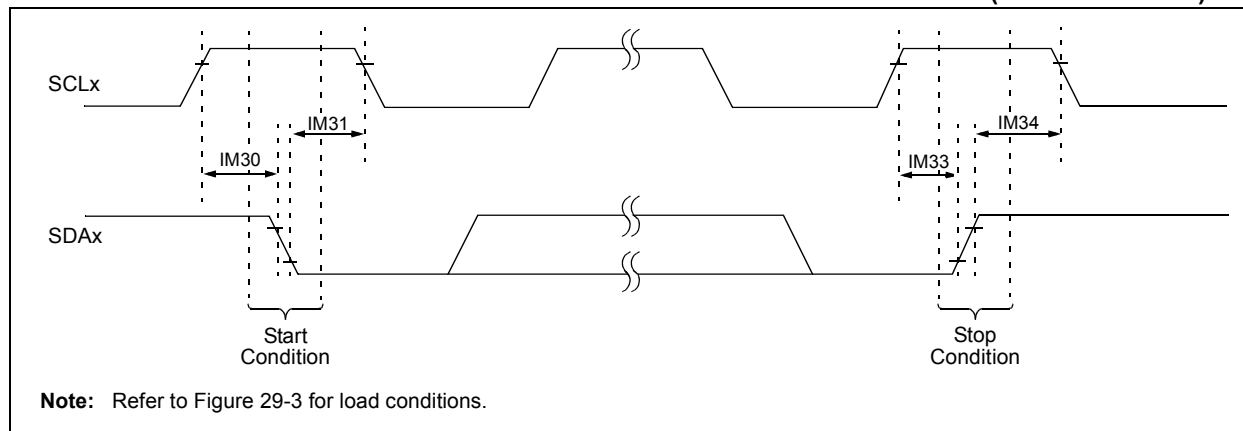
DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX					
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Sym	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Comments	Conditions
DCT10	I <sub>OUT1</sub>	CTMU Current Source, Base Range	—	550	—	nA	CTMUICON<9:8> = 01	2.5V < V <sub>DD</sub> < V <sub>DDMAX</sub>
DCT11	I <sub>OUT2</sub>	CTMU Current Source, 10x Range	—	5.5	—	μA	CTMUICON<9:8> = 10	
DCT12	I <sub>OUT3</sub>	CTMU Current Source, 100x Range	—	55	—	μA	CTMUICON<9:8> = 11	
DCT13	I <sub>OUT4</sub>	CTMU Current Source, 1000x Range	—	550	—	μA	CTMUICON<9:8> = 00 (Note 2)	
DCT20	V <sub>F</sub>	Temperature Diode Forward Voltage	—	.76	—	V		
DCT21	V <sub>Δ</sub>	Voltage Change per Degree Celsius	—	1.6	—	mV/°C		

**Note 1:** Nominal value at the center point of the current trim range (CTMUICON<7:2> = 000000). On PIC24F32KA parts, the current output is limited to the typical current value when I<sub>OUT4</sub> is chosen.

**2:** Do not use this current range with a temperature sensing diode.

# PIC24FV32KA304 FAMILY

**FIGURE 29-12: I<sup>2</sup>C™ BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**



**TABLE 29-31: I<sup>2</sup>C™ BUS START/STOP BIT TIMING REQUIREMENTS (MASTER MODE)**

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T <sub>A</sub> ≤ +85°C for Industrial) -40°C ≤ T <sub>A</sub> ≤ +125°C for Extended			
Param No.	Symbol	Characteristic		Min <sup>(1)</sup>	Max	Units	Conditions
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	T <sub>CY</sub> /2 (BRG + 1)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	T <sub>CY</sub> /2 (BRG + 1)	—	μs	
			1 MHz mode <sup>(2)</sup>	T <sub>CY</sub> /2 (BRG + 1)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	T <sub>CY</sub> /2 (BRG + 1)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	T <sub>CY</sub> /2 (BRG + 1)	—	μs	
			1 MHz mode <sup>(2)</sup>	T <sub>CY</sub> /2 (BRG + 1)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	T <sub>CY</sub> /2 (BRG + 1)	—	μs	
			400 kHz mode	T <sub>CY</sub> /2 (BRG + 1)	—	μs	
			1 MHz mode <sup>(2)</sup>	T <sub>CY</sub> /2 (BRG + 1)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	T <sub>CY</sub> /2 (BRG + 1)	—	ns	
			400 kHz mode	T <sub>CY</sub> /2 (BRG + 1)	—	ns	
			1 MHz mode <sup>(2)</sup>	T <sub>CY</sub> /2 (BRG + 1)	—	ns	

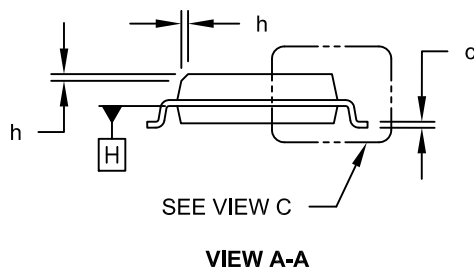
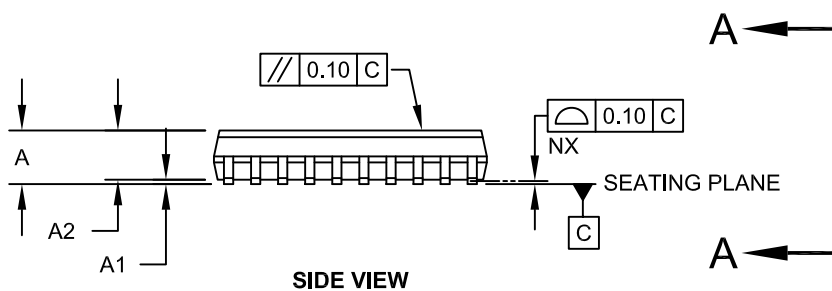
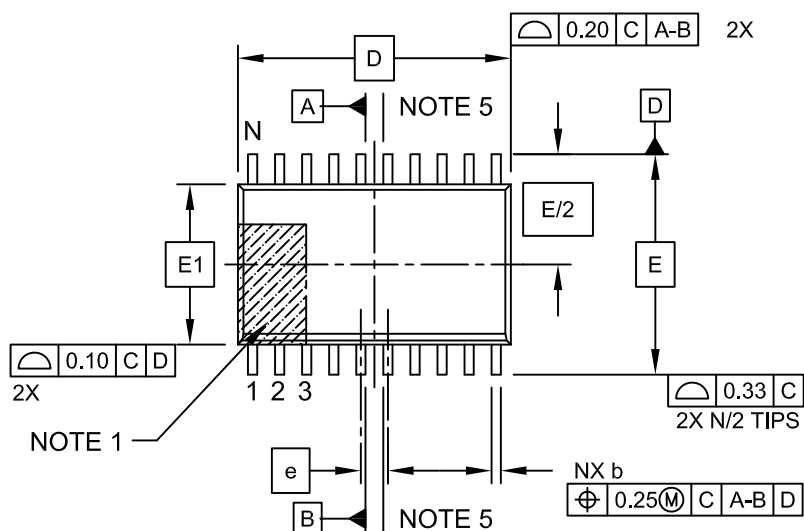
**Note 1:** BRG is the value of the I<sup>2</sup>C™ Baud Rate Generator. Refer to **Section 17.3 “Setting Baud Rate When Operating as a Bus Master”** for details.

**2:** Maximum pin capacitance = 10 pF for all I<sup>2</sup>C pins (for 1 MHz mode only).

# PIC24FV32KA304 FAMILY

## 20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-094C Sheet 1 of 2