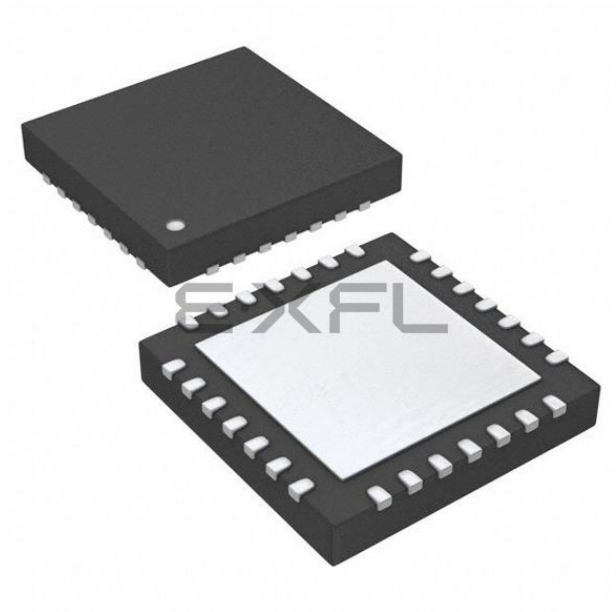

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f32ka302-i-ml

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FV32KA304 FAMILY

Features	PIC24FV16KA301	PIC24FV32KA301	PIC24FV16KA302	PIC24FV32KA302	PIC24FV16KA304	PIC24FV32KA304
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	16K	32K	16K	32K	16K	32K
Program Memory (instructions)	5632	11264	5632	11264	5632	11264
Data Memory (bytes)	2048					
Data EEPROM Memory (bytes)	512					
Interrupt Sources (soft vectors/ NMI traps)	30 (26/4)					
I/O Ports	PORTA<5:0> PORTB<15:12,9:7,4,2:0>		PORTA<7,5:0> PORTB<15:0>		PORTA<11:7,5:0> PORTB<15:0> PORTC<9:0>	
Total I/O Pins	17		23		38	
Timers: Total Number (16-bit)	5					
32-Bit (from paired 16-bit timers)	2					
Input Capture Channels	3					
Output Compare/PWM Channels	3					
Input Change Notification Interrupt	16		22		37	
Serial Communications: UART SPI (3-wire/4-wire)	2					
I^2C™	2					
12-Bit Analog-to-Digital Module (input channels)	12		13		16	
Analog Comparators	3					
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)					
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations					
Packages	20-Pin PDIP/SSOP/SOIC		28-Pin SPDIP/SSOP/SOIC/QFN		44-Pin QFN/TQFP 48-Pin UQFN	

TABLE 1-3: PIC24FV32KA304 FAMILY PINOUT DESCRIPTIONS

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
AN0	2	2	27	19	21	2	2	27	19	21	I	ANA	A/D Analog Inputs
AN1	3	3	28	20	22	3	3	28	20	22	I	ANA	
AN2	4	4	1	21	23	4	4	1	21	23	I	ANA	
AN3	5	5	2	22	24	5	5	2	22	24	I	ANA	
AN4	6	6	3	23	25	6	6	3	23	25	I	ANA	
AN5	—	7	4	24	26	—	7	4	24	26	I	ANA	
AN6	—	—	—	25	27	—	—	—	25	27	I	ANA	
AN7	—	—	—	26	28	—	—	—	26	28	I	ANA	
AN8	—	—	—	27	29	—	—	—	27	29	I	ANA	
AN9	18	26	23	15	16	18	26	23	15	16	I	ANA	
AN10	17	25	22	14	15	17	25	22	14	15	I	ANA	
AN11	16	24	21	11	12	16	24	21	11	12	I	ANA	
AN12	15	23	20	10	11	15	23	20	10	11	I	ANA	
AN13	7	9	6	30	33	7	9	6	30	33	I	ANA	
AN14	8	10	7	31	34	8	10	7	31	34	I	ANA	
AN15	9	11	8	33	36	9	11	8	33	36	I	ANA	
ASCL1	—	15	12	42	46	—	15	12	42	46	I/O	I^2C™	Alternate I2C1 Clock Input/Output
ASDA1	—	14	11	41	45	—	14	11	41	45	I/O	I^2C	Alternate I2C1 Data Input/Output
AV_{DD}	20	28	25	17	18	20	28	25	17	18	I	ANA	A/D Supply Pins
AV_{SS}	19	27	24	16	17	19	27	24	16	17	I	ANA	
C1INA	8	7	4	24	26	8	7	4	24	26	I	ANA	Comparator 1 Input A (+)
C1INB	7	6	3	23	25	7	6	3	23	25	I	ANA	Comparator 1 Input B (-)
C1INC	5	5	2	22	24	5	5	2	22	24	I	ANA	Comparator 1 Input C (+)
C1IND	4	4	1	21	23	4	4	1	21	23	I	ANA	Comparator 1 Input D (-)
C1OUT	17	25	22	14	15	17	25	22	14	15	O	—	Comparator 1 Output
C2INA	5	5	2	22	24	5	5	2	22	24	I	ANA	Comparator 2 Input A (+)
C2INB	4	4	1	21	23	4	4	1	21	23	I	ANA	Comparator 2 Input B (-)
C2INC	8	7	4	24	26	8	7	4	24	26	I	ANA	Comparator 2 Input C (+)
C2IND	7	6	3	23	25	7	6	3	23	25	I	ANA	Comparator 2 Input D (-)
C2OUT	14	20	17	7	7	11	16	13	43	47	O	—	Comparator 2 Output

NOTES:

3.3.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

1. 32-bit signed/16-bit signed divide
2. 32-bit unsigned/16-bit unsigned divide
3. 16-bit signed/16-bit signed divide
4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. Sixteen-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn), and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.3.3 MULTI-BIT SHIFT SUPPORT

The PIC24F ALU supports both single bit and single-cycle, multi-bit arithmetic and logic shifts. Multi-bit shifts are implemented using a shifter block, capable of performing up to a 15-bit arithmetic right shift, or up to a 15-bit left shift, in a single cycle. All multi-bit shift instructions only support Register Direct Addressing for both the operand source and result destination.

A full summary of instructions that use the shift operation is provided in Table 3-2.

TABLE 3-2: INSTRUCTIONS THAT USE THE SINGLE AND MULTI-BIT SHIFT OPERATION

Instruction	Description
`ASR`	Arithmetic shift right source register by one or more bits.
`SL`	Shift left source register by one or more bits.
`LSR`	Logical shift right source register by one or more bits.

TABLE 4-16: A/D REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0300	ADC1BUF0																xxxx
ADC1BUF1	0302	ADC1BUF1																xxxx
ADC1BUF2	0304	ADC1BUF2																xxxx
ADC1BUF3	0306	ADC1BUF3																xxxx
ADC1BUF4	0308	ADC1BUF4																xxxx
ADC1BUF5	030A	ADC1BUF5																xxxx
ADC1BUF6	030C	ADC1BUF6																xxxx
ADC1BUF7	030E	ADC1BUF7																xxxx
ADC1BUF8	0310	ADC1BUF8																xxxx
ADC1BUF9	0312	ADC1BUF9																xxxx
ADC1BUF10	0314	ADC1BUF10																xxxx
ADC1BUF11	0316	ADC1BUF11																xxxx
ADC1BUF12	0318	ADC1BUF12																xxxx
ADC1BUF13	031A	ADC1BUF13																xxxx
ADC1BUF14	031C	ADC1BUF14																xxxx
ADC1BUF15	031E	ADC1BUF15																xxxx
ADC1BUF16	0320	ADC1BUF16																xxxx
ADC1BUF17	0322	ADC1BUF17																xxxx
AD1CON1	0340	ADON	—	ADSIDL	—	—	MODE12	FORM1	FORM0	SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE	0000
AD1CON2	0342	PVCFG1	PVCFG0	NVCFG0	OFFCAL	BUFREGEN	CSCNA	—	—	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	0344	ADRC	EXTSAM	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	0348	CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	034E	—	CSSL30	CSSL29	CSSL28	CSSL27	CSSL26	—	—	—	—	—	—	—	—	CSSL17	CSSL16	0000
AD1CSSL	0350	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
AD1CON5	0354	ASEN	LPEN	CTMUREQ	BGREQ	r	—	ASINT1	ASINT0	—	—	—	—	WM1	WM0	CM1	CM0	0000
AD1CHITH	0356	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHH17	CHH16	0000
AD1CHITL	0358	CHH15	CHH14	CHH13	CHH12	CHH11	CHH10	CHH9	CHH8	CHH7	CHH6	CHH5	CHH4	CHH3	CHH2	CHH1	CHH0	0000

Legend: — = unimplemented, read as '0'; r = reserved. Reset values are shown in hexadecimal.

REGISTER 8-10: IFS5: INTERRUPT FLAG STATUS REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
—	—	—	—	—	—	—	ULPWUIF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **ULPWUIF:** Ultra Low-Power Wake-up Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-16: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ULPWUIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **ULPWUIE:** Ultra Low-Power Wake-up Interrupt Enable Bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-29: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CRCIP2	CRCIP1	CRCIP0	—	U2ERIP2	U2ERIP1	U2ERIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1ERIP2	U1ERIP1	U1ERIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CRCIP<2:0>:** CRC Generator Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U2ERIP<2:0>:** UART2 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U1ERIP<2:0>:** UART1 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

11.0 I/O PORTS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the I/O Ports, refer to the *"PIC24F Family Reference Manual"*, **Section 12. "I/O Ports with Peripheral Pin Select (PPS)"** (DS39711). Note that the PIC24FV32KA304 family devices do not support Peripheral Pin Select features.

All of the device pins (except VDD and VSS) are shared between the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

A parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

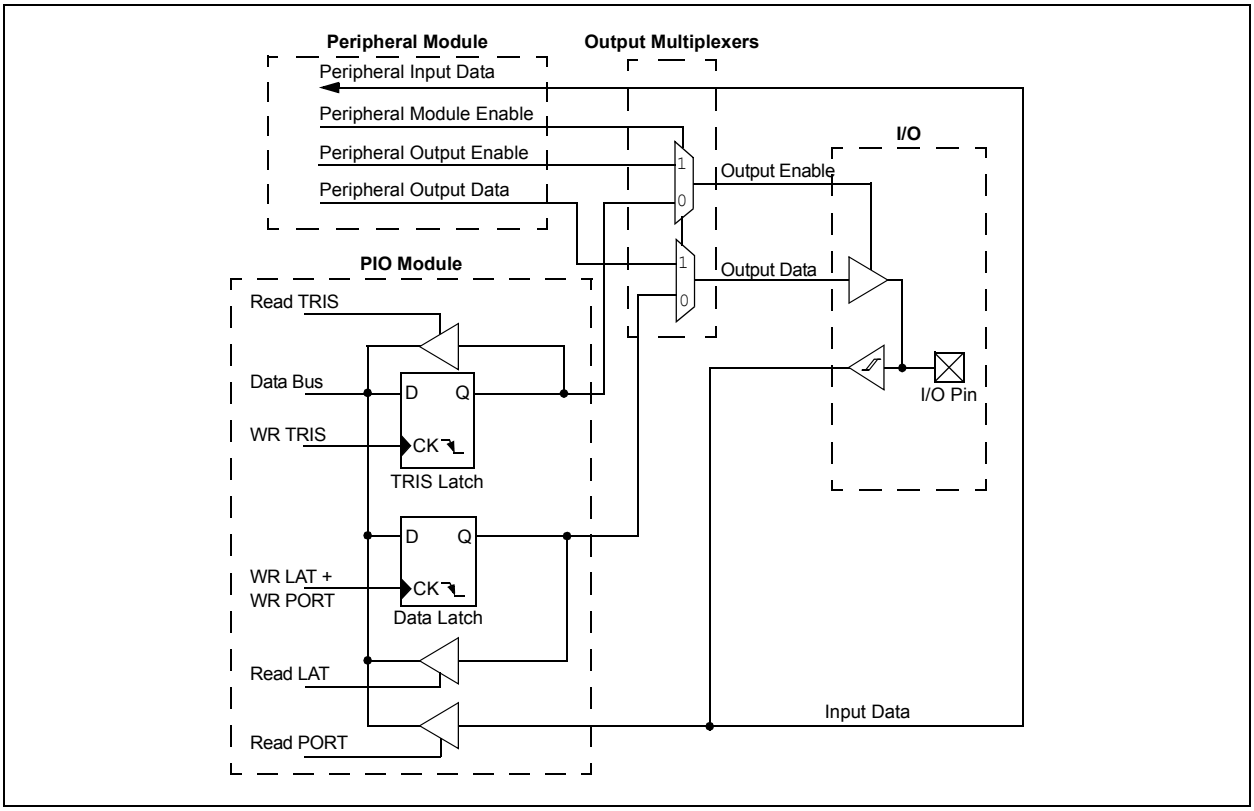
All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Data Latch register (LAT), read the latch. Writes to the latch, write the latch. Reads from the port (PORT), read the port pins; writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

Note: The I/O pins retain their state during Deep Sleep. They will retain this state at wake-up until the software restore bit (RELEASE) is cleared.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



15.0 OUTPUT COMPARE WITH DEDICATED TIMERS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **Section 35. "Output Compare with Dedicated Timer"** (DS39723).

All devices in the PIC24FV32KA304 family feature 3 independent output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events. Also, the modules can produce Pulse-Width Modulated (PWM) waveforms for driving power applications.

Key features of the output compare module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 21 user-selectable Sync/trigger sources available
- Two separate Period registers (a main register, OCxR, and a secondary register, OCxRS) for greater flexibility in generating pulses of varying widths
- Configurable for single pulse or continuous pulse generation on an output event, or continuous PWM waveform generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

15.1 General Operating Modes

15.1.1 SYNCHRONOUS AND TRIGGER MODES

By default, the output compare module operates in a Free-Running mode. The internal 16-bit counter, OCxTMR, counts up continuously, wrapping around from FFFFh to 0000h on each overflow, with its period synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the Period registers occurs.

In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected Sync source, the module's internal counter is reset. In Trigger mode, the module waits for a Sync event from another internal module to occur before allowing the counter to run.

Free-Running mode is selected by default or any time that the SYNCSELx bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSELx bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode. Setting this bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the Sync/trigger source.

15.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-bit Timer and Duty Cycle registers. To increase the range, adjacent even and odd numbered modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module (OCx) provides the Least Significant 16 bits of the 32-bit register pairs, and the even numbered module (OCy) provides the Most Significant 16 bits. Wraparounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bit (OCxCON2<8>) for both modules.

EQUATION 16-1: RELATIONSHIP BETWEEN DEVICE AND SPIx CLOCK SPEED(1)

$$FSCK = \frac{FCY}{\text{Primary Prescaler} * \text{Secondary Prescaler}}$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

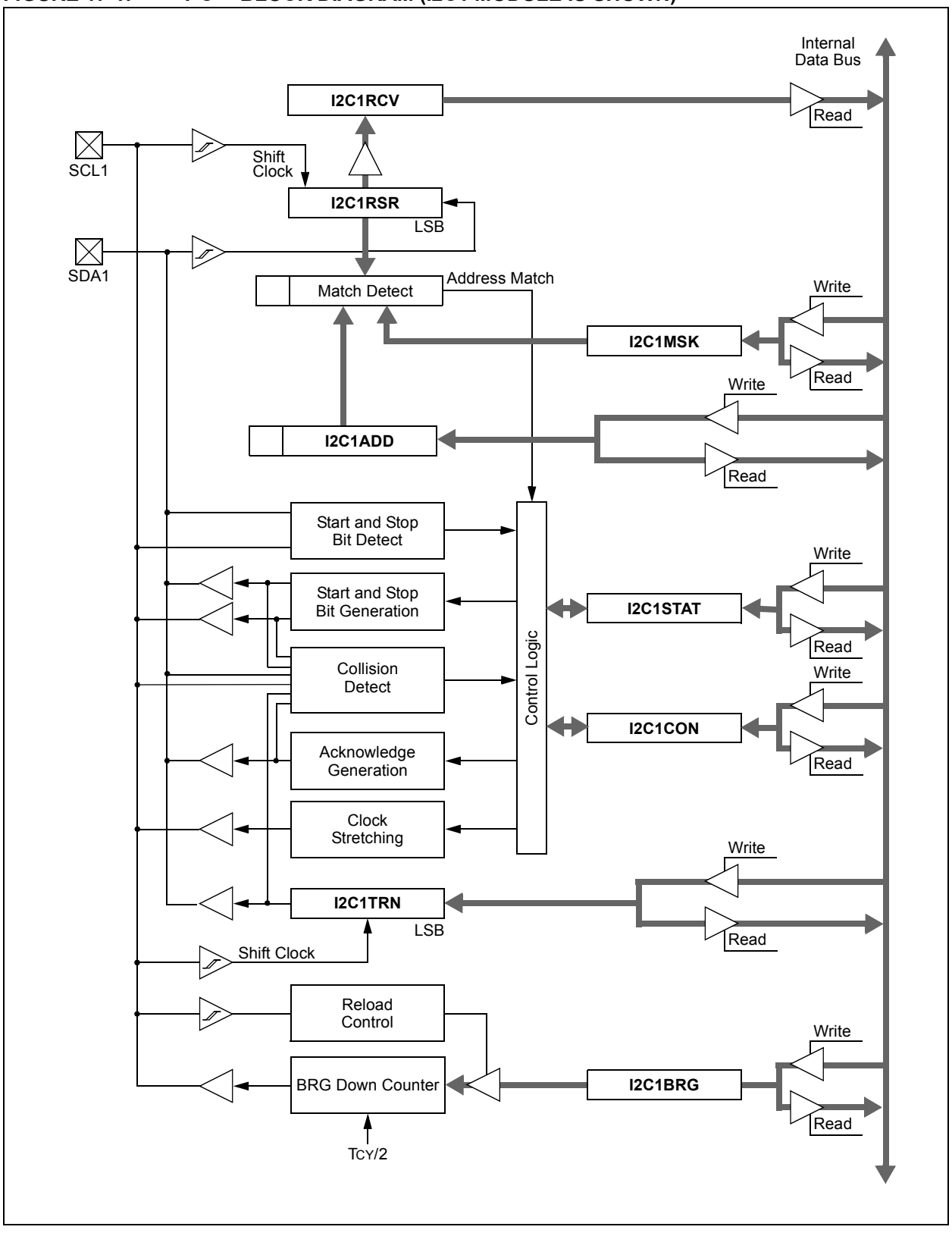
TABLE 16-1: SAMPLE SCKx FREQUENCIES(1,2)

FCY = 16 MHz		Secondary Prescaler Settings				
		1:1	2:1	4:1	6:1	8:1
Primary Prescaler Settings	1:1	Invalid	8000	4000	2667	2000
	4:1	4000	2000	1000	667	500
	16:1	1000	500	250	167	125
	64:1	250	125	63	42	31
FCY = 5 MHz						
Primary Prescaler Settings	1:1	5000	2500	1250	833	625
	4:1	1250	625	313	208	156
	16:1	313	156	78	52	39
	64:1	78	39	20	13	10

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: SCKx frequencies are indicated in kHz.

FIGURE 17-1: I²C™ BLOCK DIAGRAM (I2C1 MODULE IS SHOWN)



REGISTER 19-3: ALCFGRPT: ALARM CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 00h and CHIME = 0)

0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit

1 = Chime is enabled; ARPT<7:0> bits are allowed to roll over from 00h to FFh

0 = Chime is disabled; ARPT<7:0> bits stop once they reach 00h

bit 13-10 **AMASK<3:0>:** Alarm Mask Configuration bits

0000 = Every half second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29th, once every 4 years)
101x = Reserved – do not use
11xx = Reserved – do not use

bit 9-8 **ALRMPTR<1:0>:** Alarm Value Register Window Pointer bits

Points to the corresponding Alarm Value registers when reading the ALRMVALH and ALRMVALL registers. The ALRMPTR<1:0> value decrements on every read or write of ALRMVALH until it reaches '00'.

ALRMVAL<15:8>:
00 = ALRMMIN
01 = ALRMWD
10 = ALRMMNTH
11 = Unimplemented

ALRMVAL<7:0>:
00 = ALRMSEC
01 = ALRMHR
10 = ALRMDAY
11 = Unimplemented

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits

11111111 = Alarm will repeat 255 more times
.
.
.
00000000 = Alarm will not repeat

The counter decrements on any alarm event; it is prevented from rolling over from 00h to FFh unless CHIME = 1.

22.0 12-BIT A/D CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the 12-Bit A/D Converter with Threshold Detect, refer to the *"PIC24F Family Reference Manual"*, **Section 51. "12-Bit A/D Converter with Threshold Detect"** (DS39739).

The PIC24F 12-bit A/D Converter has the following key features:

- Successive Approximation Register (SAR) Conversion
- Conversion Speeds of up to 100 ksps
- Up to 32 Analog Input Channels (Internal and External)
- Multiple Internal Reference Input Channels
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold (S/H) Amplifier
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed-Length (one word per channel), Configurable Conversion Result Buffer
- Four Options for Results Alignment
- Configurable Interrupt Generation
- Operation During CPU Sleep and Idle modes

The 12-bit A/D Converter module is an enhanced version of the 10-bit module offered in some PIC24 devices. Both modules are Successive Approximation Register (SAR) converters at their cores, surrounded by a range of hardware features for flexible configuration. This version of the module extends functionality by providing 12-bit resolution, a wider range of automatic sampling options and tighter integration with other analog modules, such as the CTMU and a configurable results buffer. This module also includes a unique Threshold Detect feature that allows the module itself to make simple decisions based on the conversion results.

A simplified block diagram for the module is illustrated in Figure 22-1.

22.1 A/D Control Registers

The 12-bit A/D Converter module uses up to 43 registers for its operation. All registers are mapped in the data memory space.

22.1.1 CONTROL REGISTERS

Depending on the specific device, the module has up to eleven control and status registers:

- AD1CON1: A/D Control Register 1
- AD1CON2: A/D Control Register 2
- AD1CON3: A/D Control Register 3
- AD1CON5: A/D Control Register 5
- AD1CHS: A/D Sample Select Register
- AD1CHITH and AD1CHITL: A/D Scan Compare Hit Registers
- AD1CSSL and AD1CSSH: A/D Input Scan Select Registers
- AD1CTMUENH and AD1CTMUENL: CTMU Enable Registers

The AD1CON1, AD1CON2 and AD1CON3 registers (Register 22-1, Register 22-2 and Register 22-3) control the overall operation of the A/D module. This includes enabling the module, configuring the conversion clock and voltage reference sources, selecting the sampling and conversion triggers, and manually controlling the sample/convert sequences. The AD1CON5 register (Register 22-4) specifically controls features of the Threshold Detect operation, including its function in power-saving modes.

The AD1CHS register (Register 22-5) selects the input channels to be connected to the S/H amplifier. It also allows the choice of input multiplexers and the selection of a reference source for differential sampling.

The AD1CHITH and AD1CHITL registers (Register 22-6 and Register 22-7) are semaphore registers used with Threshold Detect operations. The status of individual bits, or bit pairs in some cases, indicate if a match condition has occurred. AD1CHITL is always implemented, whereas AD1CHITH may not be implemented in devices with 16 or fewer channels.

The AD1CSSH/L registers (Register 22-8 and Register 22-9) select the channels to be included for sequential scanning.

The AD1CTMUENH/L registers (Register 22-10 and Register 22-11) select the channel(s) to be used by the CTMU during conversions. Selecting a particular channel allows the A/D Converter to control the CTMU (particularly, its current source) and read its data through that channel. AD1CTMUENL is always implemented, whereas AD1CTMUENH may not be implemented in devices with 16 or fewer channels.

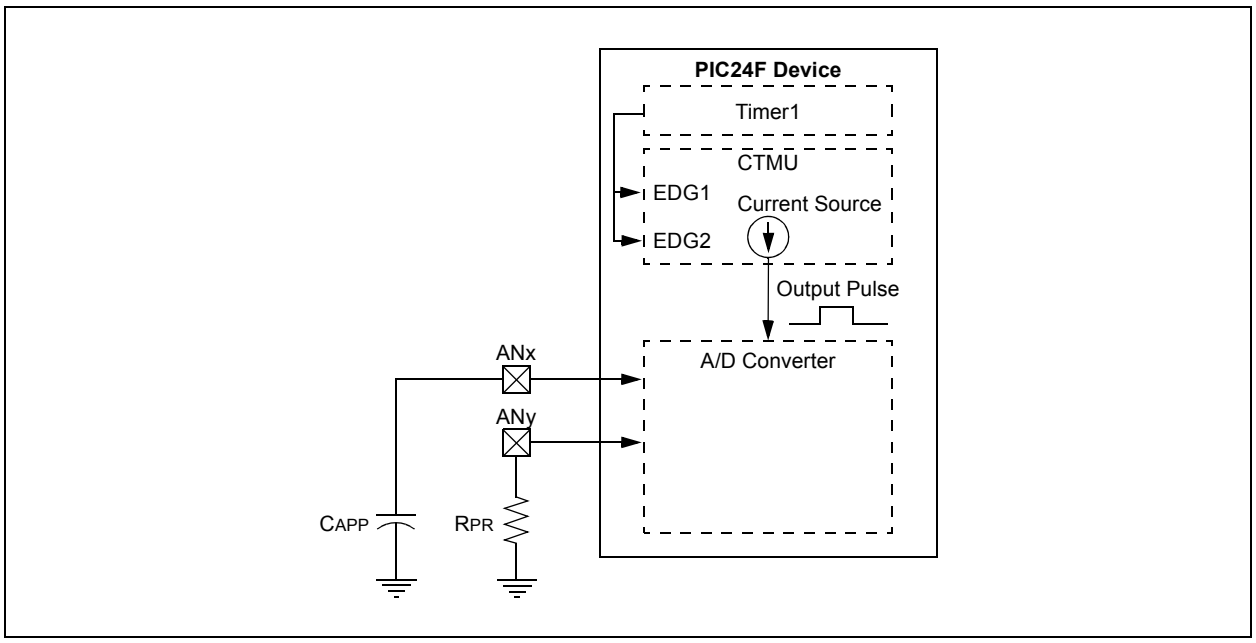
22.1.2 A/D RESULT BUFFERS

The module incorporates a multi-word, dual port RAM, called ADC1BUF. The buffer is composed of at least the same number of word locations as there are external analog channels for a particular device, with a maximum number of 32. The number of buffer addresses is always even. Each of the locations is mapped into the data memory space and is separately addressable. The buffer locations are referred to as ADC1BUF0 through ADC1BUFn (up to 31).

The A/D result buffers are both readable and writable. When the module is active (AD1CON<15> = 1), the buffers are read-only, and store the results of A/D conversions. When the module is inactive (AD1CON<15> = 0), the buffers are both readable and writable. In this state, writing to a buffer location programs a conversion threshold for Threshold Detect operations.

Buffer contents are not cleared when the module is deactivated with the ADON bit (AD1CON1<15>). Conversion results and any programmed threshold values are maintained when ADON is set or cleared.

FIGURE 25-1: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR CAPACITANCE MEASUREMENT



25.2 Measuring Time

Time measurements on the pulse width can be similarly performed using the A/D module's Internal Capacitor (C_{AD}) and a precision resistor for current calibration. Figure 25-2 displays the external connections used for time measurements, and how the CTMU and A/D modules are related in this application. This example also shows both edge events coming from the external CTEDx pins, but other configurations using internal edge sources are possible.

FIGURE 25-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT

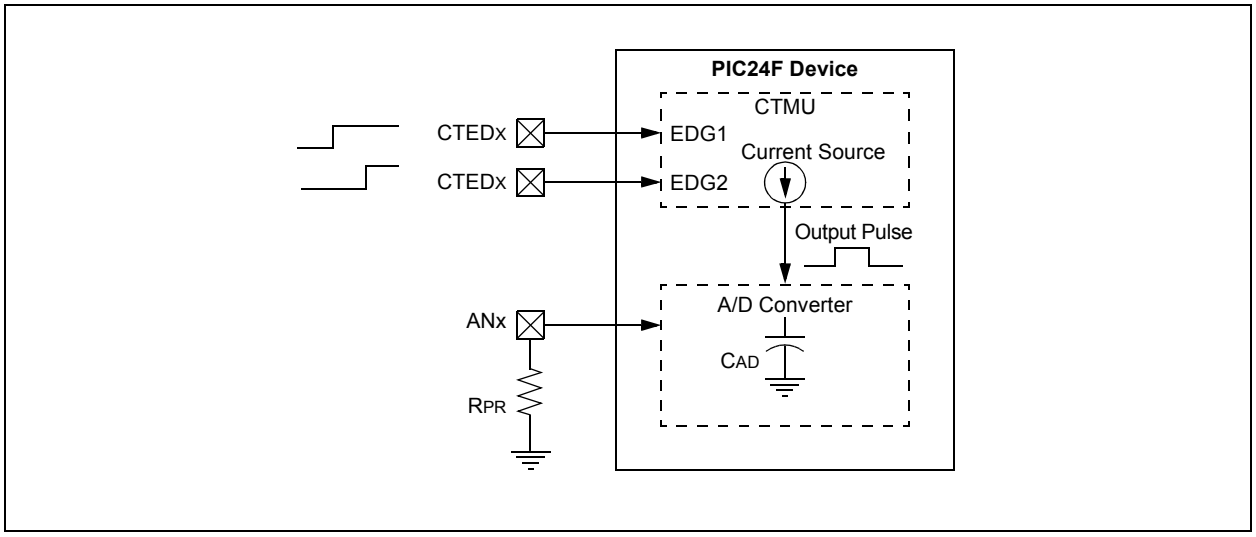


FIGURE 29-8: TIMER1/2/3/4/5 EXTERNAL CLOCK INPUT TIMING

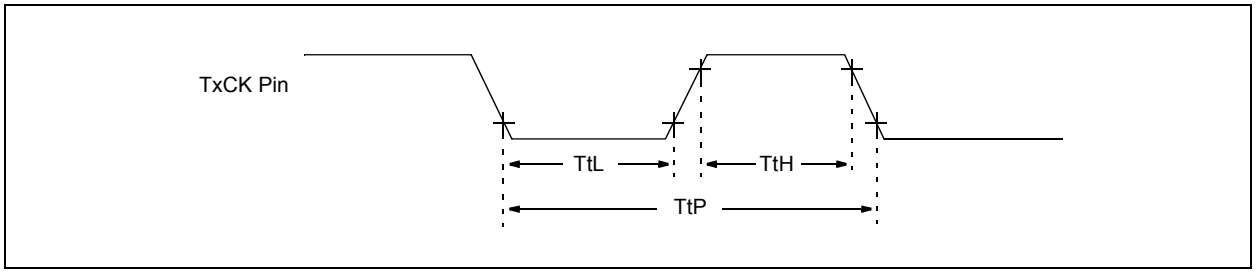


TABLE 29-27: TIMER1/2/3/4/5 EXTERNAL CLOCK INPUT REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
	TtH	TxCK High Pulse Time	Sync w/Prescaler	TCY + 20	—	ns	Must also meet Parameter Ttp
			Async w/Prescaler	10	—	ns	
			Async Counter	20	—	ns	
	TtL	TxCK Low Pulse Time	Sync w/Prescaler	TCY + 20	—	ns	Must also meet Parameter Ttp
			Async w/Prescaler	10	—	ns	
			Async Counter	20	—	ns	
	TtP	TxCK External Input Period	Sync w/Prescaler	2 * TCY + 40	—	ns	N = Prescale Value (1, 4, 8, 16)
			Async w/Prescaler	Greater of: 20 or $\frac{2 * T_{CY} + 40}{N}$	—	ns	
			Async Counter	40	—	ns	
		Delay for Input Edge to Timer Increment	Synchronous	1	2	TCY	
			Asynchronous	—	20	ns	

FIGURE 29-9: INPUT CAPTURE x TIMINGS

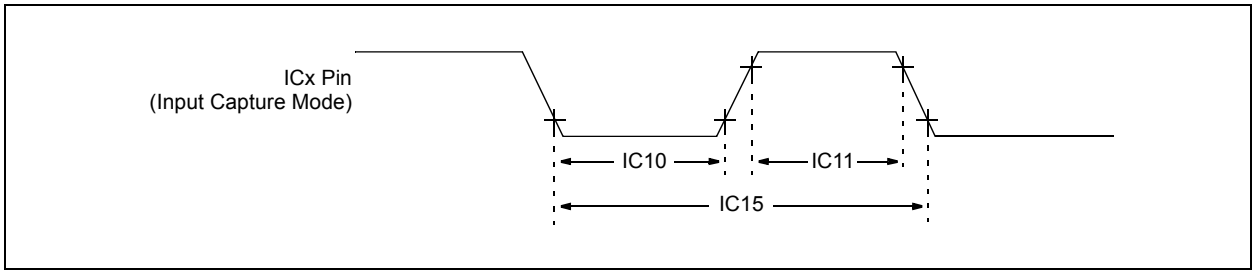


TABLE 29-28: INPUT CAPTURE x REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
IC10	TccL	ICx Input Low Time – Synchronous Timer	No Prescaler	TCY + 20	—	ns	Must also meet Parameter IC15
			With Prescaler	20	—	ns	
IC11	TccH	ICx Input Low Time – Synchronous Timer	No Prescaler	TCY + 20	—	ns	Must also meet Parameter IC15
			With Prescaler	20	—	ns	
IC15	TccP	ICx Input Period – Synchronous Timer		$\frac{2 * T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4, 16)

FIGURE 30-16: TYPICAL AND MAXIMUM IPD vs. VDD (DEEP SLEEP MODE)

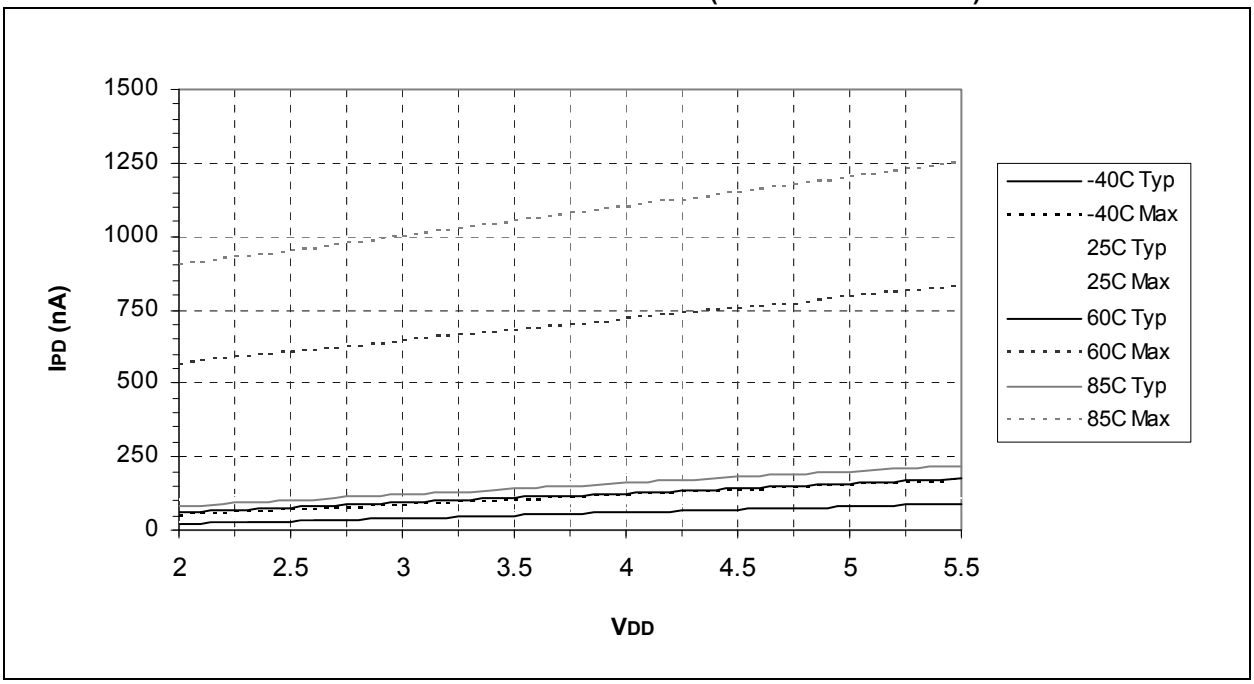
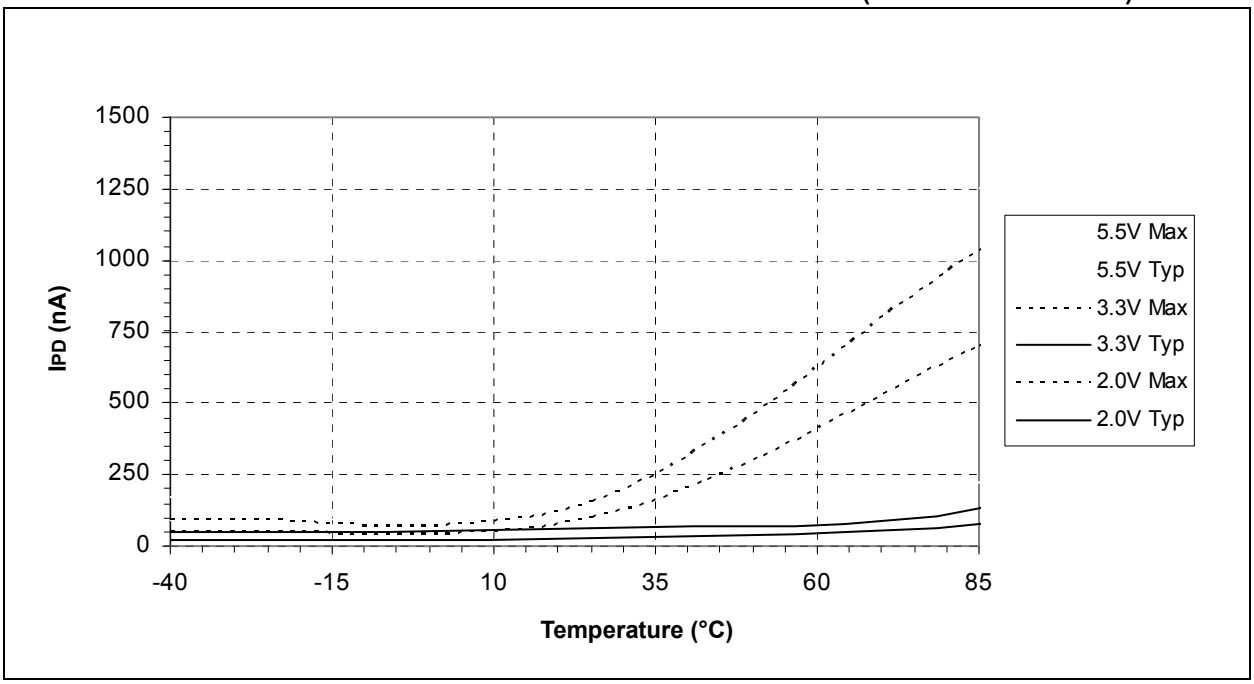
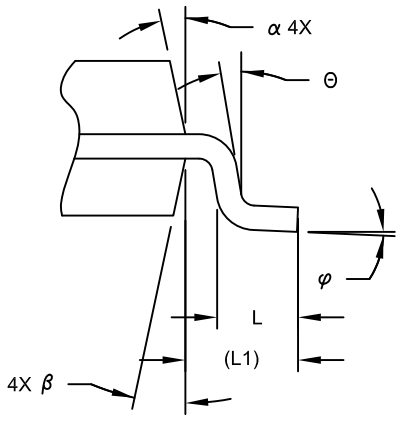


FIGURE 30-17: TYPICAL AND MAXIMUM IPD vs. TEMPERATURE (DEEP SLEEP MODE)

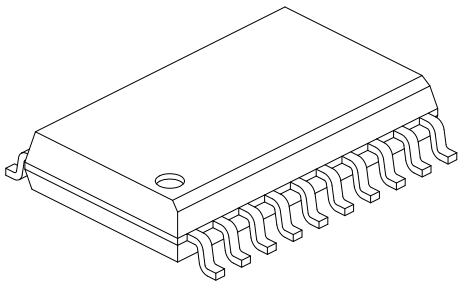


20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		12.80 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

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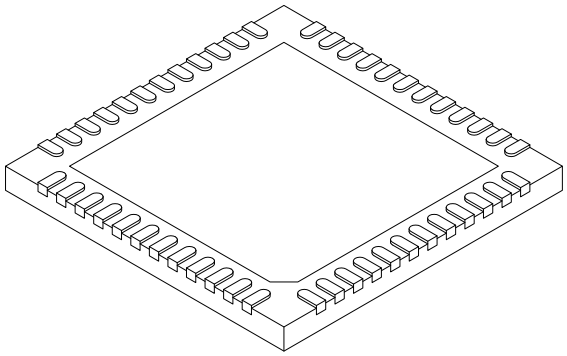
48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.45	4.60	4.75
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.45	4.60	4.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2