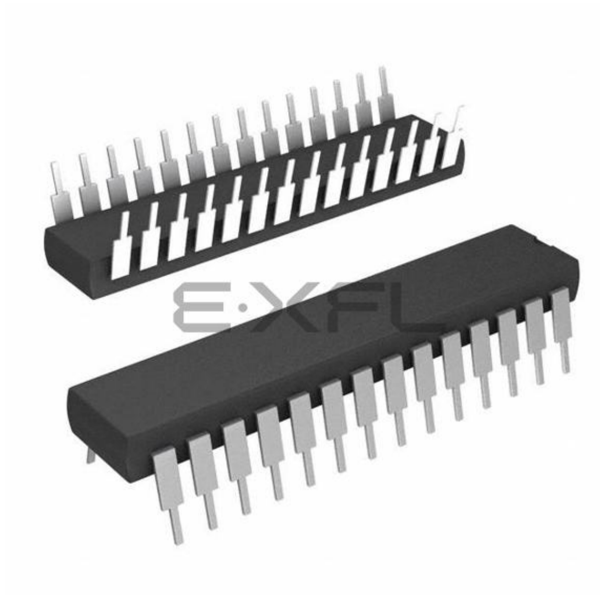

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f32ka302-i-sp

TABLE 1-3: PIC24FV32KA304 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	F Pin Number					FV Pin Number					I/O	Buffer	Description
	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
RA0	2	2	27	19	21	2	2	27	19	21	I/O	ST	PORTA Pins
RA1	3	3	28	20	22	3	3	28	20	22	I/O	ST	
RA2	7	9	6	30	33	7	9	6	30	33	I/O	ST	
RA3	8	10	7	31	34	8	10	7	31	34	I/O	ST	
RA4	10	12	9	34	37	10	12	9	34	37	I/O	ST	
RA5	1	1	26	18	19	1	1	26	18	19	I/O	ST	
RA6	14	20	17	7	7	—	—	—	—	—	I/O	ST	
RA7	—	19	16	6	6	—	19	16	6	6	I/O	ST	
RA8	—	—	—	32	35	—	—	—	32	35	I/O	ST	
RA9	—	—	—	35	38	—	—	—	35	38	I/O	ST	
RA10	—	—	—	12	13	—	—	—	12	13	I/O	ST	
RA11	—	—	—	13	14	—	—	—	13	14	I/O	ST	
RB0	4	4	1	21	23	4	4	1	21	23	I/O	ST	PORTB Pins
RB1	5	5	2	22	24	5	5	2	22	24	I/O	ST	
RB2	6	6	3	23	25	6	6	3	23	25	I/O	ST	
RB3	—	7	4	24	26	—	7	4	24	26	I/O	ST	
RB4	9	11	8	33	36	9	11	8	33	36	I/O	ST	
RB5	—	14	11	41	45	—	14	11	41	45	I/O	ST	
RB6	—	15	12	42	46	—	15	12	42	46	I/O	ST	
RB7	11	16	13	43	47	11	16	13	43	47	I/O	ST	
RB8	12	17	14	44	48	12	17	14	44	48	I/O	ST	
RB9	13	18	15	1	1	13	18	15	1	1	I/O	ST	
RB10	—	21	18	8	9	—	21	18	8	9	I/O	ST	
RB11	—	22	19	9	10	—	22	19	9	10	I/O	ST	
RB12	15	23	20	10	11	15	23	20	10	11	I/O	ST	
RB13	16	24	21	11	12	16	24	21	11	12	I/O	ST	
RB14	17	25	22	14	15	17	25	22	14	15	I/O	ST	
RB15	18	26	23	15	16	18	26	23	15	16	I/O	ST	

EXAMPLE 5-4: LOADING THE WRITE BUFFERS – ‘C’ LANGUAGE CODE

```
// C example using MPLAB C30

   #define NUM_INSTRUCTION_PER_ROW 64
   int __attribute__ ((space(auto_psv))) progAddr = 0x1234;  // Global variable located in Pgm Memory
   unsigned int offset;
   unsigned int i;
   unsigned int progData[2*NUM_INSTRUCTION_PER_ROW];        // Buffer of data to write

   //Set up NVMCON for row programming
   NVMCON = 0x4001;                                         // Initialize NVMCON

   //Set up pointer to the first memory location to be written
   TBLPAG = __builtin_tblpage(&progAddr);                   // Initialize PM Page Boundary SFR
   offset = __builtin_tbloffset(&progAddr);                 // Initialize lower word of address

   //Perform TBLWT instructions to write necessary number of latches
   for(i=0; i < 2*NUM_INSTRUCTION_PER_ROW; i++)
   {
       __builtin_tblwtl(offset, progData[i++]);             // Write to address low word
       __builtin_tblwth(offset, progData[i]);               // Write to upper byte
       offset = offset + 2;                                 // Increment address
   }
```

EXAMPLE 5-5: INITIATING A PROGRAMMING SEQUENCE – ASSEMBLY LANGUAGE CODE

```
        DISI    #5                          ; Block all interrupts
                                              for next 5 instructions
        MOV     #0x55, W0
        MOV     W0, NVMKEY                  ; Write the 55 key
        MOV     #0xAA, W1                   ;
        MOV     W1, NVMKEY                  ; Write the AA key
        BSET    NVMCON, #WR                 ; Start the erase sequence
        NOP                                 ; 2 NOPs required after setting WR
        NOP                                 ;
        BTSC    NVMCON, #15                 ; Wait for the sequence to be completed
        BRA     $-2                         ;
```

EXAMPLE 5-6: INITIATING A PROGRAMMING SEQUENCE – ‘C’ LANGUAGE CODE

```
// C example using MPLAB C30

asm("DISI #5");              // Block all interrupts for next 5 instructions

__builtin_write_NVM();       // Perform unlock sequence and set WR
```

6.4.1.1 Data EEPROM Bulk Erase

To erase the entire data EEPROM (bulk erase), the address registers do not need to be configured because this operation affects the entire data EEPROM. The following sequence helps in performing a bulk erase:

1. Configure NVMCON to Bulk Erase mode.
2. Clear the NVMIF status bit and enable the NVM interrupt (optional).
3. Write the key sequence to NVMKEY.
4. Set the WR bit to begin the erase cycle.
5. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical bulk erase sequence is provided in Example 6-3.

6.4.2 SINGLE-WORD WRITE

To write a single word in the data EEPROM, the following sequence must be followed:

1. Erase one data EEPROM word (as mentioned in the previous section) if the PGMONLY bit (NVMCON<12>) is set to '1'.
2. Write the data word into the data EEPROM latch.
3. Program the data word into the EEPROM:
   - Configure the NVMCON register to program one EEPROM word (NVMCON<5:0> = 0001xx).
   - Clear the NVMIF status bit and enable the NVM interrupt (optional).
   - Write the key sequence to NVMKEY.
   - Set the WR bit to begin the erase cycle.
   - Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).
   - To get cleared, wait until NVMIF is set.

A typical single-word write sequence is provided in Example 6-4.

EXAMPLE 6-3: DATA EEPROM BULK ERASE

```
    // Set up NVMCON to bulk erase the data EEPROM
    NVMCON = 0x4050;

    // Disable Interrupts For 5 Instructions
    asm volatile ("disi #5");

    // Issue Unlock Sequence and Start Erase Cycle
    __builtin_write_NVM();
```

EXAMPLE 6-4: SINGLE-WORD WRITE TO DATA EEPROM

```
int __attribute__ ((space(eedata))) eeData = 0x1234;
   int newData;                                       // New data to write to EEPROM
/*---------------------------------------------------------------------------------------------
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the write
-----------------------------------------------------------------------------------------------
*/
   unsigned int offset;

   // Set up NVMCON to erase one word of data EEPROM
   NVMCON = 0x4004;

   // Set up a pointer to the EEPROM location to be erased
   TBLPAG = __builtin_tblpage(&eeData);               // Initialize EE Data page pointer
   offset = __builtin_tbloffset(&eeData);             // Initizlize lower word of address
   __builtin_tblwtl(offset, newData);                 // Write EEPROM data to write latch

   asm volatile ("disi #5");                          // Disable Interrupts For 5 Instructions
   __builtin_write_NVM();                             // Issue Unlock Sequence & Start Write Cycle
   while(NVMCONbits.WR=1);                            // Optional: Poll WR bit to wait for
                                                      // write sequence to complete
```

REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER2

R/W-0	R-0, HSC	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Uses Alternate Interrupt Vector Table (AIVT)
0 = Uses standard (default) Interrupt Vector Table (IVT)

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as ‘0’

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

11111 = This output compare module(1)
11110 = Reserved
11101 = Reserved
11100 = CTMU(2)
11011 = A/D(2)
11010 = Comparator 3(2)
11001 = Comparator 2(2)
11000 = Comparator 1(2)
10111 = Input Capture 4(2)
10110 = Input Capture 3(2)
10101 = Input Capture 2(2)
10100 = Input Capture 1(2)
100xx = Reserved
01111 = Timer5
01110 = Timer4
01101 = Timer3
01100 = Timer2
01011 = Timer1
01010 = Input Capture 5(2)
01001 = Reserved
01000 = Reserved
00111 = Reserved
00110 = Reserved
00101 = Output Compare 5(1)
00100 = Output Compare 4(1)
00011 = Output Compare 3(1)
00010 = Output Compare 2(1)
00001 = Output Compare 1(1)
00000 = Not synchronized to any other module

Note 1: Do not use an output compare module as its own trigger source, either by selecting this mode or another equivalent SYNCSELx setting.

2: Use these inputs as trigger sources only and never as Sync sources.

3: These bits affect the rising edge when OCINV = 1. The bits have no effect when the OCMx bits (OCxCON1<2:0>) = 001.

REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)
11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).

REGISTER 16-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	SPIFPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SPIFE	SPIBEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FRMEN:** Framed SPIx Support bit
1 = Framed SPIx support is enabled
0 = Framed SPIx support is disabled

bit 14 **SPIFSD:** SPIx Frame Sync Pulse Direction Control on $\overline{SSx}$ Pin bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 13 **SPIFPOL:** SPIx Frame Sync Pulse Polarity bit (Frame mode only)
1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **SPIFE:** SPIx Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse coincides with the first bit clock
0 = Frame Sync pulse precedes the first bit clock

bit 0 **SPIBEN:** SPIx Enhanced Buffer Enable bit
1 = Enhanced buffer is enabled
0 = Enhanced buffer is disabled (Legacy mode)

REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 5	**ACKDT:** Acknowledge Data bit (when operating as I^{2}C master; applicable during master receive) Value that will be transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	**ACKEN:** Acknowledge Sequence Enable bit (when operating as I^{2}C master; applicable during master receive) 1 = Initiates the Acknowledge sequence on the SDAx and SCLx pins, and transmits the ACKDT data bit; hardware is clear at the end of the master Acknowledge sequence 0 = Acknowledge sequence is not in progress
bit 3	**RCEN:** Receive Enable bit (when operating as I^{2}C master) 1 = Enables Receive mode for I^{2}C; hardware is clear at the end of the eighth bit of the master receive data byte 0 = Receive sequence is not in progress
bit 2	**PEN:** Stop Condition Enable bit (when operating as I^{2}C master) 1 = Initiates Stop condition on SDAx and SCLx pins; hardware is clear at end of master Stop sequence 0 = Stop condition is not in progress
bit 1	**RSEN:** Repeated Start Condition Enable bit (when operating as I^{2}C master) 1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Repeated Start sequence 0 = Repeated Start condition is not in progress
bit 0	**SEN:** Start Condition Enable bit (when operating as I^{2}C master) 1 = Initiates Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Start sequence 0 = Start condition is not in progress

19.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Real-Time Clock and Calendar, refer to the *"PIC24F Family Reference Manual"*, **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS39696).

The RTCC provides the user with a Real-Time Clock and Calendar (RTCC) function that can be calibrated.

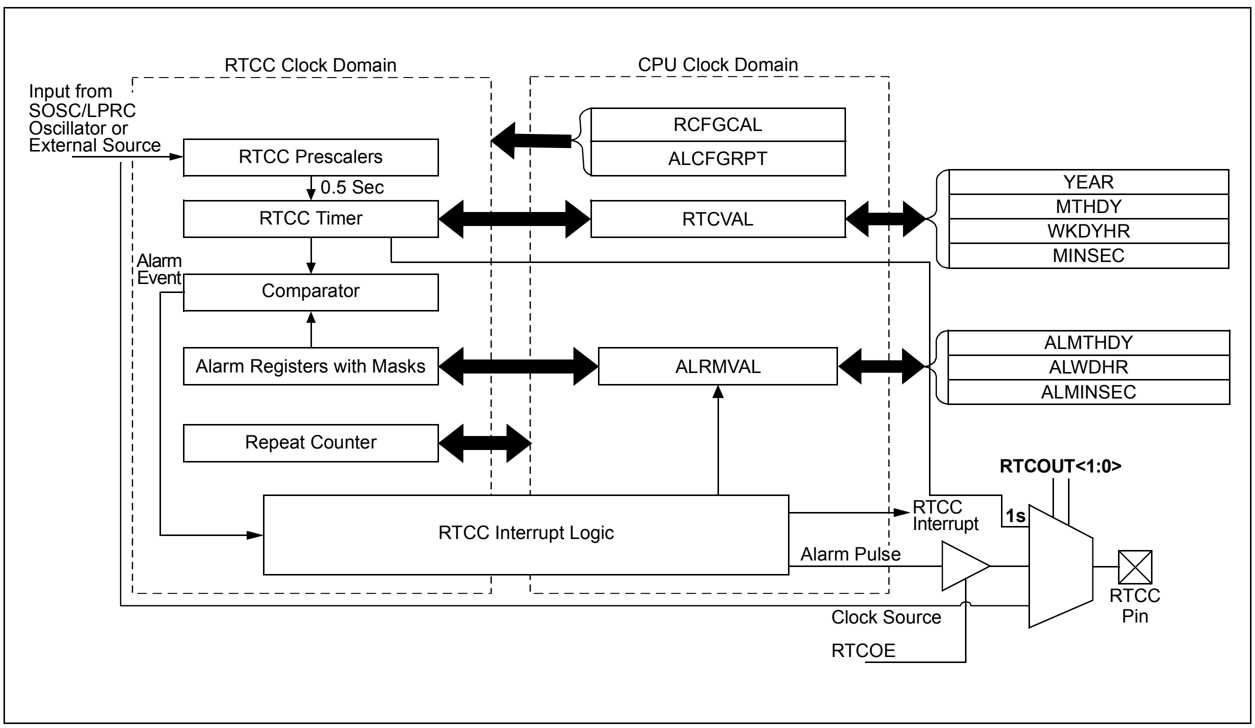
Key features of the RTCC module are:

- Operates in Deep Sleep mode
- Selectable clock source
- Provides hours, minutes and seconds using 24-hour format
- Visibility of one half second period
- Provides calendar – weekday, date, month and year
- Alarm-configurable for half a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month or one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat chime
- Year 2000 to 2099 leap year correction
- BCD format for smaller software overhead
- Optimized for long-term battery operation
- User calibration of the 32.768 kHz clock crystal/32K INTRC frequency with periodic auto-adjust
- Optimized for long-term battery operation
- Fractional second synchronization
- Calibration to within ±2.64 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Ability to periodically wake-up external devices without CPU intervention (external power control)
- Power control output for external circuit control
- Calibration takes effect every 15 seconds
- Runs from any one of the following:
  - External Real-Time Clock of 32.768 kHz
  - Internal 31.25 kHz LPRC Clock
  - 50 Hz or 60 Hz External Input

19.1 RTCC Source Clock

The user can select between the SOSC crystal oscillator, LPRC internal oscillator or an external 50 Hz/60 Hz power line input as the clock reference for the RTCC module. This gives the user an option to trade off system cost, accuracy and power consumption, based on the overall system needs.

FIGURE 19-1: RTCC BLOCK DIAGRAM



REGISTER 19-3: ALCFGRPT: ALARM CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 00h and CHIME = 0)
0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit
1 = Chime is enabled; ARPT<7:0> bits are allowed to roll over from 00h to FFh
0 = Chime is disabled; ARPT<7:0> bits stop once they reach 00h

bit 13-10 **AMASK<3:0>:** Alarm Mask Configuration bits
0000 = Every half second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29th, once every 4 years)
101x = Reserved – do not use
11xx = Reserved – do not use

bit 9-8 **ALRMPTR<1:0>:** Alarm Value Register Window Pointer bits
Points to the corresponding Alarm Value registers when reading the ALRMVALH and ALRMVALL registers. The ALRMPTR<1:0> value decrements on every read or write of ALRMVALH until it reaches ‘00’.
ALRMVAL<15:8>:
00 = ALRMMIN
01 = ALRMWD
10 = ALRMMNTH
11 = Unimplemented
ALRMVAL<7:0>:
00 = ALRMSEC
01 = ALRMHR
10 = ALRMDAY
11 = Unimplemented

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits
11111111 = Alarm will repeat 255 more times
.
.
.
00000000 = Alarm will not repeat
The counter decrements on any alarm event; it is prevented from rolling over from 00h to FFh unless CHIME = 1.

19.2.5 RTCVAL REGISTER MAPPINGS

REGISTER 19-4: YEAR: YEAR VALUE REGISTER[(1)]

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN2	YRTEN1	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year’s Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 19-5: MTHDY: MONTH AND DAY VALUE REGISTER[(1)]

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month’s Tens Digit bit
Contains a value of ‘0’ or ‘1’.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month’s Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day’s Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 19-10: ALMINSEC: ALARM MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15	**Unimplemented:** Read as ‘0’
bit 14-12	**MINTEN<2:0>:** Binary Coded Decimal Value of Minute’s Tens Digit bits Contains a value from 0 to 5.
bit 11-8	**MINONE<3:0>:** Binary Coded Decimal Value of Minute’s Ones Digit bits Contains a value from 0 to 9.
bit 7	**Unimplemented:** Read as ‘0’
bit 6-4	**SECTEN<2:0>:** Binary Coded Decimal Value of Second’s Tens Digit bits Contains a value from 0 to 5.
bit 3-0	**SECONE<3:0>:** Binary Coded Decimal Value of Second’s Ones Digit bits Contains a value from 0 to 9.

REGISTER 19-11: RTCCSWT: CONTROL/SAMPLE WINDOW TIMER REGISTER(1)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PWCSTAB7	PWCSTAB6	PWCSTAB5	PWCSTAB4	PWCSTAB3	PWCSTAB2	PWCSTAB1	PWCSTAB0
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PWCSAMP7	PWCSAMP6	PWCSAMP5	PWCSAMP4	PWCSAMP3	PWCSAMP2	PWCSAMP1	PWCSAMP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **PWCSTAB<7:0>:** PWM Stability Window Timer bits
11111111 = Stability window is 255 TPWCCLK clock periods
.
.
.
00000000 = Stability window is 0 TPWCCLK clock periods
The sample window starts when the alarm event triggers. The stability window timer starts counting from every alarm event when PWCEN = 1.

bit 7-0 **PWCSAMP<7:0>:** PWM Sample Window Timer bits
11111111 = Sample window is always enabled, even when PWCEN = 0
11111110 = Sample window is 254 TPWCCLK clock periods
.
.
.
00000000 = Sample window is 0 TPWCCLK clock periods
The sample window timer starts counting at the end of the stability window when PWCEN = 1. If PWCSTAB<7:0> = 00000000, the sample window timer starts counting from every alarm event when PWCEN = 1.

Note 1: A write to this register is only allowed when RTCWREN = 1.

24.0 COMPARATOR VOLTAGE REFERENCE

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator Voltage Reference, refer to the *"PIC24F Family Reference Manual"*, **Section 20. "Comparator Module Voltage Reference Module"** (DS39709).

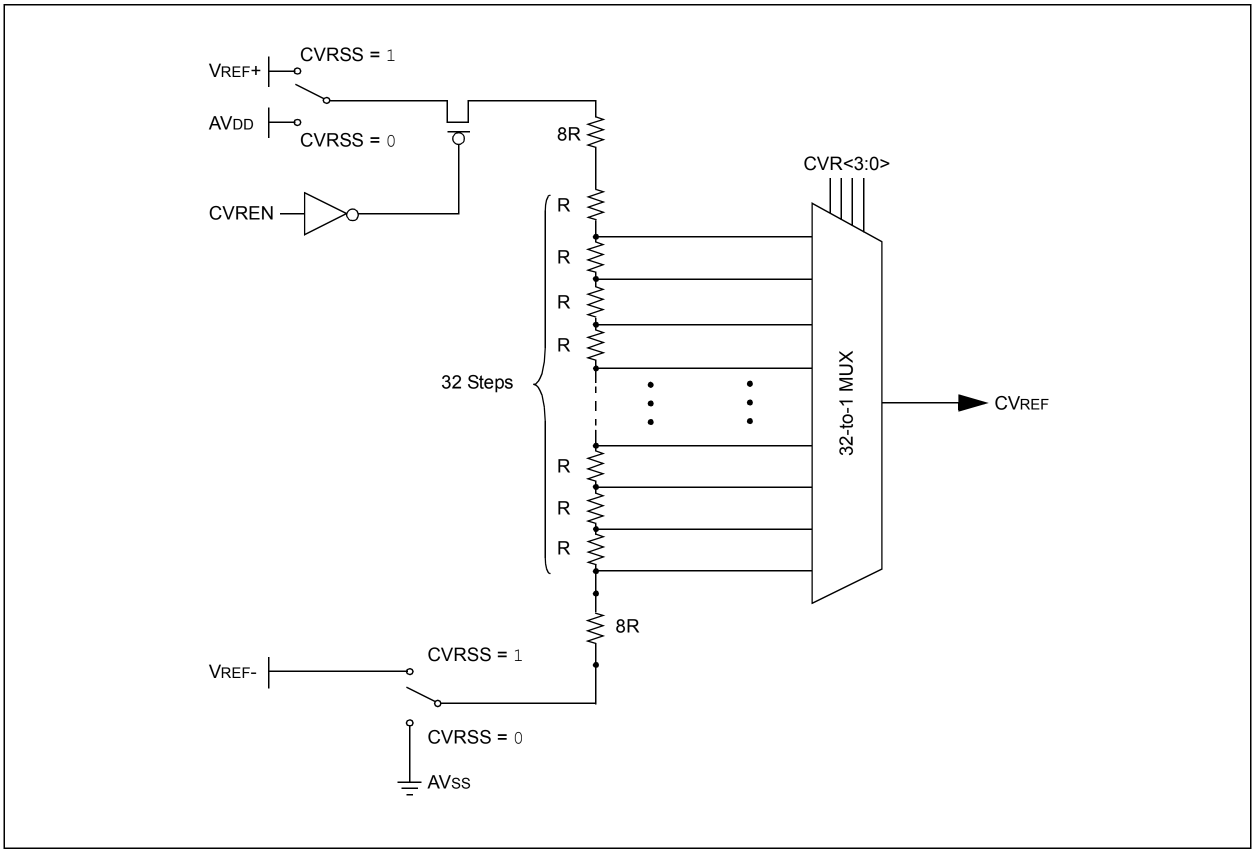
24.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRCON register (Register 24-1). The comparator voltage reference provides a range of output voltages, with 32 distinct levels.

The comparator voltage reference supply voltage can come from either VDD and VSS or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON<5>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 24-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



REGISTER 25-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = Edge 1 source is Comparator 3 output
1110 = Edge 1 source is Comparator 2 output
1101 = Edge 1 source is Comparator 1 output
1100 = Edge 1 source is IC3
1011 = Edge 1 source is IC2
1010 = Edge 1 source is IC1
1001 = Edge 1 source is CTED8
1000 = Edge 1 source is CTED7
0111 = Edge 1 source is CTED6
0110 = Edge 1 source is CTED5
0101 = Edge 1 source is CTED4
0100 = Edge 1 source is CTED3(2)
0011 = Edge 1 source is CTED1
0010 = Edge 1 source is CTED2
0001 = Edge 1 source is OC1
0000 = Edge 1 source is Timer1

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the current source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the current source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

Note 1: Edge sources, CTED11 and CTED12, are not available on PIC24FV32KA302 devices.
2: Edge sources, CTED3, CTED11, CTED12 and CTED13, are not available on PIC24FV32KA301 devices.

REGISTER 25-3: CTMUICON: CTMU CURRENT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
.
.
.
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
.
.
.
100010
100001 = Maximum negative change from nominal current

bit 9-8 **IRNG<1:0>:** Current Source Range Select bits
11 = 100 × Base Current
10 = 10 × Base Current
01 = Base Current Level (0.55 μA nominal)
00 = 1000 × Base Current

bit 7-0 **Unimplemented:** Read as ‘0’

TABLE 29-4: HIGH/LOW–VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0000(2)	—	—	1.90	V	
			HLVDL<3:0> = 0001	1.86	—	2.13	V	
			HLVDL<3:0> = 0010	2.08	—	2.35	V	
			HLVDL<3:0> = 0011	2.22	—	2.53	V	
			HLVDL<3:0> = 0100	2.30	—	2.62	V	
			HLVDL<3:0> = 0101	2.49	—	2.84	V	
			HLVDL<3:0> = 0110	2.73	—	3.10	V	
			HLVDL<3:0> = 0111	2.86	—	3.25	V	
			HLVDL<3:0> = 1000	3.00	—	3.41	V	
			HLVDL<3:0> = 1001	3.16	—	3.59	V	
			HLVDL<3:0> = 1010(1)	3.33	—	3.79	V	
			HLVDL<3:0> = 1011(1)	3.53	—	4.01	V	
			HLVDL<3:0> = 1100(1)	3.74	—	4.26	V	
			HLVDL<3:0> = 1101(1)	4.00	—	4.55	V	
			HLVDL<3:0> = 1110(1)	4.28	—	4.87	V	

Note 1: These trip points should not be used on PIC24FXXKA30X devices.
2: This trip point should not be used on PIC24FVXXKA30X devices.

TABLE 29-5: BOR TRIP POINTS

Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended								
Param No.	**Sym**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC15		BOR Hysteresis		—	5	—	mV	
DC19		BOR Voltage on VDD Transition	BORV<1:0> = 00	—	—	—	—	Valid for LPBOR and DSBOR (**Note 1**)
			BORV<1:0> = 01	2.90	3	3.38	V	
			BORV<1:0> = 10	2.53	2.7	3.07	V	
			BORV<1:0> = 11	1.75	1.85	2.05	V	**(Note 2)**
			BORV<1:0> = 11	1.95	2.05	2.16	V	**(Note 3)**

Note 1: LPBOR re-arms the POR circuit but does not cause a BOR.
2: This is valid for PIC24F (3.3V) devices.
3: This is valid for PIC24FV (5V) devices.

TABLE 29-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ[(1)]**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage[(4)]**					
DI10		I/O Pins	VSS	—	0.2 VDD	V	
DI15		$\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI16		OSCI (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSCI (HS mode)	VSS	—	0.2 VDD	V	
DI18		I/O Pins with I^2C™ Buffer	VSS	—	0.3 VDD	V	SMBus is disabled
DI19		I/O Pins with SMBus Buffer	VSS	—	0.8	V	SMBus is enabled
	VIH	**Input High Voltage[(4)]**					
DI20		I/O Pins:					
		with Analog Functions	0.8 VDD	—	VDD	V	
		Digital Only	0.8 VDD	—	VDD	V	
DI25		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
DI26		OSCI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSCI (HS mode)	0.7 VDD	—	VDD	V	
DI28		I/O Pins with I^2C Buffer:					
		with Analog Functions	0.7 VDD	—	VDD	V	
		Digital Only	0.7 VDD	—	VDD	V	
DI29		I/O Pins with SMBus	2.1	—	VDD	V	2.5V ≤ VPIN ≤ VDD
DI30	ICNPU	**CNx Pull-up Current**	50	250	500	μA	VDD = 3.3V, VPIN = VSS
	IIL	**Input Leakage Current[(2,3)]**					
DI50		I/O Ports	—	0.05	0.1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{\text{MCLR}}$	—	—	0.1	μA	VSS ≤ VPIN ≤ VDD
DI56		OSCI	—	—	5	μA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Refer to Table 1-3 for I/O pin buffer types.

FIGURE 29-10: OUTPUT COMPARE x TIMINGS

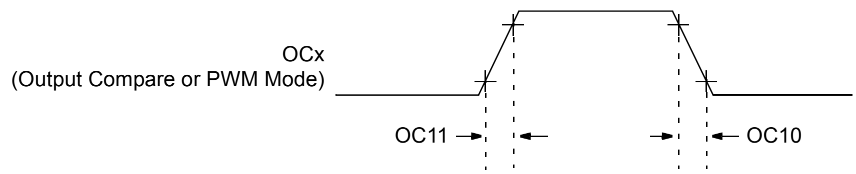


TABLE 29-29: OUTPUT CAPTURE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
OC11	TCCR	OC1 Output Rise Time	—	10	ns	
			—	—	ns	
OC10	TCCF	OC1 Output Fall Time	—	10	ns	
			—	—	ns	

FIGURE 29-11: PWM MODULE TIMING REQUIREMENTS

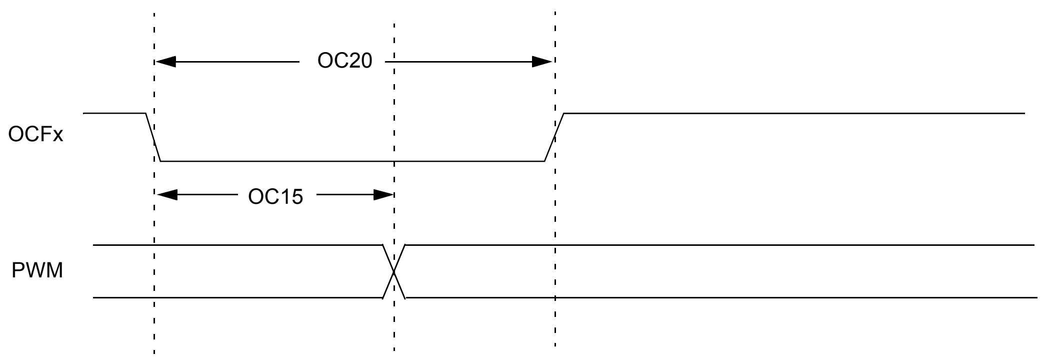


TABLE 29-30: PWM TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	25	ns	VDD = 3.0V, -40°C to +125°C
OC20	TFH	Fault Input Pulse Width	50	—	—	ns	VDD = 3.0V, -40°C to +125°C

† Data in “Typ” column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 29-14: I²C™ BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

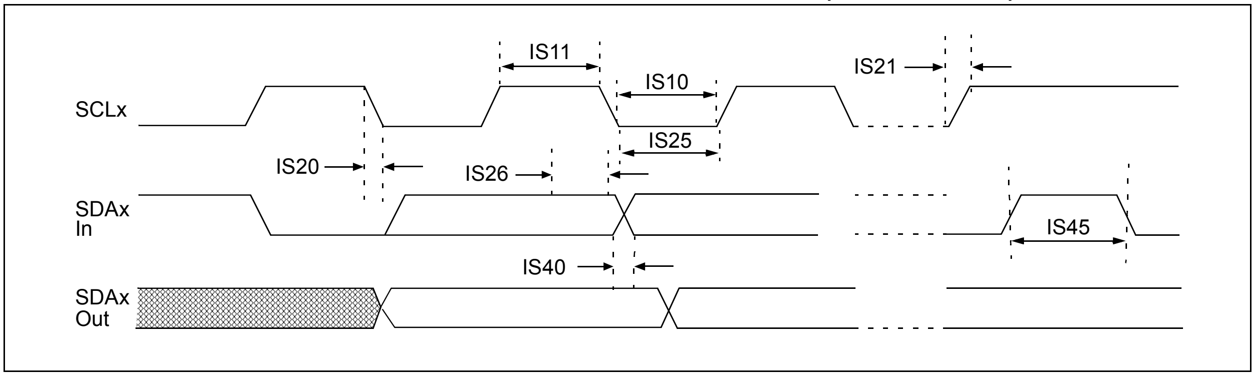


TABLE 29-33: I²C™ BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C (Industrial) -40°C ≤ TA ≤ +125°C (Extended)			
Param No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	μs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	μs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
			1 MHz mode(1)	0	0.3	μs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode(1)	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I²C™ pins (for 1 MHz mode only).

FIGURE 29-19: SPIx MODULE MASTER MODE TIMING CHARACTERISTICS (CKE = 1)

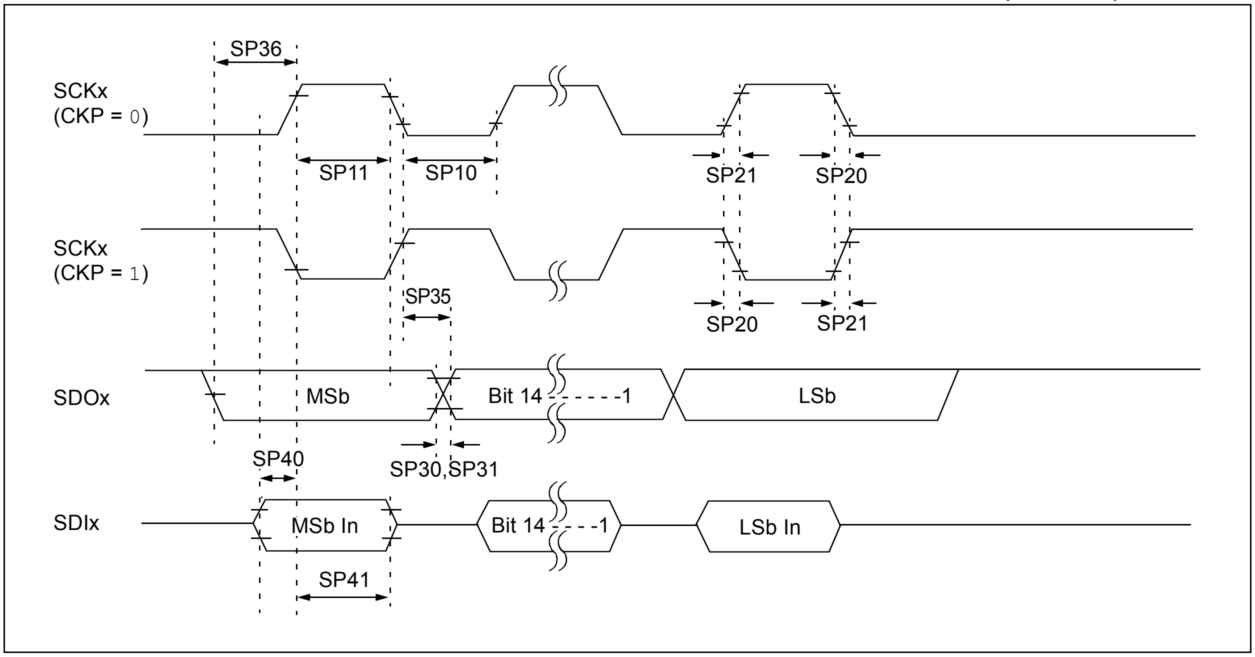


TABLE 29-37: SPIx MODULE MASTER MODE TIMING REQUIREMENTS (CKE = 1)

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(2)	TCY/2	—	—	ns	
SP11	TscH	SCKx Output High Time(2)	TCY/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(3)	—	10	25	ns	
SP21	TscR	SCKx Output Rise Time(3)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(3)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(3)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns; therefore, the clock generated in Master mode must not violate this specification.

3: This assumes a 50 pF load on all SPIx pins.