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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f32ka304-i-ml

TABLE 4-4: ICN REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNPD1	0056	CN15PDE ⁽¹⁾	CN14PDE	CN13PDE	CN12PDE	CN11PDE	CN10PDE ^(1,2)	CN9PDE ⁽¹⁾	CN8PDE ⁽³⁾	CN7PDE ⁽¹⁾	CN6PDE	CN5PDE	CN4PDE	CN3PDE	CN2PDE	CN1PDE	CN0PDE	0000
CNPD2	0058	CN31PDE ^(1,2)	CN30PDE	CN29PDE	CN28PDE ^(1,2)	CN27PDE ⁽¹⁾	CN26PDE ^(1,2)	CN25PDE ^(1,2)	CN24PDE ⁽¹⁾	CN23PDE	CN22PDE	CN21PDE	CN20PDE ^(1,2)	CN19PDE ^(1,2)	CN18PDE ^(1,2)	CN17PDE ^(1,2)	CN16PDE ⁽¹⁾	0000
CNPD3	005A	—	—	—	—	—	—	—	—	—	—	—	CN36PDE ^(1,2)	CN35PDE ^(1,2)	CN34PDE ^(1,2)	CN33PDE ^(1,2)	CN32PDE ^(1,2)	0000
CNEN1	0062	CN15IE ⁽¹⁾	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE ^(1,2)	CN9IE ⁽¹⁾	CN8IE ⁽³⁾	CN7IE ⁽¹⁾	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0064	CN31IE ^(1,2)	CN30IE	CN29IE	CN28IE ^(1,2)	CN27IE ⁽¹⁾	CN26IE ^(1,2)	CN25IE ^(1,2)	CN24IE ⁽¹⁾	CN23IE	CN22IE	CN21IE	CN20IE ^(1,2)	CN19IE ^(1,2)	CN18IE ^(1,2)	CN17IE ^(1,2)	CN16IE ⁽¹⁾	0000
CNEN3	0066	—	—	—	—	—	—	—	—	—	—	—	CN36IE ^(1,2)	CN35IE ^(1,2)	CN34IE ^(1,2)	CN33IE ^(1,2)	CN32IE ^(1,2)	0000
CNPU1	006E	CN15PUE ⁽¹⁾	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE ^(1,2)	CN9PUE ⁽¹⁾	CN8PUE ⁽³⁾	CN7PUE ⁽¹⁾	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	0070	CN31PUE ^(1,2)	CN30PUE	CN29PUE	CN28PUE ^(1,2)	CN27PUE ⁽¹⁾	CN26PUE ^(1,2)	CN25PUE ^(1,2)	CN24PUE ⁽¹⁾	CN23PUE	CN22PUE	CN21PUE	CN20PUE ^(1,2)	CN19PUE ^(1,2)	CN18PUE ^(1,2)	CN17PUE ^(1,2)	CN16PUE ⁽¹⁾	0000
CNPU3	0072	—	—	—	—	—	—	—	—	—	—	—	CN36PUE ^(1,2)	CN35PUE ^(1,2)	CN34PUE ^(1,2)	CN33PUE ^(1,2)	CN32PUE ^(1,2)	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are not implemented in 20-pin devices.
2: These bits are not implemented in 28-pin devices.
3: These bits are not implemented in FV devices.

TABLE 4-8: OUTPUT COMPARE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0190	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0192	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0194	OC1RS																0000
OC1R	0196	OC1R																0000
OC1TMR	0198	OC1TMR																xxxx
OC2CON1	019A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	019C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	019E	OC2RS																0000
OC2R	01A0	OC2R																0000
OC2TMR	01A2	OC2TMR																xxxx
OC3CON1	01A4	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	01A6	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	01A8	OC3RS																0000
OC3R	01AA	OC3R																0000
OC3TMR	01AC	OC3TMR																xxxx

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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NOTES:

10.2.4.2 Exiting Deep Sleep Mode

Deep Sleep mode exits on any one of the following events:

- A POR event on VDD supply. If there is no DSBOR circuit to re-arm the VDD supply POR circuit, the external VDD supply must be lowered to the natural arming voltage of the POR circuit.
- A DSWDT time-out. When the DSWDT timer times out, the device exits Deep Sleep.
- An RTCC alarm (if RTCEN = 1).
- An assertion ('0') of the $\overline{\text{MCLR}}$ pin.
- An assertion of the INT0 pin (if the interrupt was enabled before Deep Sleep mode was entered). The polarity configuration is used to determine the assertion level ('0' or '1') of the pin that will cause an exit from Deep Sleep mode. Exiting from Deep Sleep mode requires a change on the INT0 pin while in Deep Sleep mode.

Note: Any interrupt pending when entering Deep Sleep mode is cleared.

Exiting Deep Sleep mode generally does not retain the state of the device and is equivalent to a Power-on Reset (POR) of the device. Exceptions to this include the RTCC (if present), which remains operational through the wake-up, the DSGPRx registers and DSWDT.

Wake-up events that occur after Deep Sleep exits, but before the POR sequence completes, are ignored and are not be captured in the DSWAKE register.

The sequence for exiting Deep Sleep mode is:

1. After a wake-up event, the device exits Deep Sleep and performs a POR. The DSEN bit is cleared automatically. Code execution resumes at the Reset vector.
2. To determine if the device exited Deep Sleep, read the Deep Sleep bit, DPSLP (RCON<10>). This bit will be set if there was an exit from Deep Sleep mode; if the bit is set, clear it.
3. Determine the wake-up source by reading the DSWAKE register.
4. Determine if a DSBOR event occurred during Deep Sleep mode by reading the DSBOR bit (DSCON<1>).
5. If application context data has been saved, read it back from the DSGPR0 and DSGPR1 registers.
6. Clear the RELEASE bit (DSCON<0>).

10.2.4.3 Saving Context Data with the DSGPR0/DSGPR1 Registers

As exiting Deep Sleep mode causes a POR, most Special Function Registers reset to their default POR values. In addition, because V_{CORE} power is not supplied in Deep Sleep mode, information in data RAM may be lost when exiting this mode.

Applications which require critical data to be saved prior to Deep Sleep may use the Deep Sleep General Purpose registers, DSGPR0 and DSGPR1 or data EEPROM (if available). Unlike other SFRs, the contents of these registers are preserved while the device is in Deep Sleep mode. After exiting Deep Sleep, software can restore the data by reading the registers and clearing the RELEASE bit (DSCON<0>).

10.2.4.4 I/O Pins During Deep Sleep

During Deep Sleep, the general purpose I/O pins retain their previous states and the Secondary Oscillator (SOSC) will remain running, if enabled. Pins that are configured as inputs (TRISx bit is set), prior to entry into Deep Sleep, remain high-impedance during Deep Sleep. Pins that are configured as outputs (TRISx bit is clear), prior to entry into Deep Sleep, remain as output pins during Deep Sleep. While in this mode, they continue to drive the output level determined by their corresponding LATx bit at the time of entry into Deep Sleep.

Once the device wakes back up, all I/O pins continue to maintain their previous states, even after the device has finished the POR sequence and is executing application code again. Pins configured as inputs during Deep Sleep remain high-impedance and pins configured as outputs continue to drive their previous value. After waking up, the TRIS and LAT registers, and the SOSCEN bit (OSCCON<1>) are reset. If firmware modifies any of these bits or registers, the I/O will not immediately go to the newly configured states. Once the firmware clears the RELEASE bit (DSCON<0>), the I/O pins are "released". This causes the I/O pins to take the states configured by their respective TRISx and LATx bit values.

This means that keeping the SOSC running after waking up requires the SOSCEN bit to be set before clearing RELEASE.

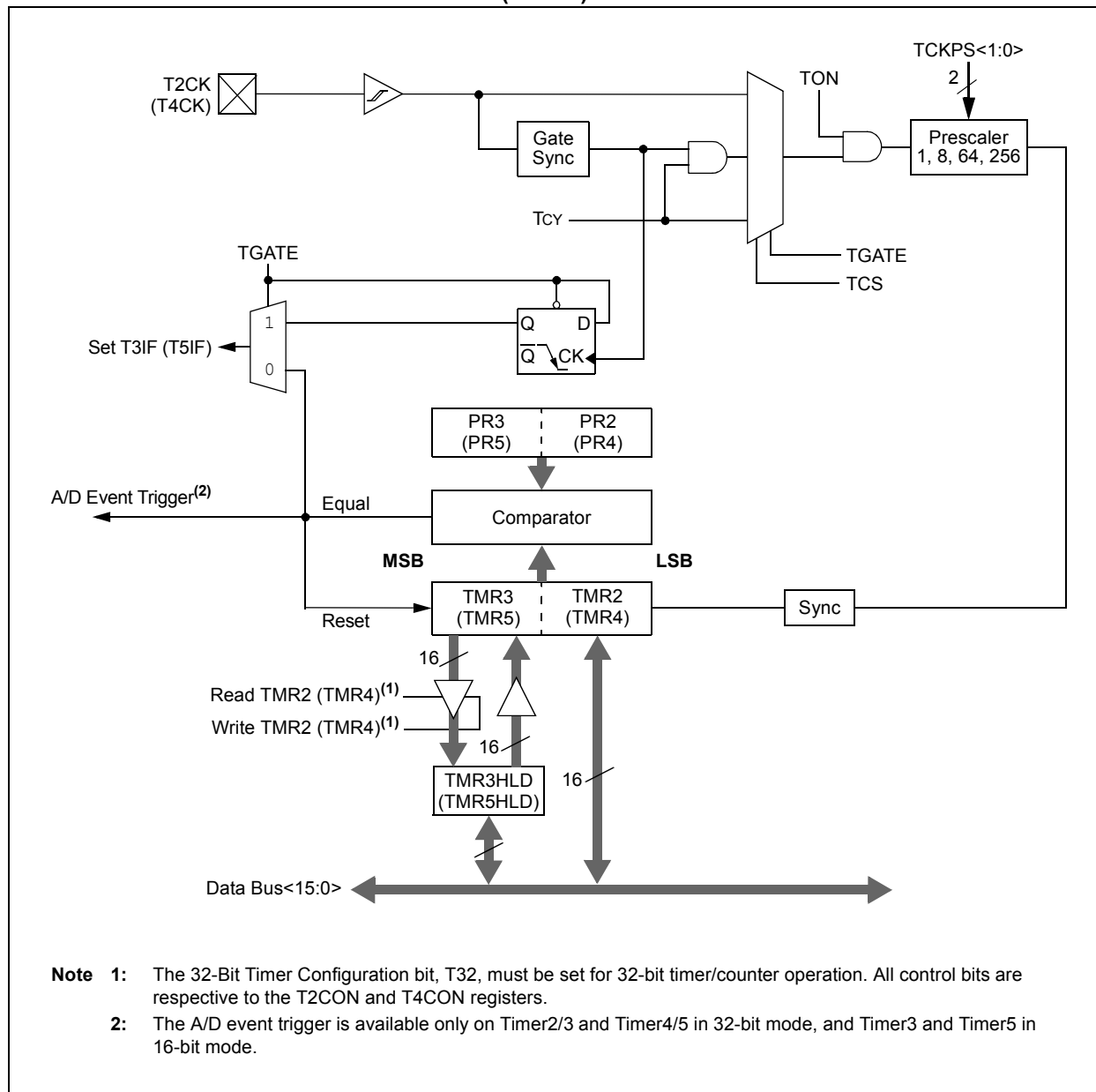
If the Deep Sleep BOR (DSBOR) is enabled, and a DSBOR or a true POR event occurs during Deep Sleep, the I/O pins will be immediately released, similar to clearing the RELEASE bit. All previous state information will be lost, including the general purpose DSGPR0 and DSGPR1 contents.

If a $\overline{\text{MCLR}}$ Reset event occurs during Deep Sleep, the DSGPRx, DSCON and DSWAKE registers will remain valid, and the RELEASE bit will remain set. The state of the SOSC will also be retained. The I/O pins, however, will be reset to their $\overline{\text{MCLR}}$ Reset state. Since RELEASE is still set, changes to the SOSCEN bit (OSCCON<1>) cannot take effect until the RELEASE bit is cleared.

In all other Deep Sleep wake-up cases, application firmware must clear the RELEASE bit in order to reconfigure the I/O pins.

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FIGURE 13-1: TIMER2/3 AND TIMER4/5 (32-BIT) BLOCK DIAGRAM



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REGISTER 13-1: TxCON: TIMER2 AND TIMER4 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32 ⁽¹⁾	—	TCS	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **TON:** Timerx On bit

When TxCON<3> = 1:

1 = Starts 32-bit Timerx/y

0 = Stops 32-bit Timerx/y

When TxCON<3> = 0:

1 = Starts 16-bit Timerx

0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit⁽¹⁾

1 = Timer2 and Timer3 or Timer4 and Timer5 form a single 32-bit timer

0 = Timer2 and Timer3 or Timer4 and Timer5 act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit

1 = External clock from pin, TxCK (on the rising edge)

0 = Internal clock (Fosc/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: In 32-bit mode, the T3CON or T5CON control bits do not affect 32-bit timer operation.

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REGISTER 17-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK9	AMSK8
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AMSK<9:0>:** Mask for Address Bit x Select bits

1 = Enables masking for bit x of an incoming message address; bit match is not required in this position

0 = Disables masking for bit x; bit match is required in this position

REGISTER 17-4: PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	SMBUSDEL2	SMBUSDEL1	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **SMBUSDEL2:** SMBus SDA2 Input Delay Select bit

1 = The I2C2 module is configured for a longer SMBus input delay (nominal 300 ns delay)

0 = The I2C2 module is configured for a legacy input delay (nominal 150 ns delay)

bit 4 **SMBUSDEL1:** SMBus SDA1 Input Delay Select bit

1 = The I2C1 module is configured for a longer SMBus input delay (nominal 300 ns delay)

0 = The I2C1 module is configured for a legacy input delay (nominal 150 ns delay)

bit 3-0 **Unimplemented:** Read as '0'

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REGISTER 19-6: WKDYHR: WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 19-7: MINSEC: MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit bits
Contains a value from 0 to 9.

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REGISTER 19-10: ALMINSEC: ALARM MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit bits
Contains a value from 0 to 9.

FIGURE 19-2: ALARM MASK SETTINGS

Alarm Mask Setting (AMASK<3:0>)	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 - Every half second 0001 - Every second	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>
0010 - Every 10 seconds	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> s
0011 - Every minute	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> s <input type="checkbox"/> s
0100 - Every 10 minutes	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
0101 - Every hour	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
0110 - Every day	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> h <input type="checkbox"/> h	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
0111 - Every week	<input type="checkbox"/> d	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> h <input type="checkbox"/> h	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
1000 - Every month	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> d <input type="checkbox"/> d	<input type="checkbox"/> h <input type="checkbox"/> h	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
1001 - Every year ⁽¹⁾	<input type="checkbox"/>	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> d <input type="checkbox"/> d	<input type="checkbox"/> h <input type="checkbox"/> h	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s

Note 1: Annually, except when configured for February 29.

19.5 POWER CONTROL

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, wait for the device to be stable before sampling wake-up events from that device and then shut down the external device. This can be done completely autonomously by the RTCC, without the need to wake from the current low-power mode (Sleep, Deep Sleep, etc.).

To enable this feature, the RTCC must be enabled (RTCCEN = 1), the PWCEN register bit must be set and the RTCC pin must be driving the PWC control signal (RTCCOE = 1 and RTCOUT<1:0> = 11).

The polarity of the PWC control signal may be chosen using the PWCPOL register bit. Active-low or active-high may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pin. This setting is able to drive the GND pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches. Finally, the CHIME bit should be set to enable the PWC periodicity.

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27.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

27.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, pre-processor, and one-step driver, and can run on multiple platforms.

27.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

27.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

27.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

PIC24FV32KA304 FAMILY

TABLE 29-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX					
		Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Parameter No.	Device	Typical ⁽¹⁾	Max	Units	Conditions		
Module Differential Current (ΔIPD) ⁽³⁾							
DC78	PIC24FV32KA3XX	0.03	—	μA	-40°C	2.0V	Deep Sleep BOR: ΔILPBOR ⁽⁵⁾
		0.05	0.20	μA	+85°C	5.0V	
		—	0.30	μA	+125°C	5.0V	
	PIC24F32KA3XX	0.03	—	μA	-40°C	1.8V	
		0.05	0.20	μA	+85°C	3.3V	
		—	0.30	μA	+125°C	3.3V	
DC80	PIC24FV32KA3XX	0.20	—	μA	-40°C	2.0V	Deep Sleep WDT: ΔIDSWDT (LPRC) ⁽⁶⁾
		0.70	1.5	μA	+85°C	5.0V	
		—	1.5	μA	+125°C	5.0V	
	PIC24F32KA3XX	0.20	—	μA	-40°C	1.8V	
		0.35	0.8	μA	+85°C	3.3V	
		—	1.5	μA	+125°C	3.3V	

Legend: Unshaded rows represent PIC24F32KA3XX devices and shaded rows represent PIC24FV32KA3XX devices.

Note 1: Data in the Typical column is at 3.3V, +25°C (PIC24F32KA3XX) or 5.0V, +25°C (PIC24FV32KA3XX) unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low, PMSLP is set to '0' and WDT, etc., are all switched off.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: This current applies to Sleep only.

5: This current applies to Sleep and Deep Sleep.

6: This current applies to Deep Sleep only.

PIC24FV32KA304 FAMILY

FIGURE 29-8: TIMER1/2/3/4/5 EXTERNAL CLOCK INPUT TIMING

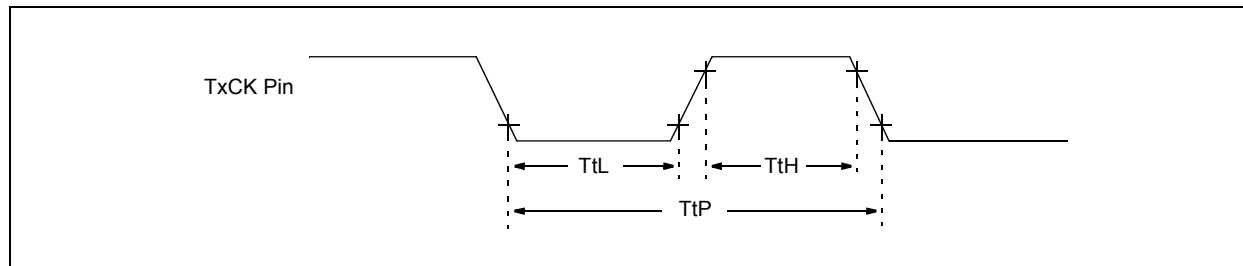


TABLE 29-27: TIMER1/2/3/4/5 EXTERNAL CLOCK INPUT REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
	TtH	TxCK High Pulse Time	Sync w/Prescaler	$T_{CY} + 20$	—	ns	Must also meet Parameter Ttp
			Async w/Prescaler	10	—	ns	
			Async Counter	20	—	ns	
	TtL	TxCK Low Pulse Time	Sync w/Prescaler	$T_{CY} + 20$	—	ns	Must also meet Parameter Ttp
			Async w/Prescaler	10	—	ns	
			Async Counter	20	—	ns	
	TtP	TxCK External Input Period	Sync w/Prescaler	$2 * T_{CY} + 40$	—	ns	N = Prescale Value (1, 4, 8, 16)
			Async w/Prescaler	Greater of: 20 or $\frac{2 * T_{CY} + 40}{N}$	—	ns	
			Async Counter	40	—	ns	
		Delay for Input Edge to Timer Increment	Synchronous	1	2	T_{CY}	
			Asynchronous	—	20	ns	

FIGURE 29-9: INPUT CAPTURE x TIMINGS

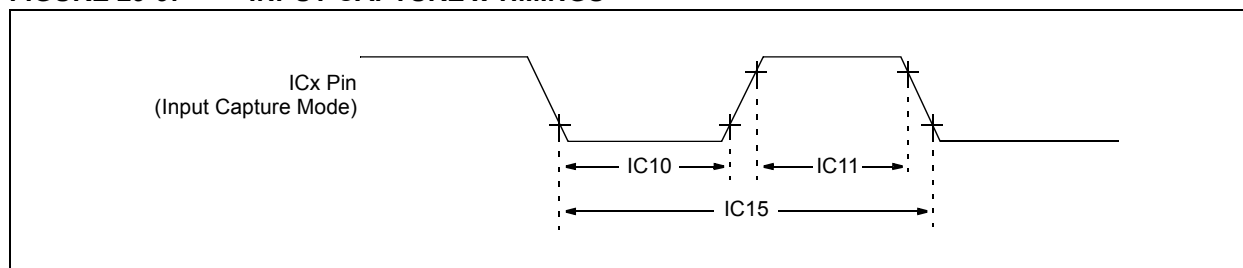


TABLE 29-28: INPUT CAPTURE x REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
IC10	TccL	ICx Input Low Time – Synchronous Timer	No Prescaler	$T_{CY} + 20$	—	ns	Must also meet Parameter IC15
			With Prescaler	20	—	ns	
IC11	TccH	ICx Input Low Time – Synchronous Timer	No Prescaler	$T_{CY} + 20$	—	ns	Must also meet Parameter IC15
			With Prescaler	20	—	ns	
IC15	TccP	ICx Input Period – Synchronous Timer		$\frac{2 * T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4, 16)

PIC24FV32KA304 FAMILY

FIGURE 29-12: I²C™ BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

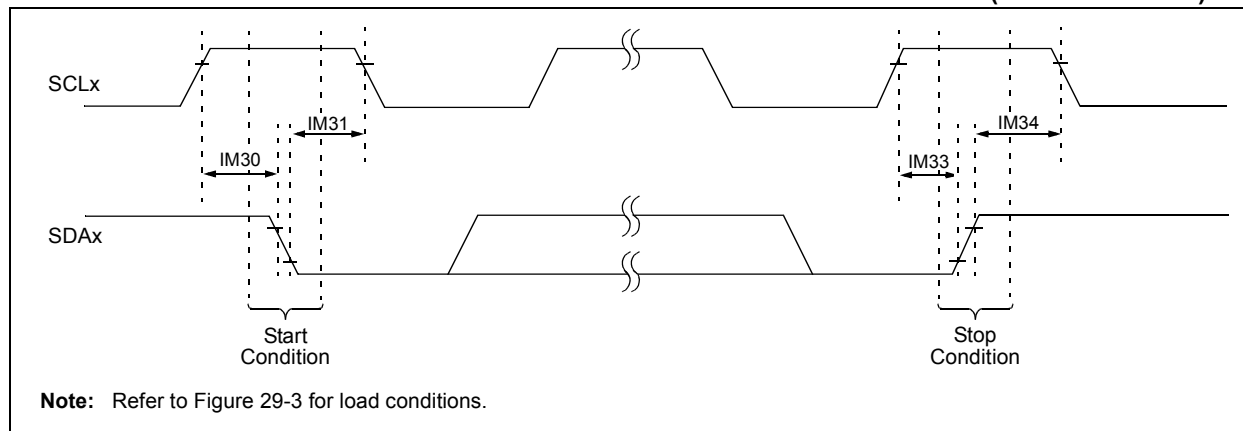


TABLE 29-31: I²C™ BUS START/STOP BIT TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial) -40°C ≤ T _A ≤ +125°C for Extended			
Param No.	Symbol	Characteristic		Min ⁽¹⁾	Max	Units	Conditions
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	T _{CY} /2 (BRG + 1)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	T _{CY} /2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	T _{CY} /2 (BRG + 1)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	T _{CY} /2 (BRG + 1)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	T _{CY} /2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	T _{CY} /2 (BRG + 1)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	T _{CY} /2 (BRG + 1)	—	μs	
			400 kHz mode	T _{CY} /2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	T _{CY} /2 (BRG + 1)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	T _{CY} /2 (BRG + 1)	—	ns	
			400 kHz mode	T _{CY} /2 (BRG + 1)	—	ns	
			1 MHz mode ⁽²⁾	T _{CY} /2 (BRG + 1)	—	ns	

Note 1: BRG is the value of the I²C™ Baud Rate Generator. Refer to **Section 17.3 “Setting Baud Rate When Operating as a Bus Master”** for details.

2: Maximum pin capacitance = 10 pF for all I²C pins (for 1 MHz mode only).

PIC24FV32KA304 FAMILY

FIGURE 30-3: TYPICAL AND MAXIMUM I_{IDLE} vs. FREQUENCY (EC MODE, 2 MHz TO 32 MHz)

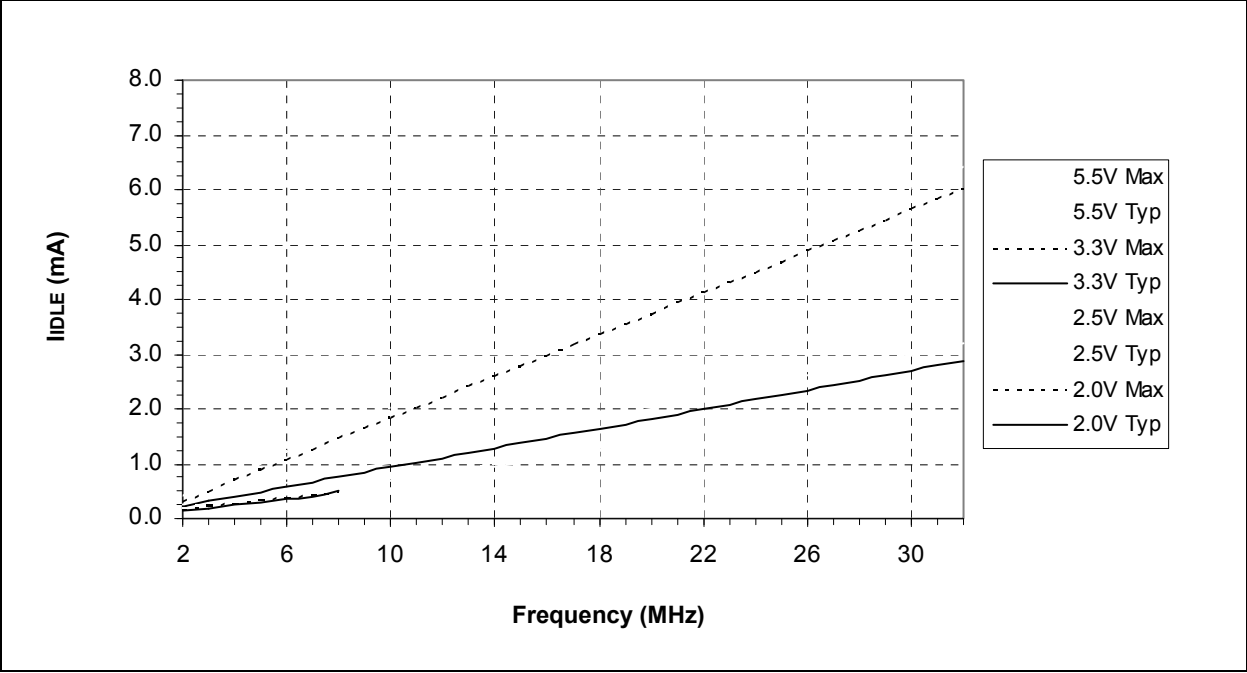
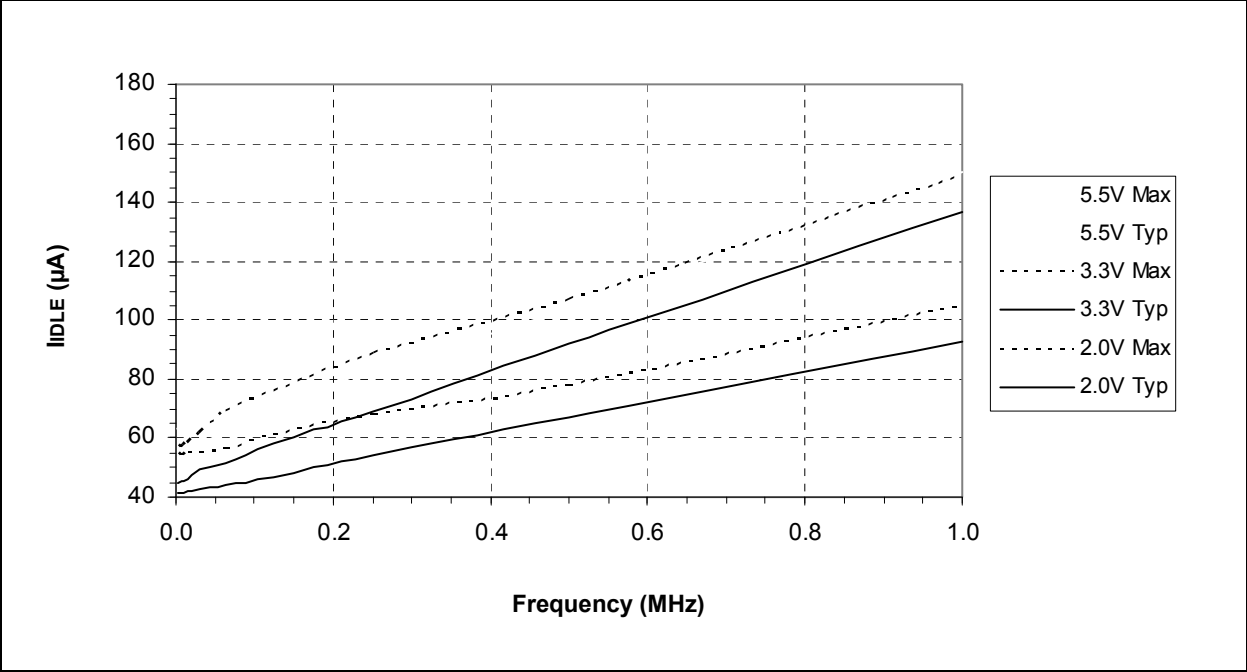


FIGURE 30-4: TYPICAL AND MAXIMUM I_{IDLE} vs. FREQUENCY (EC MODE, 1.95 kHz TO 1 MHz)



PIC24FV32KA304 FAMILY

FIGURE 30-5: TYPICAL I_{DD} vs. V_{DD} (8 MHz, EC MODE)

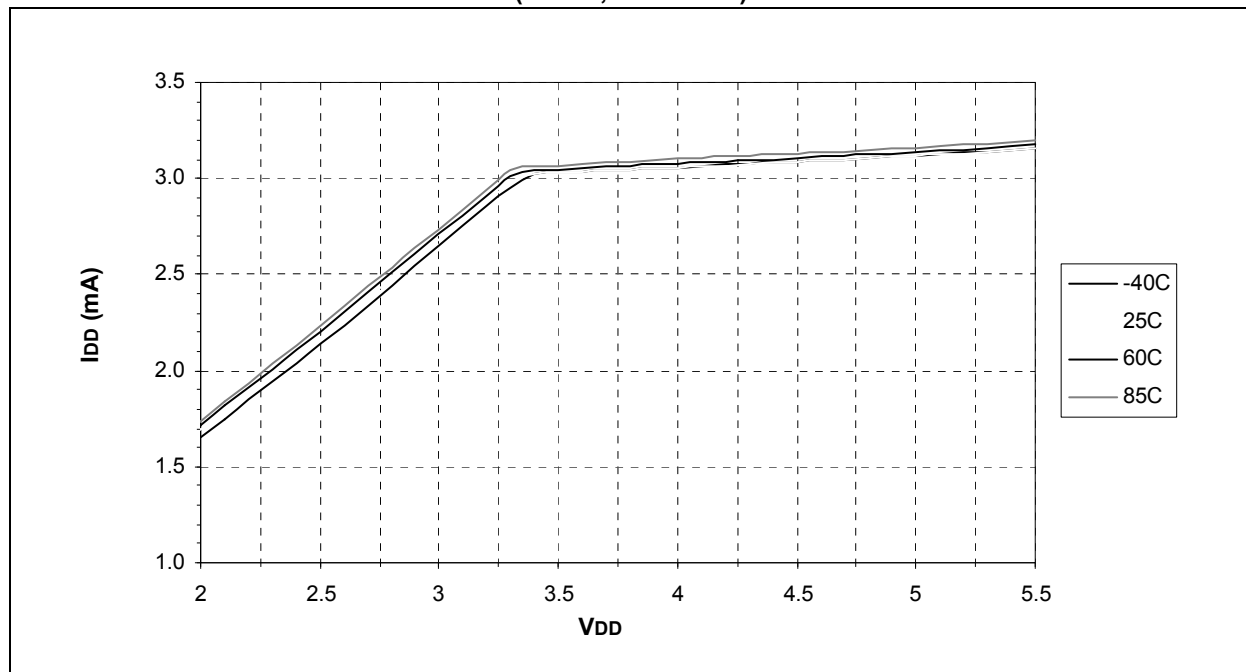


FIGURE 30-6: TYPICAL I_{DD} vs. V_{DD} (FRC MODE)

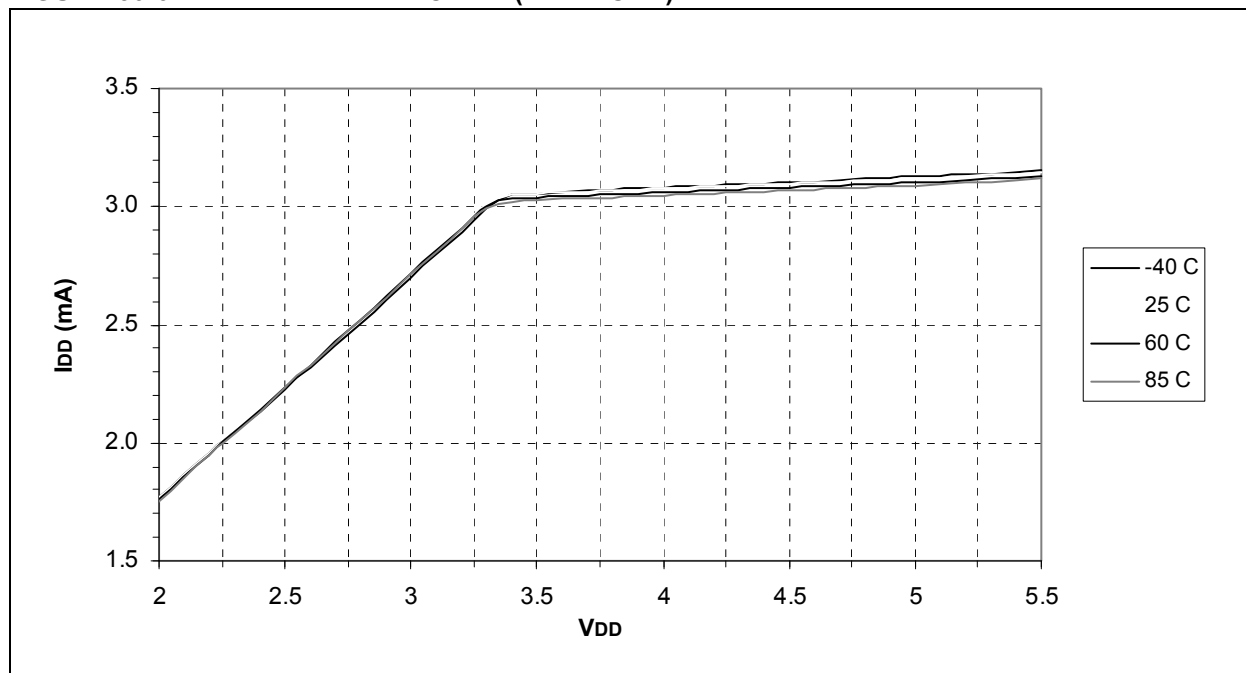
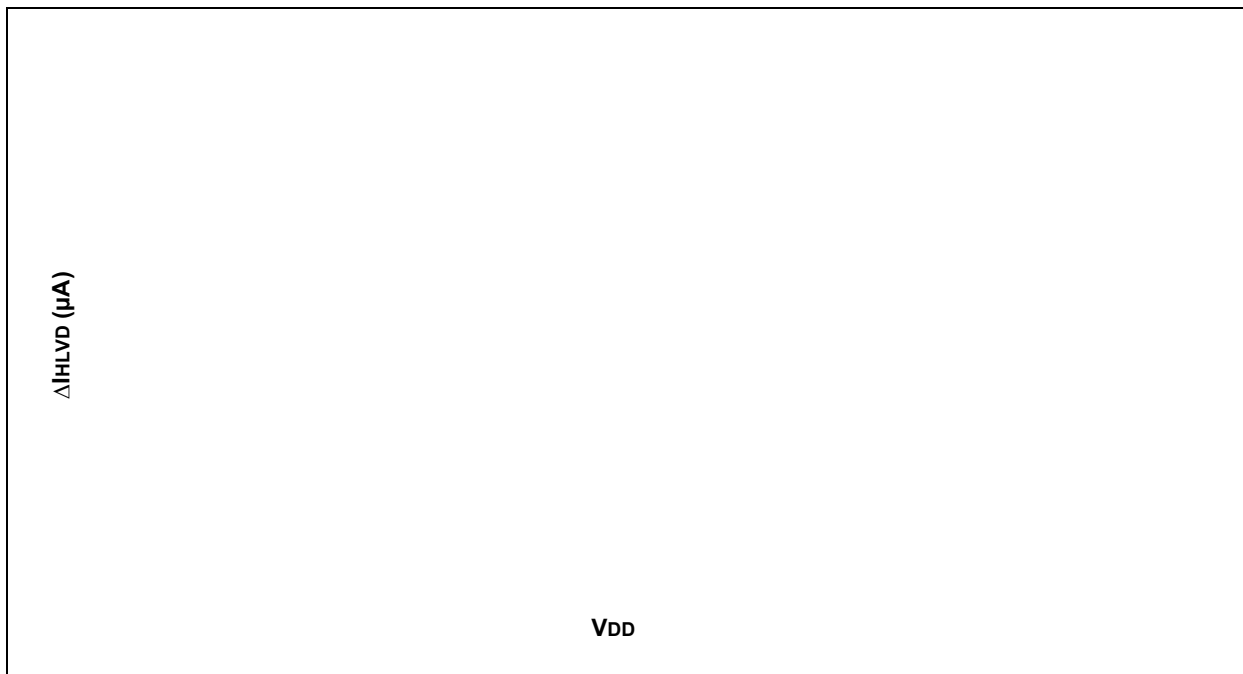


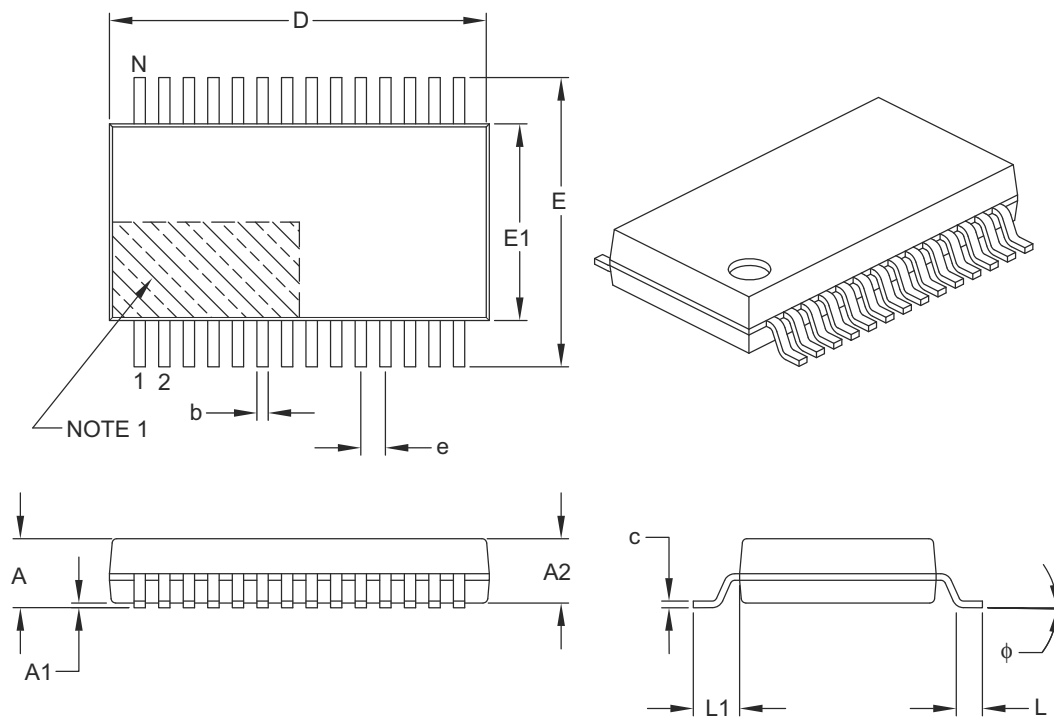
FIGURE 30-48: TYPICAL ΔI_{HLVD} vs. V_{DD}



PIC24FV32KA304 FAMILY

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

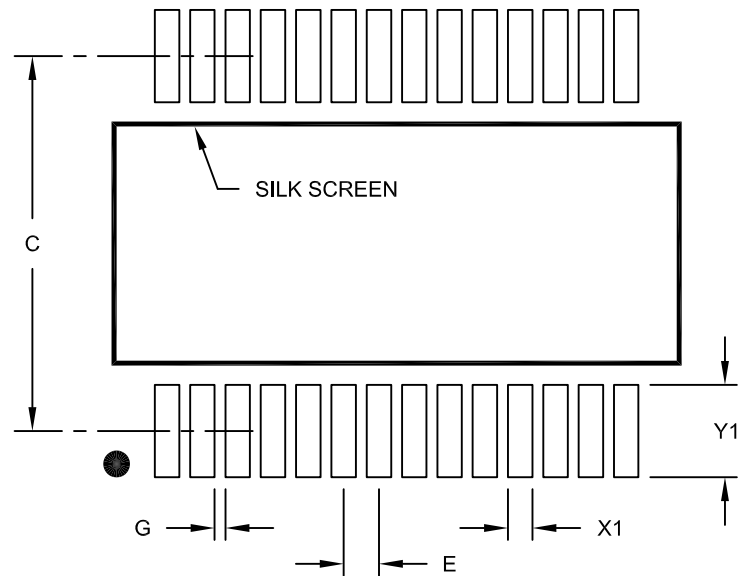
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

PIC24FV32KA304 FAMILY

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

PIC24FV32KA304 FAMILY

NOTES: