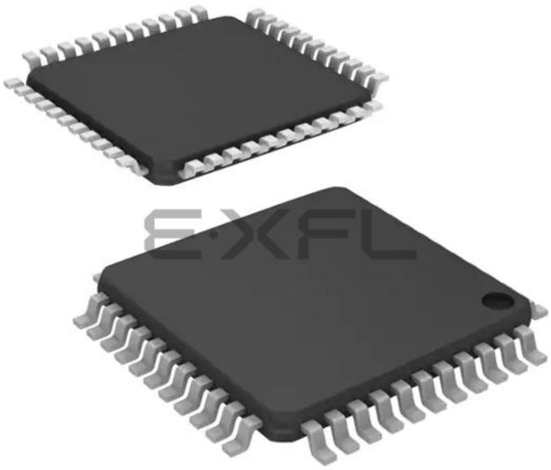


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

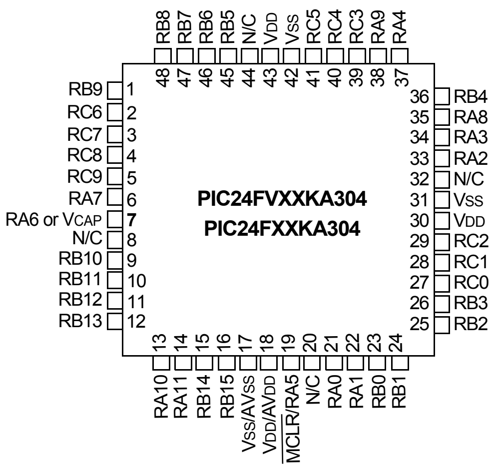
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f32ka304-i-pt

Pin Diagrams

48-Pin UQFN(1,2,3)



Pin	Pin Features	
	PIC24FVXXKA304	**PIC24FXXKA304**
1	SDA1/T1CK/$\overline{\text{U1RTS}}$/CTED4/CN21/RB9	SDA1/T1CK/$\overline{\text{U1RTS}}$/CTED4/CN21/RB9
2	U1RX/CN18/RC6	U1RX/CN18/RC6
3	U1TX/CN17/RC7	U1TX/CN17/RC7
4	OC2/CN20/RC8	OC2/CN20/RC8
5	IC2/CTED7/CN19/RC9	IC2/CTED7/CN19/RC9
6	IC1/CTED3/CN9/RA7	IC1/CTED3/CN9/RA7
7	**VCAP**	**C20UT/OC1/CTED1/INT2CN8/RA6**
8	N/C	N/C
9	PGED2/SDI1/CTED11/CN16/RB10	PGED2/SDI1/CTED11/CN16/RB10
10	PGEC2/SCK1/CTED9/CN15/RB11	PGEC2/SCK1/CTED9/CN15/RB11
11	AN12/HLVDIN/CTED2/**INT2**/CN14/RB12	AN12/HLVDIN/CTED2/CN14/RB12
12	AN11/SDO1/CTPLS/CN13/RB13	AN11/SDO1/CTPLS/CN13/RB13
13	OC3/CN35/RA10	OC3/CN35/RA10
14	IC3/CTED8/CN36/RA11	IC3/CTED8/CN36/RA11
15	CVREF/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14	CVREF/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14
16	AN9/C3INA/T3CK/T2CK/REFO/$\overline{\text{SS1}}$/CTED6/CN11/RB15	AN9/C3INA/T3CK/T2CK/REFO/$\overline{\text{SS1}}$/CTED6/CN11/RB15
17	VSS/AVSS	VSS/AVSS
18	VDD/AVDD	VDD/AVDD
19	$\overline{\text{MCLR}}$/RA5	$\overline{\text{MCLR}}$/RA5
20	N/C	N/C
21	VREF+/CVREF+/AN0/C3INC/CTED1/CN2/RA0	VREF+/CVREF+/AN0/C3INC/CN2/RA0
22	CVREF-/VREF-/AN1/CN3/RA1	CVREF-/VREF-/AN1/CN3/RA1
23	PGED1/AN2/ULPWU/CTCMP/C1IND/C2INB/C3IND/U2TX/CN4/RB0	PGED1/AN2/ULPWU/CTCMP/C1IND/C2INB/C3IND/U2TX/CN4/RB0
24	PGEC1/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1	PGEC1/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1
25	AN4/C1INB/C2IND/SDA2/T5CK/T4CK/CTED13/CN6/RB2	AN4/C1INB/C2IND/SDA2/T5CK/T4CK/CTED13/CN6/RB2
26	AN5/C1INA/C2INC/SCL2/CN7/RB3	AN5/C1INA/C2INC/SCL2/CN7/RB3
27	AN6/CN32/RC0	AN6/CN32/RC0
28	AN7/CN31/RC1	AN7/CN31/RC1
29	AN8/CN10/RC2	AN8/CN10/RC2
30	VDD	VDD
31	VSS	VSS
32	N/C	N/C
33	OSCI/AN13/CLKI/CN30/RA2	OSCI/AN13/CLKI/CN30/RA2
34	OSCO/AN14/CLKO/CN29/RA3	OSCO/AN14/CLKO/CN29/RA3
35	OCFB/CN33/RA8	OCFB/CN33/RA8
36	SOSCI/AN15/$\overline{\text{U2RTS}}$/CN1/RB4	SOSCI/AN15/$\overline{\text{U2RTS}}$/CN1/RB4
37	SOSCO/SCLKI/$\overline{\text{U2CTS}}$/CN0/RA4	SOSCO/SCLKI/$\overline{\text{U2CTS}}$/CN0/RA4
38	$\overline{\text{SS2}}$/CN34/RA9	$\overline{\text{SS2}}$/CN34/RA9
39	SDI2/CN28/RC3	SDI2/CN28/RC3
40	SDO2/CN25/RC4	SDO2/CN25/RC4
41	SCK2/CN26/RC5	SCK2/CN26/RC5
42	VSS	VSS
43	VDD	VDD
44	N/C	N/C
45	PGED3/ASDA1(2)/CN27/RB5	PGED3/ASDA1(2)/CN27/RB5
46	PGEC3/ASCL1(2)/CN24/RB6	PGEC3/ASCL1(2)/CN24/RB6
47	C2OUT/OC1/INT0/CN23/RB7	INT0/CN23/RB7
48	SCL1/$\overline{\text{U1CTS}}$/C3OUT/CTED10/CN22/RB8	SCL1/$\overline{\text{U1CTS}}$/C3OUT/CTED10/CN22/RB8

Legend: Pin numbers in **bold** indicate pin function differences between PIC24FV and PIC24F devices.

Note 1: Exposed pad on underside of device is connected to VSS.

2: Alternative multiplexing for SDA1 (ASDA1) and SCL1 (ASCL1) when the I2CSEL Configuration bit is set.

3: PIC24F32KA3XX device pins have a maximum voltage of 3.6V and are not 5V tolerant.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24F32KA304 FAMILY

Features	PIC24F16KA301	PIC24F32KA301	PIC24F16KA302	PIC24F32KA302	PIC16F16KA304	PIC24F32KA304
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	16K	32K	16K	32K	16K	32K
Program Memory (instructions)	5632	11264	5632	11264	5632	11264
Data Memory (bytes)	2048					
Data EEPROM Memory (bytes)	512					
Interrupt Sources (soft vectors/ NMI traps)	30 (26/4)					
I/O Ports	PORTA<6:0>, PORTB<15:12, 9:7, 4, 2:0>		PORTA<7:0>, PORTB<15:0>		PORTA<11:0>, PORTB<15:0>, PORTC<9:0>	
Total I/O Pins	18		24		39	
Timers: Total Number (16-bit)	5					
32-Bit (from paired 16-bit timers)	2					
Input Capture Channels	3					
Output Compare/PWM Channels	3					
Input Change Notification Interrupt	17		23		38	
Serial Communications: UART SPI (3-wire/4-wire)	2					
I^2C™	2					
12-Bit Analog-to-Digital Module (input channels)	12		13		16	
Analog Comparators	3					
Resets (and delays)	POR, BOR, `RESET` Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, `REPEAT` Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)					
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations					
Packages	20-Pin PDIP/SSOP/SOIC		28-Pin SPDIP/SSOP/SOIC/QFN		44-Pin QFN/TQFP 48-Pin UQFN	

TABLE 1-3: PIC24FV32KA304 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
CN23	11	16	13	43	47	11	16	13	43	47	I	ST	Interrupt-on-Change Inputs
CN24	—	15	12	42	46	—	15	12	42	46	I	ST	
CN25	—	—	—	37	40	—	—	—	37	40	I	ST	
CN26	—	—	—	38	41	—	—	—	38	41	I	ST	
CN27	—	14	11	41	45	—	14	11	41	45	I	ST	
CN28	—	—	—	36	39	—	—	—	36	39	I	ST	
CN29	8	10	7	31	34	8	10	7	31	34	I	ST	
CN30	7	9	6	30	33	7	9	6	30	33	I	ST	
CN31	—	—	—	26	28	—	—	—	26	28	I	ST	
CN32	—	—	—	25	27	—	—	—	25	27	I	ST	
CN33	—	—	—	32	35	—	—	—	32	35	I	ST	
CN34	—	—	—	35	38	—	—	—	35	38	I	ST	
CN35	—	—	—	12	13	—	—	—	12	13	I	ST	
CN36	—	—	—	13	14	—	—	—	13	14	I	ST	
CVREF	17	25	22	14	15	17	25	22	14	15	I	ANA	Comparator Voltage Reference Output
CVREF+	2	2	27	19	21	2	2	27	19	21	I	ANA	Comparator Reference Positive Input Voltage
CVREF-	3	3	28	20	22	3	3	28	20	22	I	ANA	Comparator Reference Negative Input Voltage
CTCMP	4	4	1	21	23	4	4	1	21	23	I	ANA	CTMU Comparator Input
CTED1	14	20	17	7	7	11	2	27	19	21	I	ST	CTMU Trigger Edge Inputs
CTED2	15	23	20	10	11	15	23	20	10	11	I	ST	
CTED3	—	19	16	6	6	—	19	16	6	6	I	ST	
CTED4	13	18	15	1	1	13	18	15	1	1	I	ST	
CTED5	17	25	22	14	15	17	25	22	14	15	I	ST	
CTED6	18	26	23	15	16	18	26	23	15	16	I	ST	
CTED7	—	—	—	5	5	—	—	—	5	5	I	ST	
CTED8	—	—	—	13	14	—	—	—	13	14	I	ST	
CTED9	—	22	19	9	10	—	22	19	9	10	I	ST	
CTED10	12	17	14	44	48	12	17	14	44	48	I	ST	
CTED11	—	21	18	8	9	—	21	18	8	9	I	ST	
CTED12	5	5	2	22	24	5	5	2	22	24	I	ST	
CTED13	6	6	3	23	25	6	6	3	23	25	I	ST	

4.0 MEMORY ORGANIZATION

As Harvard architecture devices, the PIC24F microcontrollers feature separate program and data memory space and bussing. This architecture also allows the direct access of program memory from the data space during code execution.

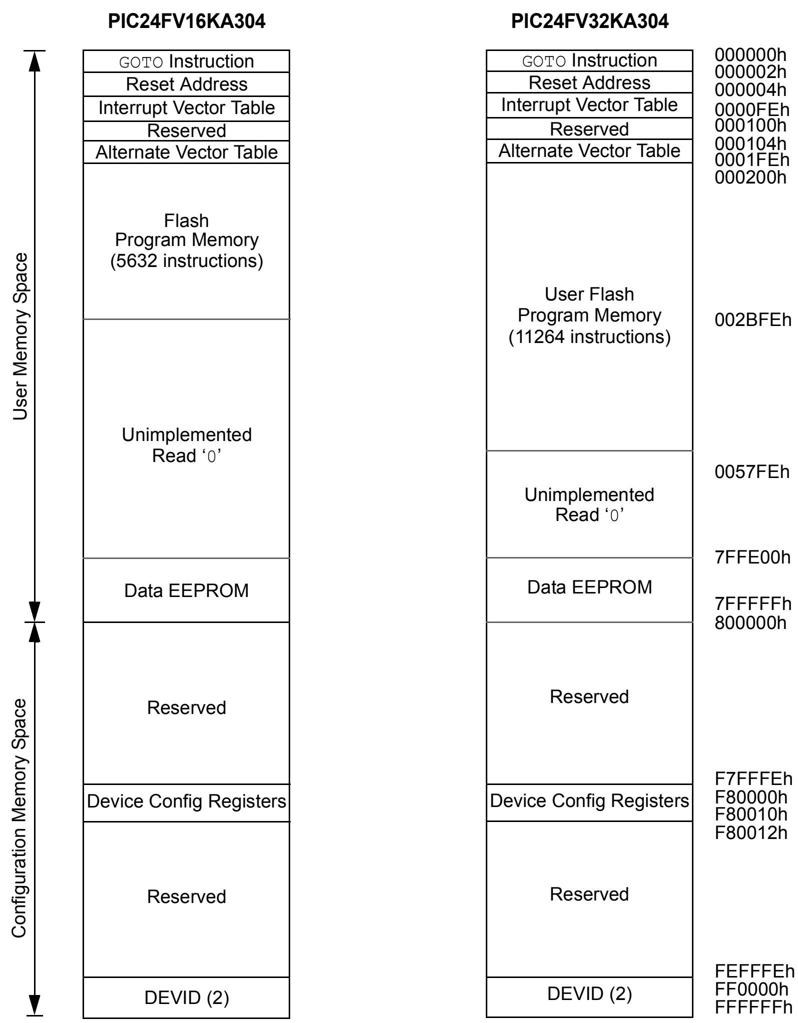
4.1 Program Address Space

The program address memory space of the PIC24FV32KA304 family is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from a table operation or data space remapping, as described in **Section 4.3 "Interfacing Program and Data Memory Spaces"**.

User access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFh). The exception is the use of `TBLRD/TBLWT` operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for the PIC24FV32KA304 family of devices are shown in Figure 4-1.

FIGURE 4-1: PROGRAM SPACE MEMORY MAP FOR PIC24FV32KA304 FAMILY DEVICES



Note: Memory areas are not displayed to scale.

REGISTER 8-30: IPC18: INTERRUPT PRIORITY CONTROL REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	HLVDIP2	HLVDIP1	HLVDIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **HLVDIP<2:0>:** High/Low-Voltage Detect Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-31: IPC19: INTERRUPT PRIORITY CONTROL REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CTMUIP2	CTMUIP1	CTMUIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CTMUIP<2:0>:** CTMU Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

13.0 TIMER2/3 AND TIMER4/5

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Timers, refer to the *"PIC24F Family Reference Manual"*, **Section 14. "Timers"** (DS39704).

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent,16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 or Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle mode
- Interrupt on a 32-Bit Period Register Match
- A/D Event Trigger

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the A/D event trigger (this is implemented only with Timer3). The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. The T2CON,T3CON, T4CON and T5CON registers are provided in generic form in Register 13-1 and Register 13-2, respectively.

For 32-bit timer/counter operation, Timer2/Timer4 is the least significant word (lsw) and Timer3/Timer5 is the most significant word (msw) of the 32-bit timer.

> **Note:** For 32-bit operation, T3CON or T5CON control bits are ignored. Only T2CON or T4CON control bits are used for setup and control. Timer2 or Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 or Timer5 interrupt flags.

To configure Timer2/3 or Timer4/5 for 32-bit operation:

1. Set the T32 bit (T2CON<3> or T4CON<3> = `1`).
2. Select the prescaler ratio for Timer2 or Timer4 using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Load the timer period value. PR3 (or PR5) will contain the most significant word of the value, while PR2 (or PR4) contains the least significant word.
5. If interrupts are required, set the Timerx Interrupt Enable bit, TxIE. Use the Timerx Interrupt Priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON bit (TxCON<15> = `1`).

The timer value, at any point, is stored in the register pair, TMR3:TMR2 (or TMR5:TMR4). TMR3 (TMR5) always contains the most significant word of the count, while TMR2 (TMR4) contains the least significant word.

To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit corresponding to that timer (T2CON<3> for Timer2 and Timer3 or T4CON<3> for Timer4 and Timer5).
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the Timerx Interrupt Enable bit, TxIE; use the Timerx Interrupt Priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON bit (TxCON<15> = `1`).

15.0 OUTPUT COMPARE WITH DEDICATED TIMERS

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **Section 35. "Output Compare with Dedicated Timer"** (DS39723).

All devices in the PIC24FV32KA304 family feature 3 independent output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events. Also, the modules can produce Pulse-Width Modulated (PWM) waveforms for driving power applications.

Key features of the output compare module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 21 user-selectable Sync/trigger sources available
- Two separate Period registers (a main register, OCxR, and a secondary register, OCxRS) for greater flexibility in generating pulses of varying widths
- Configurable for single pulse or continuous pulse generation on an output event, or continuous PWM waveform generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

15.1 General Operating Modes

15.1.1 SYNCHRONOUS AND TRIGGER MODES

By default, the output compare module operates in a Free-Running mode. The internal 16-bit counter, OCxTMR, counts up continuously, wrapping around from FFFFh to 0000h on each overflow, with its period synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the Period registers occurs.

In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected Sync source, the module's internal counter is reset. In Trigger mode, the module waits for a Sync event from another internal module to occur before allowing the counter to run.

Free-Running mode is selected by default or any time that the SYNCSELx bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSELx bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode. Setting this bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the Sync/trigger source.

15.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-bit Timer and Duty Cycle registers. To increase the range, adjacent even and odd numbered modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module (OCx) provides the Least Significant 16 bits of the 32-bit register pairs, and the even numbered module (OCy) provides the Most Significant 16 bits. Wraparounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bit (OCxCON2<8>) for both modules.

REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
HS = Hardware Settable bit	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** IrDA® Encoder Transmit Polarity Inversion bit

<u>If IREN = 0:</u>
1 = UxTX Idle ‘0’
0 = UxTX Idle ‘1’

<u>If IREN = 1:</u>
1 = UxTX Idle ‘1’
0 = UxTX Idle ‘0’

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve ‘0’ bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit
- 1 = Transmit is enabled; UxTX pin is controlled by UARTx
- 0 = Transmit is disabled; any pending transmission is aborted and the buffer is reset. UxTX pin is controlled by the PORT register.

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and the transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty; a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on a RSR transfer, making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on a RSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the RSR to the receive buffer; receive buffer has one or more characters.

REGISTER 19-2: RTCPWC: RTCC CONFIGURATION REGISTER 2(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCEN	PWCPOL	PWCCPRE	PWCSPRE	RTCCLK1(2)	RTCCLK0(2)	RTCOUT1	RTCOUT0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWCEN:** Power Control Enable bit
1 = Power control is enabled
0 = Power control is disabled

bit 14 **PWCPOL:** Power Control Polarity bit
1 = Power control output is active-high
0 = Power control output is active-low

bit 13 **PWCCPRE:** Power Control Control/Stability Prescaler bits
1 = PWC stability window clock is divide-by-2 of source RTCC clock
0 = PWC stability window clock is divide-by-1 of source RTCC clock

bit 12 **PWCSPRE:** Power Control Sample Prescaler bits
1 = PWC sample window clock is divide-by-2 of source RTCC clock
0 = PWC sample window clock is divide-by-1 of source RTCC clock

bit 11-10 **RTCCLK<1:0>:** RTCC Clock Select bits(2)
Determines the source of the internal RTCC clock, which is used for all RTCC timer operations.
00 = External Secondary Oscillator (SOSC)
01 = Internal LPRC Oscillator
10 = External power line source – 50 Hz
11 = External power line source – 60 Hz

bit 9-8 **RTCOUT<1:0>:** RTCC Output Select bits
Determines the source of the RTCC pin output.
00 = RTCC alarm pulse
01 = RTCC seconds clock
10 = RTCC clock
11 = Power control

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: The RTCPWC register is only affected by a POR.
2: When a new value is written to these register bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

19.2.6 ALRMVAL REGISTER MAPPINGS

REGISTER 19-8: ALMTHDY: ALARM MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month’s Tens Digit bit
Contains a value of ‘0’ or ‘1’.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month’s Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day’s Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 19-9: ALWDHR: ALARM WEEKDAY AND HOURS VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour’s Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

20.1.3 DATA SHIFT DIRECTION

The LENDIAN bit (CRCCON1<3>) is used to control the shift direction. By default, the CRC will shift data through the engine, MSb first. Setting LENDIAN (= `1`) causes the CRC to shift data, LSb first. This setting allows better integration with various communication schemes and removes the overhead of reversing the bit order in software. Note that this only changes the direction of the data that is shifted into the engine. The result of the CRC calculation will still be a normal CRC result, not a reverse CRC result.

20.1.4 INTERRUPT OPERATION

The module generates an interrupt that is configurable by the user for either of two conditions. If CRCISEL is '`0`', an interrupt is generated when the VWORD<4:0> bits make a transition from a value of '`1`' to '`0`'. If CRCISEL is '`1`', an interrupt will be generated after the CRC operation finishes and the module sets the CRCGO bit to '`0`'. Manually setting CRCGO to '`0`' will not generate an interrupt.

20.1.5 TYPICAL OPERATION

To use the module for a typical CRC calculation:

1. Set the CRCEN bit to enable the module.
2. Configure the module for the desired operation:
   a) Program the desired polynomial using the CRCXORL and CRCXORH registers, and the PLEN<4:0> bits.
   b) Configure the data width and shift direction using the DWIDTHx and LENDIAN bits.
   c) Select the desired interrupt mode using the CRCISEL bit.
3. Preload the FIFO by writing to the CRCDATL and CRCDATH registers until the CRCFUL bit is set or no data is left.
4. Clear old results by writing 00h to CRCWDATL and CRCWDATH. CRCWDAT can also be left unchanged to resume a previously halted calculation.
5. Set the CRCGO bit to start calculation.
6. Write the remaining data into the FIFO as space becomes available.
7. When the calculation completes, CRCGO is automatically cleared. An interrupt will be generated if CRCISEL = `1`.
8. Read CRCWDATL and CRCWDATH for the result of the calculation.

20.2 Registers

There are eight registers associated with the module:

- CRCCON1
- CRCCON2
- CRCXORL
- CRCXORH
- CRCDATL
- CRCDATH
- CRCWDATL
- CRCWDATH

The CRCCON1 and CRCCON2 registers (Register 20-1 and Register 20-2) control the operation of the module, and configure the various settings. The CRCXOR registers (Register 20-3 and Register 20-4) select the polynomial terms to be used in the CRC equation. The CRCDAT and CRCWDAT registers are each register pairs that serve as buffers for the double-word, input data and CRC processed output, respectively.

REGISTER 22-1: AD1CON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	—	—	MODE12	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as ‘0’	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** A/D Operating Mode bit
1 = A/D Converter module is operating
0 = A/D Converter is off

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **ADSIDL:** A/D Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **Unimplemented:** Read as ‘0’

bit 10 **MODE12:** 12-Bit Operation Mode bit
1 = 12-bit A/D operation
0 = 10-bit A/D operation

bit 9-8 **FORM<1:0>:** Data Output Format bits (see the following formats)
11 = Fractional result, signed, left-justified
10 = Absolute fractional result, unsigned, left-justified
01 = Decimal result, signed, right-justified
00 = Absolute decimal result, unsigned, right-justified

bit 7-4 **SSRC<3:0>:** Sample Clock Source Select bits
1111 = Not available; do not use
•
•
•
1000 = Not available; do not use
0111 = Internal counter ends sampling and starts conversion (auto-convert)
0110 = Not available; do not use
0101 = Timer1 event ends sampling and starts conversion
0100 = CTMU event ends sampling and starts conversion
0011 = Timer5 event ends sampling and starts conversion
0010 = Timer3 event ends sampling and starts conversion
0001 = INT0 event ends sampling and starts conversion
0000 = Clearing the SAMP bit in software ends sampling and begins conversion

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **ASAM:** A/D Sample Auto-Start bit
1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set
0 = Sampling begins when the SAMP bit is manually set

bit 1 **SAMP:** A/D Sample Enable bit
1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit
1 = A/D conversion cycle has completed
0 = A/D conversion cycle has not started or is in progress

REGISTER 22-4: AD1CON5: A/D CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	r-0	U-0	R/W-0	R/W-0
ASEN(1)	LPEN	CTMREQ	BGREQ	r	—	ASINT1	ASINT0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	WM1	WM0	CM1	CM0
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ASEN:** Auto-Scan Enable bit(1)
- 1 = Auto-scan is enabled
- 0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
- 1 = Returns to Low-Power mode after scan
- 0 = Remains in Full-Power mode after scan

bit 13 **CTMREQ:** CTMU Request bit
- 1 = CTMU is enabled when the A/D is enabled and active
- 0 = CTMU is not enabled by the A/D

bit 12 **BGREQ:** Band Gap Request bit
- 1 = Band gap is enabled when the A/D is enabled and active
- 0 = Band gap is not enabled by the A/D

bit 11 **Reserved:** Maintain as ‘0’

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits
- 11 = Interrupt after a Threshold Detect sequence completed and a valid compare has occurred
- 10 = Interrupt after a valid compare has occurred
- 01 = Interrupt after a Threshold Detect sequence completed
- 00 = No interrupt

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-2 **WM<1:0>:** Write Mode bits
- 11 = Reserved
- 10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match, as defined by the CMx and ASINTx bits, occurs)
- 01 = Convert and save (conversion results are saved to locations as determined by the register bits when a match, as defined by the CMx bits, occurs)
- 00 = Legacy operation (conversion data is saved to a location determined by the buffer register bits)

bit 1-0 **CM<1:0>:** Compare Mode bits
- 11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
- 10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
- 01 = Greater Than mode (valid match occurs if the result is greater than the value in the corresponding buffer register)
- 00 = Less Than mode (valid match occurs if the result is less than the value in the corresponding buffer register)

Note 1: When using auto-scan with Threshold Detect (ASEN = 1), do not configure the sample clock source to Auto-Convert mode (SSRCx = 7). Any other available SSRCx selection is valid. To use auto-convert as the sample clock source (SSRCx = 7), make sure ASEN is cleared.

REGISTER 25-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = Edge 1 source is Comparator 3 output
1110 = Edge 1 source is Comparator 2 output
1101 = Edge 1 source is Comparator 1 output
1100 = Edge 1 source is IC3
1011 = Edge 1 source is IC2
1010 = Edge 1 source is IC1
1001 = Edge 1 source is CTED8
1000 = Edge 1 source is CTED7
0111 = Edge 1 source is CTED6
0110 = Edge 1 source is CTED5
0101 = Edge 1 source is CTED4
0100 = Edge 1 source is CTED3(2)
0011 = Edge 1 source is CTED1
0010 = Edge 1 source is CTED2
0001 = Edge 1 source is OC1
0000 = Edge 1 source is Timer1

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the current source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the current source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

Note 1: Edge sources, CTED11 and CTED12, are not available on PIC24FV32KA302 devices.
2: Edge sources, CTED3, CTED11, CTED12 and CTED13, are not available on PIC24FV32KA301 devices.

TABLE 28-2: INSTRUCTION SET OVERVIEW

Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
ADD	ADD f	f = f + WREG	1	1	C, DC, N, OV, Z
	ADD f,WREG	WREG = f + WREG	1	1	C, DC, N, OV, Z
	ADD #lit10,Wn	Wd = lit10 + Wd	1	1	C, DC, N, OV, Z
	ADD Wb,Ws,Wd	Wd = Wb + Ws	1	1	C, DC, N, OV, Z
	ADD Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C, DC, N, OV, Z
ADDC	ADDC f	f = f + WREG + (C)	1	1	C, DC, N, OV, Z
	ADDC f,WREG	WREG = f + WREG + (C)	1	1	C, DC, N, OV, Z
	ADDC #lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C, DC, N, OV, Z
	ADDC Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C, DC, N, OV, Z
	ADDC Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C, DC, N, OV, Z
AND	AND f	f = f .AND. WREG	1	1	N, Z
	AND f,WREG	WREG = f .AND. WREG	1	1	N, Z
	AND #lit10,Wn	Wd = lit10 .AND. Wd	1	1	N, Z
	AND Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N, Z
	AND Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N, Z
ASR	ASR f	f = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR f,WREG	WREG = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C, N, OV, Z
	ASR Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N, Z
	ASR Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N, Z
BCLR	BCLR f,#bit4	Bit Clear f	1	1	None
	BCLR Ws,#bit4	Bit Clear Ws	1	1	None
BRA	BRA C,Expr	Branch if Carry	1	1 (2)	None
	BRA GE,Expr	Branch if Greater than or Equal	1	1 (2)	None
	BRA GEU,Expr	Branch if Unsigned Greater than or Equal	1	1 (2)	None
	BRA GT,Expr	Branch if Greater than	1	1 (2)	None
	BRA GTU,Expr	Branch if Unsigned Greater than	1	1 (2)	None
	BRA LE,Expr	Branch if Less than or Equal	1	1 (2)	None
	BRA LEU,Expr	Branch if Unsigned Less than or Equal	1	1 (2)	None
	BRA LT,Expr	Branch if Less than	1	1 (2)	None
	BRA LTU,Expr	Branch if Unsigned Less than	1	1 (2)	None
	BRA N,Expr	Branch if Negative	1	1 (2)	None
	BRA NC,Expr	Branch if Not Carry	1	1 (2)	None
	BRA NN,Expr	Branch if Not Negative	1	1 (2)	None
	BRA NOV,Expr	Branch if Not Overflow	1	1 (2)	None
	BRA NZ,Expr	Branch if Not Zero	1	1 (2)	None
	BRA OV,Expr	Branch if Overflow	1	1 (2)	None
	BRA Expr	Branch Unconditionally	1	2	None
	BRA Z,Expr	Branch if Zero	1	1 (2)	None
	BRA Wn	Computed Branch	1	2	None
BSET	BSET f,#bit4	Bit Set f	1	1	None
	BSET Ws,#bit4	Bit Set Ws	1	1	None
BSW	BSW.C Ws,Wb	Write C bit to Ws<Wb>	1	1	None
	BSW.Z Ws,Wb	Write Z bit to Ws<Wb>	1	1	None
BTG	BTG f,#bit4	Bit Toggle f	1	1	None
	BTG Ws,#bit4	Bit Toggle Ws	1	1	None
BTSC	BTSC f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
	BTSC Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None

29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC24FV32KA304 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FV32KA304 family devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(†)

Ambient temperature under bias..-40°C to +135°C
Storage temperature .... -65°C to +150°C
Voltage on VDD with respect to VSS (PIC24FVXXKA30X) .... -0.3V to +6.5V
Voltage on VDD with respect to VSS (PIC24FXXKA30X) .... -0.3V to +4.5V
Voltage on any combined analog and digital pin with respect to VSS .... -0.3V to (VDD + 0.3V)
Voltage on any digital only pin with respect to VSS .... -0.3V to (VDD + 0.3V)
Voltage on $\overline{\text{MCLR}}$/VPP pin with respect to VSS .... -0.3V to +9.0V
Maximum current out of VSS pin ....300 mA
Maximum current into VDD pin(1)..250 mA
Maximum output current sunk by any I/O pin...25 mA
Maximum output current sourced by any I/O pin ....25 mA
Maximum current sunk by all ports ....200 mA
Maximum current sourced by all ports(1)...200 mA

Note 1: Maximum allowable current is a function of the device maximum power dissipation (see Table 29-1).

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 30-20: TYPICAL ΔI_{DSBOR} vs. V_{DD}

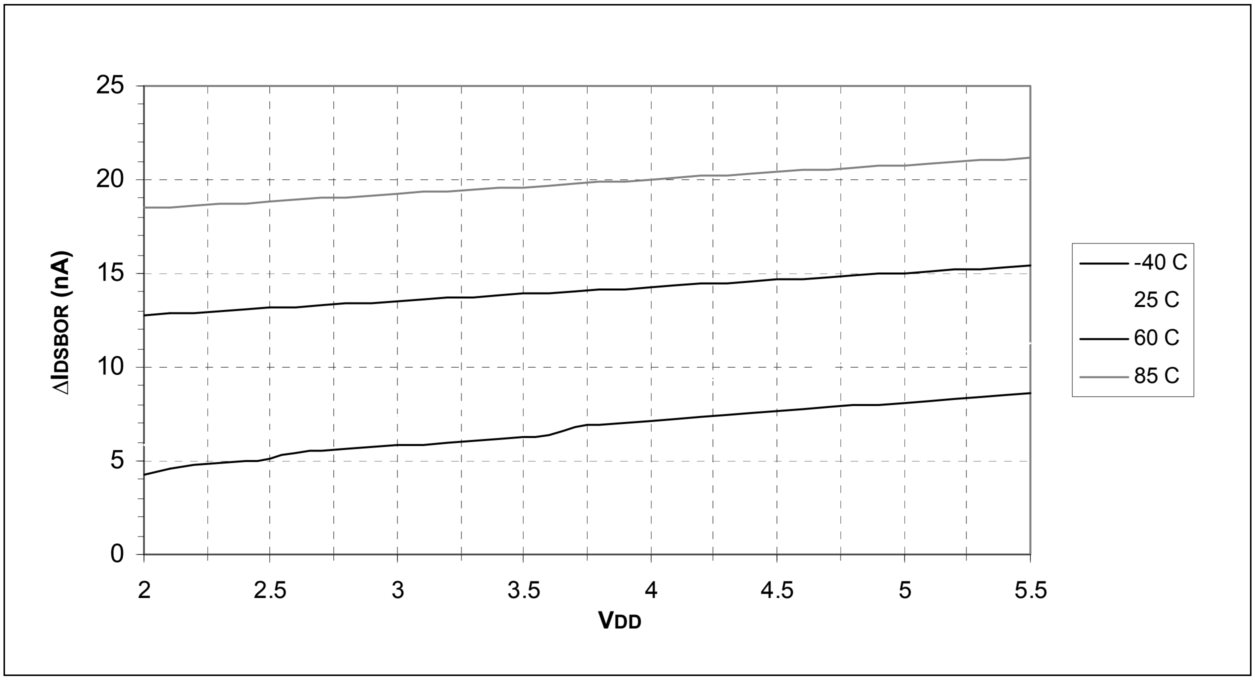
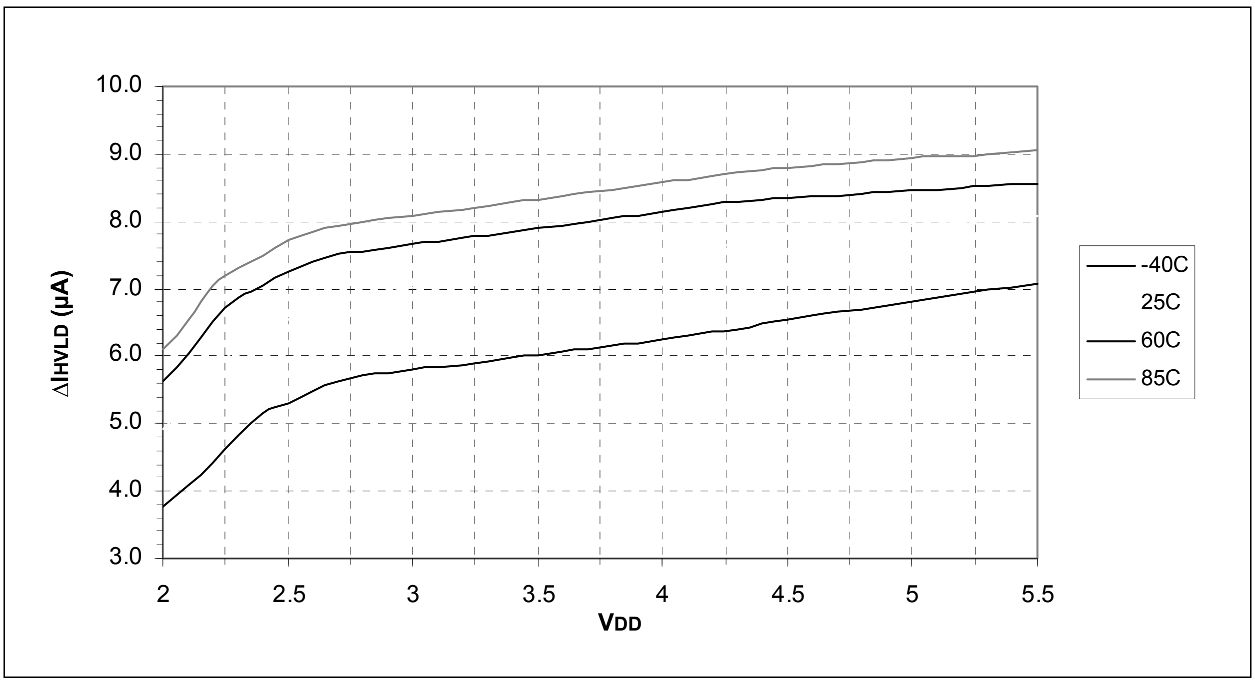
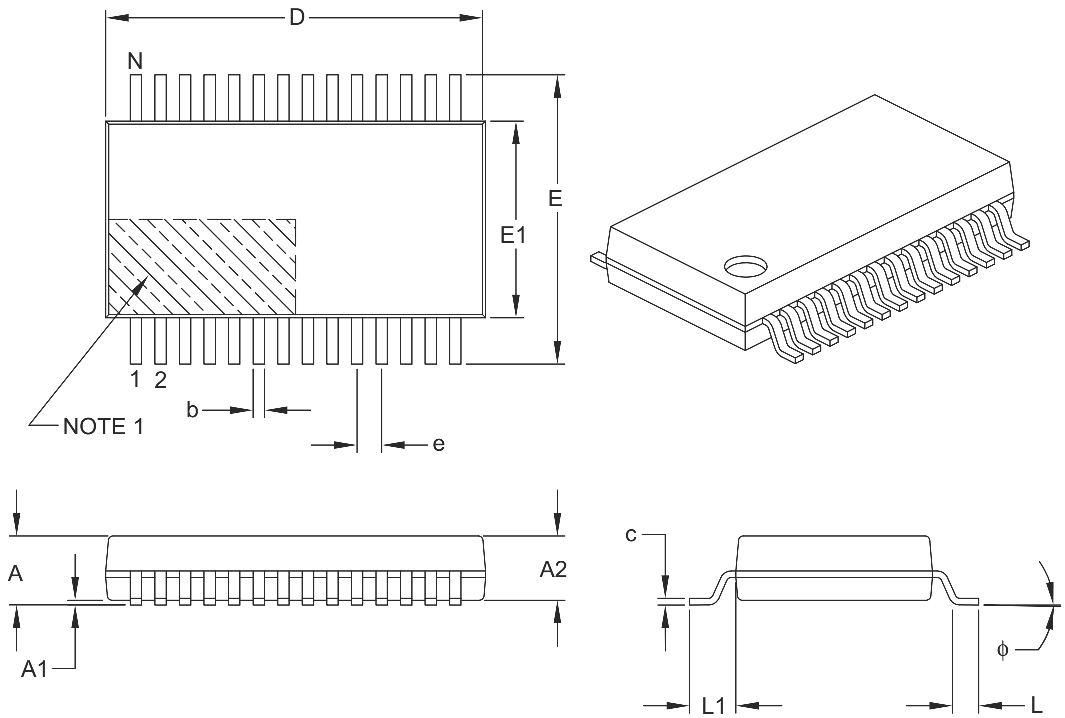


FIGURE 30-21: TYPICAL ΔI_{HLVD} vs. V_{DD}



28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS	
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

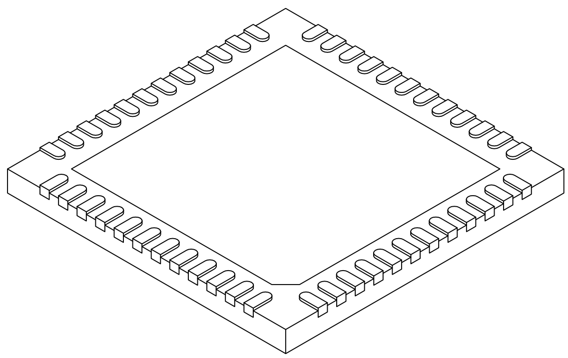
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.45	4.60	4.75
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.45	4.60	4.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision A (March 2011)

Original data sheet for the PIC24FV32KA304 family of devices.

Revision B (April 2011)

Section 25.0 "Charge Time Measurement Unit (CTMU)" was revised to change the description of the IRNGx bits in CTMUICON (Register 25-3). Setting '01' is the base current level (0.55 μA nominal) and setting '00' is 1000x base current.

Section 29.0 "Electrical Characteristics" was revised to change the following typical IPD specifications:

- DC20h/i/j/k from 204 μA to 200 μA
- DC60h/i/j/k from 0.15 μA to 0.025 μA
- DC60l/m/n/o from 0.25 μA to 0.040 μA
- DC72h/i/j/k from 0.80 μA to 0.70 μA

Revision C (April 2012)

Updated the Pin Diagrams on Pages 3 through 7, to change "LVDIN" to "HLVDIN" in all occurrences, and correct the placement of certain functions.

Updated Table 1-3 to remove references to unimplemented package types, corrected several erroneous pin assignments and removed other alternate but unimplemented assignments.

For **Section 5.0 "Flash Program Memory"**, updated Example 5-2, Example 5-3 and Example 5-4 with new table offset functions.

Updated Figure 12-1 to correctly show the implemented Timer1 input options.

For **Section 22.0 "12-Bit A/D Converter with Threshold Detect"**:

- Updated Register 22-1 to add the MODE12 bit
- Updated the descriptions of the PVCFGx and CSCNA bits in Register 22-2
- Updated Register 22-4 to change the VRSREQ bit to a reserved bit position
- Modified footnote text in Register 22-5
- Corrected CHOLD in Figure 22-2

For **Section 25.0 "Charge Time Measurement Unit (CTMU)"**:

- Updated the text in **Section 25.1 "Measuring Capacitance"** and **Section 25.3 "Pulse Generation and Delay"** to better reflect the module's implementation
- Updated Figure 25-3 to show additional detail in pulse generation

Added the following timing diagrams and timing requirement tables to **Section 29.0 "Electrical Characteristics"**:

- Figure 29-6 (Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing Characteristics)
- Figure 29-7 (Brown-out Reset Characteristics)
- Figure 29-9 (Input Capture x Timings) through Figure 29-21 (SPIx Module Slave Mode Timing Characteristics (CKE = 1))
- Table 29-28 (Input Capture x Requirements) through Table 29-39 (SPIx Module Slave Mode Timing Requirements (CKE = 1))
- Figure 29-22 (A/D Conversion Timing)

Updated Table 29-5 to add specification, DC15.

Replaced Table 29-6, Table 29-7 and Table 29-8 with new, shorter versions that remove unimplemented temperature options. (No existing specification values have been changed in this process.)

Updated Table 29-16 with correct values for CTMUICON bit settings.

Combined previous Table 29-21 and Table 29-22 to create a new Table 29-21 (AC Characteristics: Internal RC Accuracy). All existing subsequent tables are renumbered accordingly.

Updated Table 29-26 to add specifications, SY35 and SY55.

Updated Table 29-40:

- Split AD01 into separate entries for "F" and "FV" device families
- Added specifications, AD08 (IVREF) and AD09 (ZVREF)
- Changed AD17 (2.5 kΩ max. to 1 kΩ max.)

Updated Table 29-41:

- Changed AD50 (75 ns min. to 600 ns min.)
- Changed AD51 (250 ns typ. to 1.67 μs typ.)
- Changed AD60 (0.5 TAD min. to 2 TAD min.)
- Split AD55 into separate entries for 10-bit and 12-bit conversions

Added **Section 30.0 "DC and AC Characteristics Graphs and Tables"**, with Figure 30-1 through Figure 30-39.

Replaced some of the packaging diagrams in **Section 31.0 "Packaging Information"** with the newly revised diagrams.

Other minor typographic corrections throughout.

