What is "<u>Embedded - Microcontrollers</u>"?

"<u>Embedded - Microcontrollers</u>" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
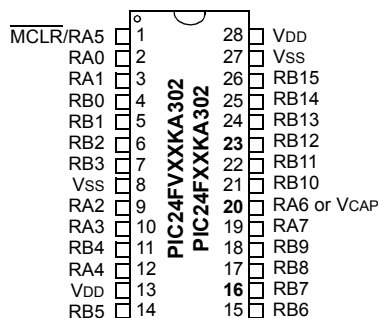
Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16ka301-e-p

Pin Diagrams

28-Pin SPDIP/SSOP/SOIC[1,2]

```
                    MCLR/RA5 □ 1      28 □ VDD
                        RA0 □ 2      27 □ VSS
                        RA1 □ 3      26 □ RB15
                        RB0 □ 4      25 □ RB14
                        RB1 □ 5      24 □ RB13
                        RB2 □ 6      23 □ RB12
                        RB3 □ 7      22 □ RB11
                        VSS □ 8      21 □ RB10
                        RA2 □ 9      20 □ RA6 or VCAP
                        RA3 □ 10     19 □ RA7
                        RB4 □ 11     18 □ RB9
                        RA4 □ 12     17 □ RB8
                        VDD □ 13     16 □ RB7
                        RB5 □ 14     15 □ RB6
```
PIC24FVXXKA302
PIC24FXXKA302

Pin	Pin Features	
	PIC24FVXXKA302	**PIC24FXXKA302**
1	MCLR/VPP/RA5	MCLR/VPP/RA5
2	VREF+/CVREF+/AN0/C3INC/CTED1/CN2/RA0	VREF+/CVREF+/AN0/C3INC/CTED1/CN2/RA0
3	CVREF-/VREF-/AN1/CN3/RA1	CVREF-/VREF-/AN1/CN3/RA1
4	PGED1/AN2/ULPWU/CTCMP/C1IND/C2INB/C3IND/U2TX/CN4/RB0	PGED1/AN2/ULPWU/CTCMP/C1IND/C2INB/C3IND/U2TX/CN4/RB0
5	PGEC1/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1	PGEC1/AN3/C1INC/C2INA/U2RX/CN5/RB1
6	AN4/C1INB/C2IND/SDA2/T5CK/T4CK/U1RX/CTED13/CN6/RB2	AN4/C1INB/C2IND/SDA2/T5CK/T4CK/U1RX/CTED13/CN6/RB2
7	AN5/C1INA/C2INC/SCL2/CN7/RB3	AN5/C1INA/C2INC/SCL2/CN7/RB3
8	VSS	VSS
9	OSCI/AN13/CLKI/CN30/RA2	OSCI/AN13/CLKI/CN30/RA2
10	OSCO/AN14/CLKO/CN29/RA3	OSCO/AN14/CLKO/CN29/RA3
11	SOSCI/AN15/U2RTS/CN1/RB4	SOSCI/AN15/U2RTS/CN1/RB4
12	SOSCO/SCLKI/U2CTS/CN0/RA4	SOSCO/SCLKI/U2CTS/CN0/RA4
13	VDD	VDD
14	PGED3/ASDA[1]/SCK2/CN27/RB5	PGED3/ASDA[1]/SCK2/CN27/RB5
15	PGEC3/ASCL[1]/SDO2/CN24/RB6	PGEC3/ASCL[1]/SDO2/CN24/RB6
16	**U1TX/C2OUT/OC1/INT0/CN23/RB7**	**U1TX/INT0/CN23/RB7**
17	SCL1/U1CTS/C3OUT/CTED10/CN22/RB8	SCL1/U1CTS/C3OUT/CTED10/CN22/RB8
18	SDA1/T1CK/U1RTS/IC2/CTED4/CN21/RB9	SDA1/T1CK/U1RTS/IC2/CTED4/CN21/RB9
19	SDI2/IC1/CTED3/CN9/RA7	SDI2/IC1/CTED3/CN9/RA7
20	**VCAP**	**C2OUT/OC1/CTED1/INT2/CN8/RA6**
21	PGED2/SDI1/OC3/CTED11/CN16/RB10	PGED2/SDI1/OC3/CTED11/CN16/RB10
22	PGEC2/SCK1/OC2/CTED9/CN15/RB11	PGEC2/SCK1/OC2/CTED9/CN15/RB11
23	**AN12/HLVDIN/SS2/IC3/CTED2/INT2/CN14/RB12**	**AN12/HLVDIN/SS2/IC3/CTED2/CN14/RB12**
24	AN11/SDO1/OCFB/CTPLS/CN13/RB13	AN11/SDO1/OCFB/CTPLS/CN13/RB13
25	CVREF/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/**INT1/**CN12/RB14	CVREF/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/**INT1/**CN12/RB14
26	AN9/C3INA/T3CK/T2CK/REFO/SS1/CTED6/CN11/RB15	AN9/C3INA/T3CK/T2CK/REFO/SS1/CTED6/CN11/RB15
27	VSS/AVSS	VSS/AVSS
28	VDD/AVDD	VDD/AVDD

Legend: Pin numbers in **bold** indicate pin function differences between PIC24FV and PIC24F devices.

Note 1: Alternative multiplexing for SDA1 (ASDA1) and SCL1 (ASCL1) when the I2CSEL Configuration bit is set.

2: PIC24F32KA304 device pins have a maximum voltage of 3.6V and are not 5V tolerant.

PIC24FV32KA304 FAMILY

TABLE 1-3:   PIC24FV32KA304 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
CN23	11	16	13	43	47	11	16	13	43	47	I	ST	Interrupt-on-Change Inputs
CN24	—	15	12	42	46	—	15	12	42	46	I	ST	
CN25	—	—	—	37	40	—	—	—	37	40	I	ST	
CN26	—	—	—	38	41	—	—	—	38	41	I	ST	
CN27	—	14	11	41	45	—	14	11	41	45	I	ST	
CN28	—	—	—	36	39	—	—	—	36	39	I	ST	
CN29	8	10	7	31	34	8	10	7	31	34	I	ST	
CN30	7	9	6	30	33	7	9	6	30	33	I	ST	
CN31	—	—	—	26	28	—	—	—	26	28	I	ST	
CN32	—	—	—	25	27	—	—	—	25	27	I	ST	
CN33	—	—	—	32	35	—	—	—	32	35	I	ST	
CN34	—	—	—	35	38	—	—	—	35	38	I	ST	
CN35	—	—	—	12	13	—	—	—	12	13	I	ST	
CN36	—	—	—	13	14	—	—	—	13	14	I	ST	
CVREF	17	25	22	14	15	17	25	22	14	15	I	ANA	Comparator Voltage Reference Output
CVREF+	2	2	27	19	21	2	2	27	19	21	I	ANA	Comparator Reference Positive Input Voltage
CVREF-	3	3	28	20	22	3	3	28	20	22	I	ANA	Comparator Reference Negative Input Voltage
CTCMP	4	4	1	21	23	4	4	1	21	23	I	ANA	CTMU Comparator Input
CTED1	14	20	17	7	7	11	2	27	19	21	I	ST	CTMU Trigger Edge Inputs
CTED2	15	23	20	10	11	15	23	20	10	11	I	ST	
CTED3	—	19	16	6	6	—	19	16	6	6	I	ST	
CTED4	13	18	15	1	1	13	18	15	1	1	I	ST	
CTED5	17	25	22	14	15	17	25	22	14	15	I	ST	
CTED6	18	26	23	15	16	18	26	23	15	16	I	ST	
CTED7	—	—	—	5	5	—	—	—	5	5	I	ST	
CTED8	—	—	—	13	14	—	—	—	13	14	I	ST	
CTED9	—	22	19	9	10	—	22	19	9	10	I	ST	
CTED10	12	17	14	44	48	12	17	14	44	48	I	ST	
CTED11	—	21	18	8	9	—	21	18	8	9	I	ST	
CTED12	5	5	2	22	24	5	5	2	22	24	I	ST	
CTED13	6	6	3	23	25	6	6	3	23	25	I	ST	

4.2.5 SOFTWARE STACK

In addition to its use as a working register, the W15 register in PIC24F devices is also used as a Software Stack Pointer. The pointer always points to the first available free word and grows from lower to higher addresses. It predecrements for stack pops and post-increments for stack pushes, as shown in Figure 4-4.

Note that for a PC push during any `CALL` instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

> **Note:** A PC push during exception processing will concatenate the SRL register to the MSB of the PC prior to the push.

The Stack Pointer Limit Value (SPLIM) register, associated with the Stack Pointer, sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' as all stack operations must be word-aligned. Whenever an EA is generated, using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal, and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation.

Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address, 0DF6 in RAM, initialize the SPLIM with the value, 0DF4.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0800h. This prevents the stack from interfering with the Special Function Register (SFR) space.

> **Note:** A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-4: **`CALL` STACK FRAME**
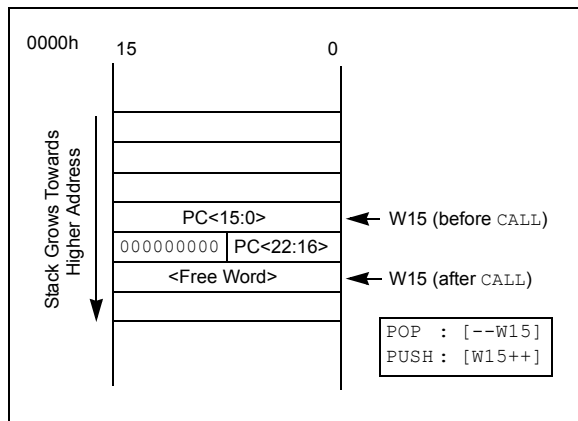
4.3 Interfacing Program and Data Memory Spaces

The PIC24F architecture uses a 24-bit wide program space and 16-bit wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Apart from the normal execution, the PIC24F architecture provides two methods by which the program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the data space, PSV

Table instructions allow an application to read or write small areas of the program memory. This makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. It can only access the least significant word (lsw) of the program word.

4.3.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Memory Page Address register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the Most Significant bit (MSb) of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = 0) or the configuration memory (TBLPAG<7> = 1).

For remapping operations, the 8-bit Program Space Visibility Page Address register (PSVPAG) is used to define a 16K word page in the program space. When the MSb of the EA is '1', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike the table operations, this limits remapping operations strictly to the user memory area.

Table 4-27 and Figure 4-5 show how the program EA is created for table operations and remapping accesses from the data EA. Here, the P<23:0> bits refer to a program space word, whereas the D<15:0> bits refer to a data space word.
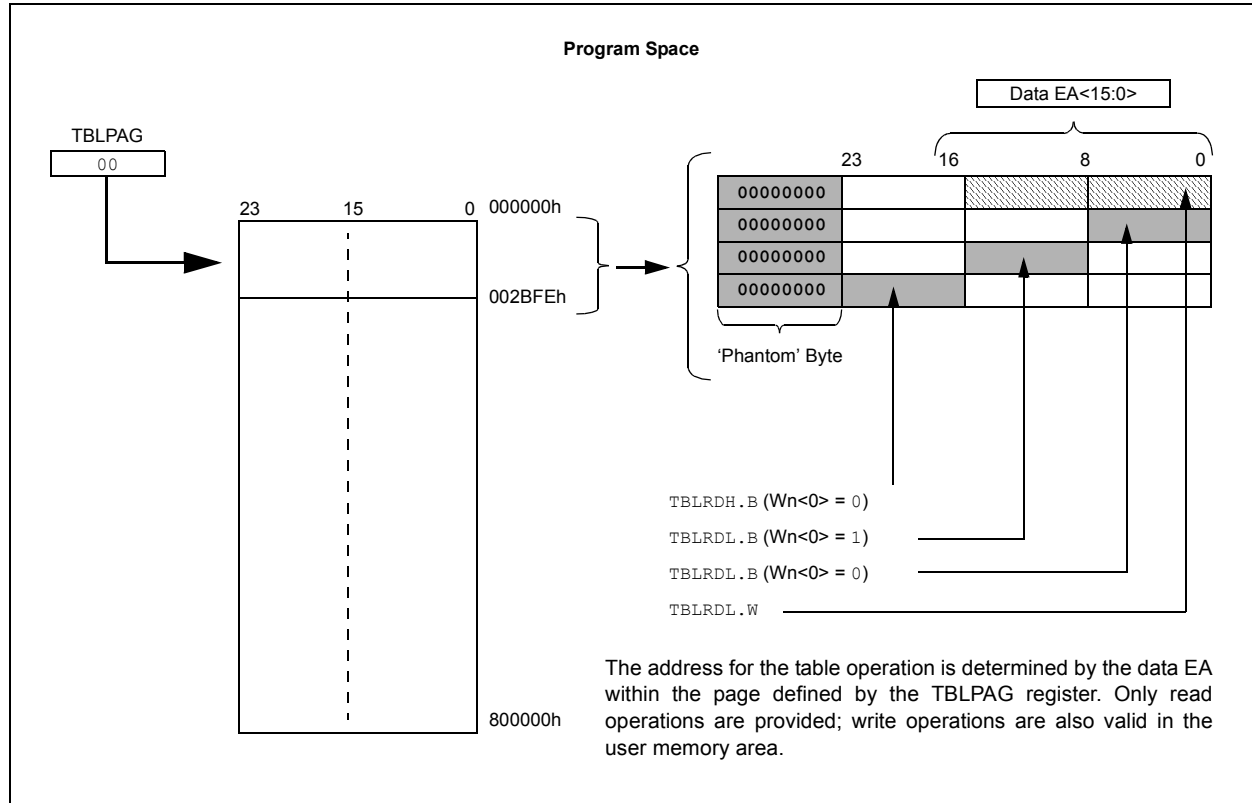
In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When

TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

Note:	Only Table Read operations will execute in the configuration memory space, and only then, in implemented areas, such as the Device ID. Table write operations are not allowed.

FIGURE 4-6: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

The address for the table operation is determined by the data EA within the page defined by the TBLPAG register. Only read operations are provided; write operations are also valid in the user memory area.

7.0 RESETS

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Resets, refer to the *"PIC24F Family Reference Manual"*, **Section 40. "Reset with Programmable Brown-out Reset"** (DS39728).

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Pin Reset
- SWR: `RESET` Instruction
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- Low-Power BOR/Deep Sleep BOR
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode Reset
- UWR: Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 7-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on Power-on Reset (POR) and unchanged by all other Resets.

> **Note:** Refer to the specific peripheral or **Section 3.0 "CPU"** of this data sheet for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). A Power-on Reset will clear all bits except for the BOR and POR bits (RCON<1:0>) which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer (WDT) and device power-saving states. The function of these bits is discussed in other sections of this manual.

> **Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

FIGURE 7-1: RESET SYSTEM BLOCK DIAGRAM
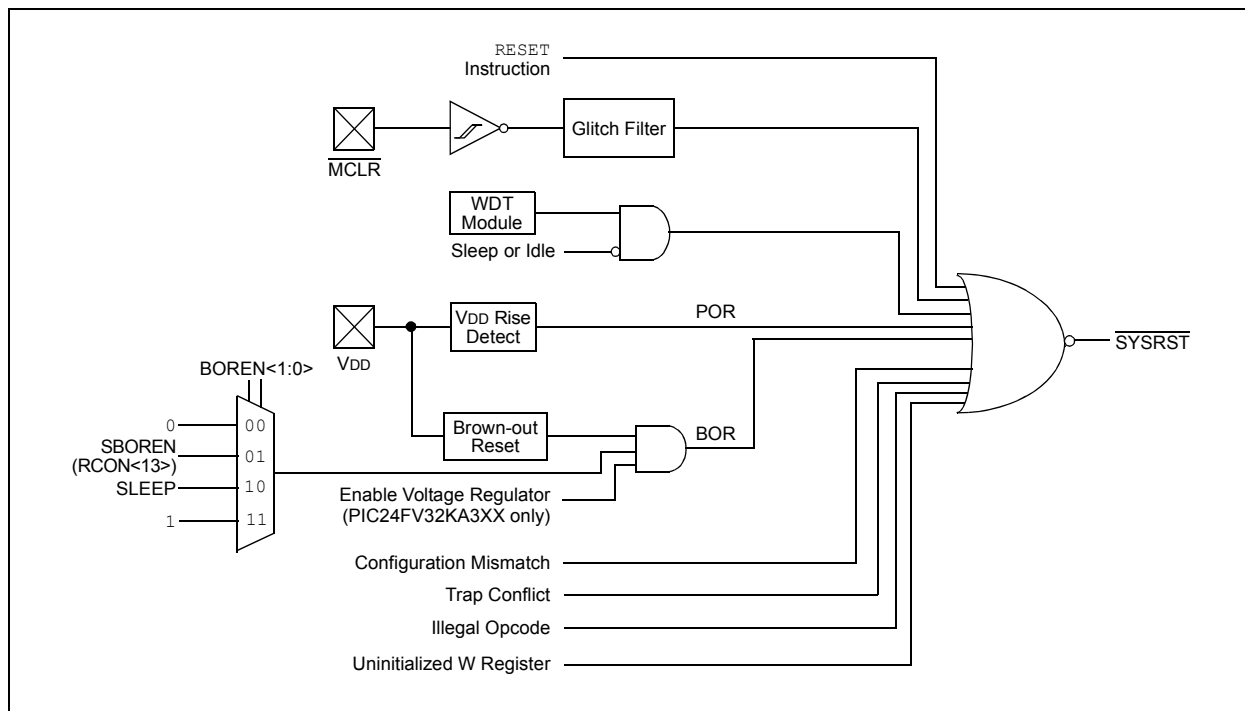
REGISTER 8-17:   IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **T1IP<2:0>:** Timer1 Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **OC1IP<2:0>:** Output Compare Channel 1 Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **IC1IP<2:0>:** Input Capture Channel 1 Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **INT0IP<2:0>:** External Interrupt 0 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

PIC24FV32KA304 FAMILY

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

11.2 Configuring Analog Port Pins

The use of the ANS and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRISx bit set (input). If the TRISx bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

11.2.1 ANALOG SELECTION REGISTERS

I/O pins with shared analog functionality, such as A/D inputs and comparator inputs, must have their digital inputs shut off when analog functionality is used. Note that analog functionality includes an analog voltage being applied to the pin externally.

To allow for analog control, the ANSx registers are provided. There is one ANS register for each port (ANSA, ANSB and ANSC). Within each ANSx register, there is a bit for each pin that shares analog functionality with the digital I/O functionality.

If a particular pin does not have an analog function, that bit is unimplemented. See Register 11-1 to Register 11-3 for implementation.

REGISTER 11-1: ANSA: ANALOG SELECTION (PORTA)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3-0 **ANSA<3:0>:** Analog Select Control bits

1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

16.0 SERIAL PERIPHERAL INTERFACE (SPI)

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Serial Peripheral Interface, refer to the *"PIC24F Family Reference Manual"*, **Section 23. "Serial Peripheral Interface (SPI)"** (DS39699).

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial data EEPROMs, shift registers, display drivers, A/D Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

The module supports operation in two buffer modes. In Standard mode, data is shifted through a single serial buffer. In Enhanced Buffer mode, data is shifted through an 8-level FIFO buffer.

> **Note:** Do not perform read-modify-write operations (such as bit-oriented instructions) on the SPI1BUF register in either Standard or Enhanced Buffer mode.

The module also supports a basic framed SPI protocol while operating in either Master or Slave mode. A total of four framed SPI configurations are supported.

The SPI serial interface consists of four pins:

- SDI1: Serial Data Input
- SDO1: Serial Data Output
- SCK1: Shift Clock Input or Output
- SS1: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPI module can be configured to operate using 2, 3 or 4 pins. In the 3-pin mode, SS1 is not used. In the 2-pin mode, both SDO1 and SS1 are not used.

Block diagrams of the module, in Standard and Enhanced Buffer modes, are shown in Figure 16-1 and Figure 16-2.

The devices of the PIC24FV32KA304 family offer two SPI modules on a device.

> **Note:** In this section, the SPI modules are referred to as SPIx. Special Function Registers (SFRs) will follow a similar notation. For example, SPI1CON1 or SPI1CON2 refers to the control register for the SPI1 module.

To set up the SPI1 module for the Standard Master mode of operation:

1. If using interrupts:
   a) Clear the SPI1IF bit in the IFS0 register.
   b) Set the SPI1IE bit in the IEC0 register.
   c) Write the respective SPI1IPx bits in the IPC2 register to set the interrupt priority.
2. Write the desired settings to the SPI1CON1 and SPI1CON2 registers with the MSTEN bit (SPI1CON1<5>) = 1.
3. Clear the SPIROV bit (SPI1STAT<6>).
4. Enable SPI operation by setting the SPIEN bit (SPI1STAT<15>).
5. Write the data to be transmitted to the SPI1BUF register. Transmission (and reception) will start as soon as data is written to the SPI1BUF register.

To set up the SPI1 module for the Standard Slave mode of operation:

1. Clear the SPI1BUF register.
2. If using interrupts:
   a) Clear the SPI1IF bit in the IFS0 register.
   b) Set the SPI1IE bit in the IEC0 register.
   c) Write the respective SPI1IPx bits in the IPC2 register to set the interrupt priority.
3. Write the desired settings to the SPI1CON1 and SPI1CON2 registers with the MSTEN bit (SPI1CON1<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit (SPI1CON1<7>) must be set to enable the SS1 pin.
6. Clear the SPIROV bit (SPI1STAT<6>).
7. Enable SPI operation by setting the SPIEN bit (SPI1STAT<15>).

REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	RBF	TBF
bit 7							bit 0

Legend:			
	C = Clearable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ACKSTAT:** Acknowledge Status bit

1 = NACK was detected last
0 = ACK was detected last
Hardware is set or clear at the end of Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit
(when operating as I^{2}C master; applicable to master transmit operation)

1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of the master transmission; hardware is clear at the end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit

1 = A bus collision has been detected during a master operation
0 = No collision
Hardware is set at the detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit

1 = General call address was received
0 = General call address was not received
Hardware is set when an address matches the general call address; hardware is clear at Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit

1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at a match of the 2nd byte of the matched 10-bit address; hardware is clear at Stop detection.

bit 7 **IWCOL:** I2Cx Write Collision Detect bit

1 = An attempt to write to the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision
Hardware is set at an occurrence of a write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit

1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D/$\overline{\text{A}}$:** Data/$\overline{\text{Address}}$ bit (when operating as I^{2}C slave)

1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was the device address
Hardware is clear at a device address match; hardware is set by a write to I2CxTRN or by reception of a slave byte.

REGISTER 22-2: AD1CON2: A/D CONTROL REGISTER 2 (CONTINUED)

bit 0   **ALTS:** Alternate Input Sample Mode Select bit

         1 = Uses channel input selects for Sample A on the first sample and Sample B on the next sample
         0 = Always uses channel input selects for Sample A

Note 1: This is only applicable when the buffer is used in FIFO mode (BUFREGEN = 0). In addition, BUFS is only used when BUFM = 1.

     2: The voltage reference setting will not be within the specification with V$_{DD}$ below 4.5V.

     3: The voltage reference setting will not be within the specification with V$_{DD}$ below 2.3V.

REGISTER 22-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	R-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	EXTSAM	r	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:		r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **ADRC:** A/D Conversion Clock Source bit

         1 = RC clock
         0 = Clock is derived from the system clock

bit 14   **EXTSAM:** Extended Sampling Time bit

         1 = A/D is still sampling after SAMP = 0
         0 = A/D is finished sampling

bit 13   **Reserved:** Maintain as '0'

bit 12-8   **SAMC<4:0>:** Auto-Sample Time Select bits

         11111 = 31 T$_{AD}$
         •
         •
         •
         00001 = 1 T$_{AD}$
         00000 = 0 T$_{AD}$

bit 7-0   **ADCS<7:0>:** A/D Conversion Clock Select bits

         11111111-01000000 = Reserved
         00111111 = 64 · T$_{CY}$ = T$_{AD}$
         •
         •
         •
         00000001 = 2 · T$_{CY}$ = T$_{AD}$
         00000000 = T$_{CY}$ = T$_{AD}$

REGISTER 26-2: FGS: GENERAL SEGMENT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/C-1	R/C-1
—	—	—	—	—	—	GSS0	GWRP
bit 7							bit 0

Legend:		
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **GSS0:** General Segment Code Flash Code Protection bit

1 = No protection
0 = Standard security is enabled

bit 0 **GWRP:** General Segment Code Flash Write Protection bit

1 = General segment may be written
0 = General segment is write-protected

REGISTER 26-3: FOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	U-0	U-0	R/P-1	R/P-1	R/P-1
IESO	LPRCSEL	SOSCSRC	—	—	FNOSC2	FNOSC1	FNOSC0
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IESO:** Internal External Switchover bit

1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **LPRCSEL:** Internal LPRC Oscillator Power Select bit

1 = High-Power/High-Accuracy mode
0 = Low-Power/Low-Accuracy mode

bit 5 **SOSCSRC:** Secondary Oscillator Clock Source Configuration bit

1 = SOSC analog crystal function is available on the SOSCI/SOSCO pins
0 = SOSC crystal is disabled; digital SCLKI function is selected on the SOSCO pin

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits

000 = Fast RC Oscillator (FRC)
001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCDIV+PLL)
010 = Primary Oscillator (XT, HS, EC)
011 = Primary Oscillator with PLL module (HS+PLL, EC+PLL)
100 = Secondary Oscillator (SOSC)
101 = Low-Power RC Oscillator (LPRC)
110 = 500 kHz Low-Power FRC Oscillator with Divide-by-N (LPFRCDIV)
111 = 8 MHz FRC Oscillator with Divide-by-N (FRCDIV)

TABLE 29-6: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	Device	Typical	Max	Units	Conditions	
I_{DD} Current						
D20	PIC24FV32KA3XX	269	450	µA	2.0V	0.5 MIPS, F_{OSC} = 1 MHz[1]
		465	830	µA	5.0V	
	PIC24F32KA3XX	200	330	µA	1.8V	
		410	750	µA	3.3V	
DC22	PIC24FV32KA3XX	490	—	µA	2.0V	1 MIPS, F_{OSC} = 2 MHz[1]
		880	—	µA	5.0V	
	PIC24F32KA3XX	407	—	µA	1.8V	
		800	—	µA	3.3V	
DC24	PIC24FV32KA3XX	13.0	20.0	mA	5.0V	16 MIPS, F_{OSC} = 32 MHz[1]
	PIC24F32KA3XX	12.0	18.0	mA	3.3V	
DC26	PIC24FV32KA3XX	2.0	—	mA	2.0V	FRC (4 MIPS), F_{OSC} = 8 MHz
		3.5	—	mA	5.0V	
	PIC24F32KA3XX	1.80	—	mA	1.8V	
		3.40	—	mA	3.3V	
DC30	PIC24FV32KA3XX	48.0	250	µA	2.0V	LPRC (15.5 KIPS), F_{OSC} = 31 kHz
		75.0	450	µA	5.0V	
	PIC24F32KA3XX	8.1	28	µA	1.8V	
		13.50	150	µA	3.3V	

Legend: Unshaded rows represent PIC24F32KA3XX devices and shaded rows represent PIC24FV32KA3XX devices.

Note 1: Oscillator is in External Clock mode (FOSCSEL<2:0> = `010`, FOSC<1:0> = `00`).

TABLE 29-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)

DC CHARACTERISTICS					Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	Device	Typical[1]	Max	Units	Conditions		
Module Differential Current (ΔIPD)[3]							
DC71	PIC24FV32KA3XX	0.50	—	µA	-40°C	2.0V	Watchdog Timer Current: ΔIWDT[4]
		0.70	1.5	µA	+85°C	5.0V	
		—	1.5	µA	+125°C	5.0V	
	PIC24F32KA3XX	0.50	—	µA	-40°C	1.8V	
		0.70	1.5	µA	+85°C	3.3V	
		—	1.5	µA	+125°C	3.3V	
DC72	PIC24FV32KA3XX	0.80	—	µA	-40°C	2.0V	32 kHz Crystal with RTCC, DSWDT or Timer1: ΔISOSC (SOSCSEL = 0)[5]
		1.50	2.0	µA	+85°C	5.0V	
		—	2.0	µA	+125°C	5.0V	
	PIC24F32KA3XX	0.70	—	µA	-40°C	1.8V	
		1.0	1.5	µA	+85°C	3.3V	
		—	1.5	µA	+125°C	3.3V	
DC75	PIC24FV32KA3XX	5.4	—	µA	-40°C	2.0V	ΔIHLVD[4]
		8.1	14.0	µA	+85°C	5.0V	
		—	14.0	µA	+125°C	5.0V	
	PIC24F32KA3XX	4.9	—	µA	-40°C	1.8V	
		7.5	14.0	µA	+85°C	3.3V	
		—	14.0	µA	+125°C	3.3V	
DC76	PIC24FV32KA3XX	5.6	—	µA	-40°C	2.0V	ΔIBOR[4]
		6.5	11.2	µA	-40°C	5.0V	
		—	11.2	µA	+125°C	5.0V	
	PIC24F32KA3XX	5.6	—	µA	-40°C	1.8V	
		6.0	11.2	µA	+85°C	3.3V	
		—	11.2	µA	+125°C	3.3V	

Legend: Unshaded rows represent PIC24F32KA3XX devices and shaded rows represent PIC24FV32KA3XX devices.

Note 1: Data in the Typical column is at 3.3V, +25°C (PIC24F32KA3XX) or 5.0V, +25°C (PIC24FV32KA3XX) unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low, PMSLP is set to '0' and WDT, etc., are all switched off.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

4: This current applies to Sleep only.

5: This current applies to Sleep and Deep Sleep.

6: This current applies to Deep Sleep only.
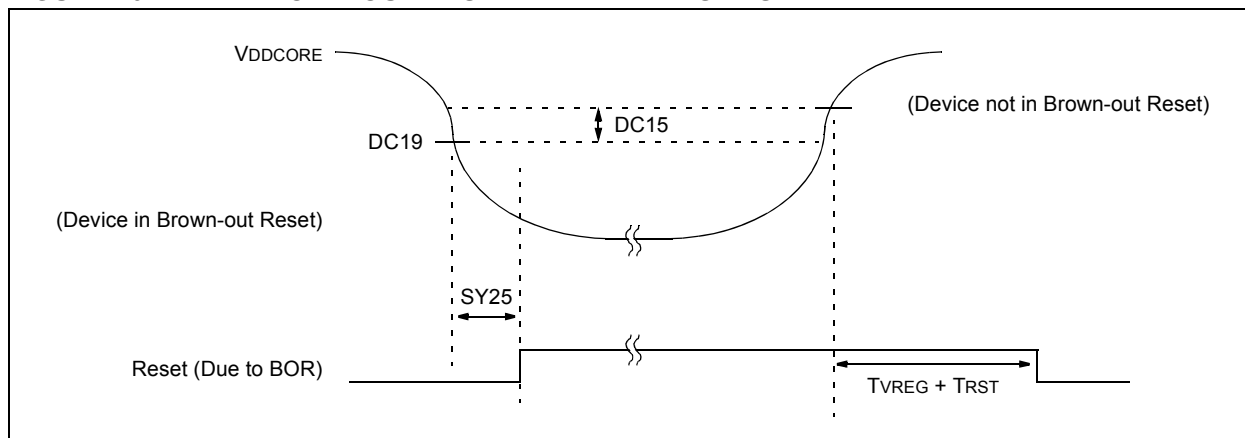
FIGURE 29-7: BROWN-OUT RESET CHARACTERISTICS

TABLE 29-26: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ[1]	Max.	Units	Conditions
SY10	T_{mcL}	$\overline{MCLR}$ Pulse Width (low)	2	—	—	μs	
SY11	T_{PWRT}	Power-up Timer Period	50	64	90	ms	
SY12	T_{POR}	Power-on Reset Delay	1	5	10	μs	
SY13	T_{IOZ}	I/O High-Impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	100	ns	
SY20	T_{WDT}	Watchdog Timer Time-out Period	0.85	1.0	1.15	ms	1.32 prescaler
			3.4	4.0	4.6	ms	1:128 prescaler
SY25	T_{BOR}	Brown-out Reset Pulse Width	1	—	—	μs	
SY35	T_{FSCM}	Fail-Safe Clock Monitor Delay	—	2.0	2.3	μs	
SY45	T_{RST}	Internal State Reset Time	—	5	—	μs	
SY50	T_{VREG}	On-Chip Voltage Regulator Output Delay	—	10	—	μs	**(Note 2)**
SY55	T_{LOCK}	PLL Start-up Time	—	100	—	μs	
SY65	T_{OST}	Oscillator Start-up Time	—	1024	—	T_{OSC}	
SY70	T_{DSWU}	Wake-up from Deep Sleep Time	—	100	—	μs	Based on full discharge of 10 μF capacitor on VCAP; includes T_{POR} and T_{RST}
SY71	T_{PM}	Program Memory Wake-up Time	—	1	—	μs	Sleep wake-up with PMSLP = 0
SY72	T_{LVR}	Retention Regulator Wake-up Time	—	250	—	μs	
SY73	T_{HVLD}	HVLD Interrupt Response Time	—	2	—	μs	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: This applies to PIC24FV32KA3XX devices only.
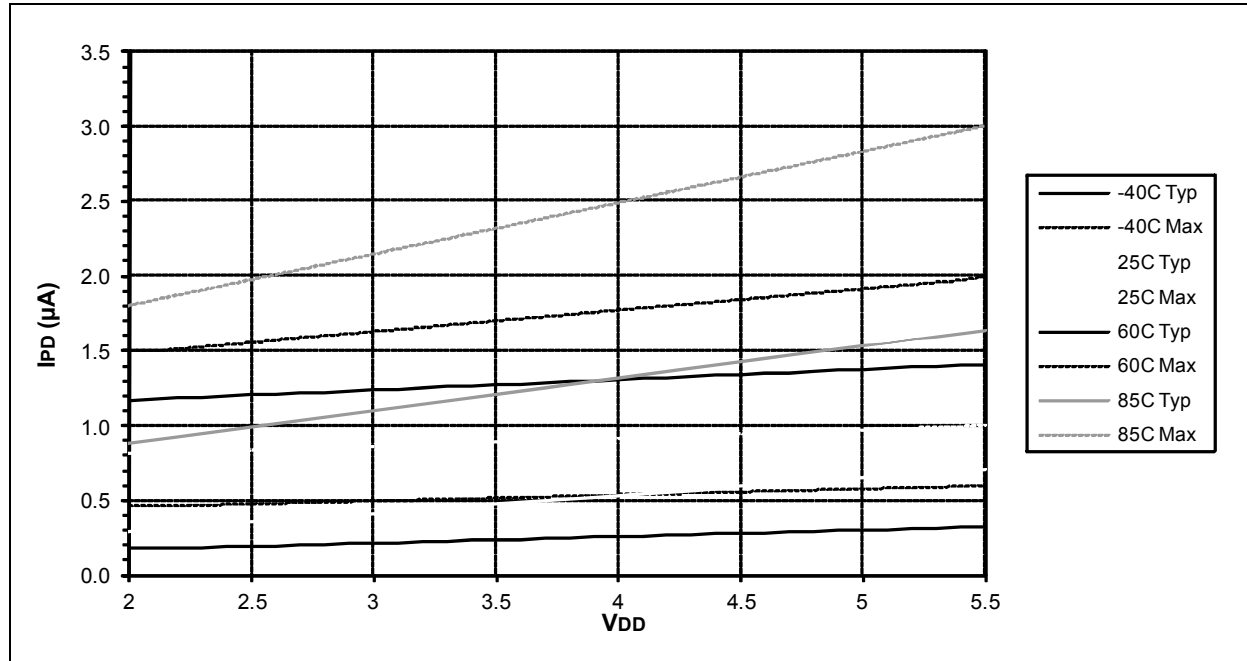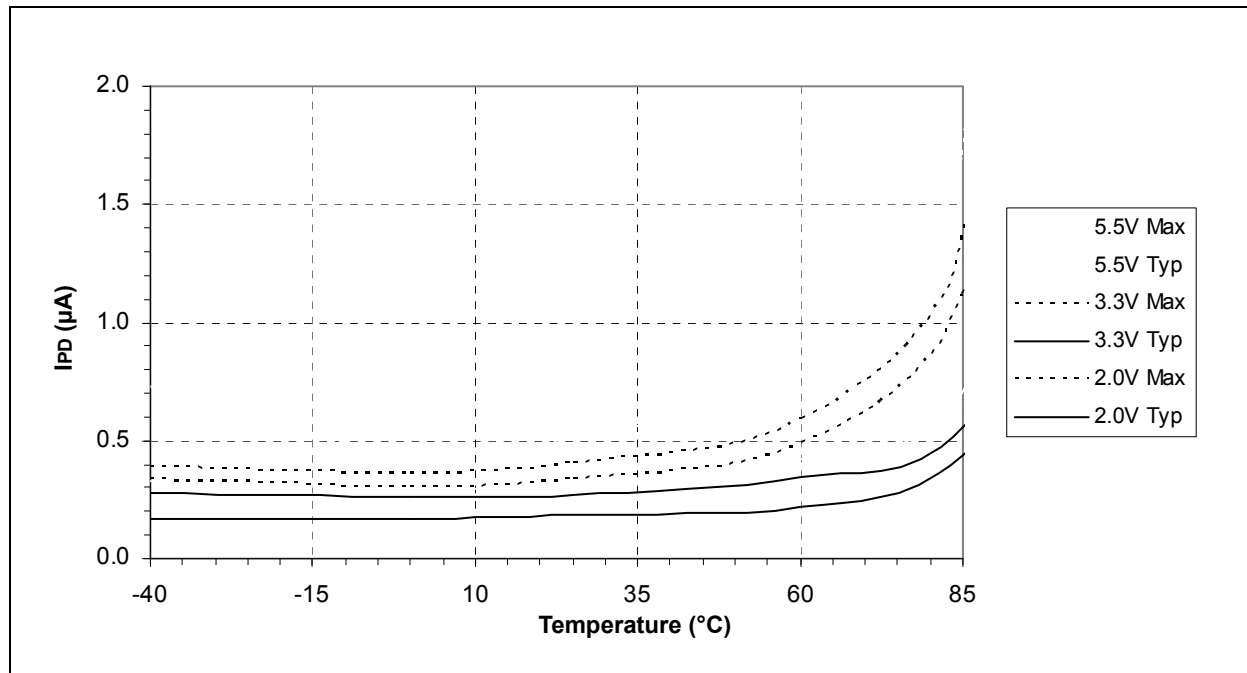
FIGURE 30-14: TYPICAL AND MAXIMUM I$_{PD}$ vs. V$_{DD}$

FIGURE 30-15: TYPICAL AND MAXIMUM I$_{PD}$ vs. TEMPERATURE

FIGURE 30-20: TYPICAL ΔI$_{DSBOR}$ vs. V$_{DD}$

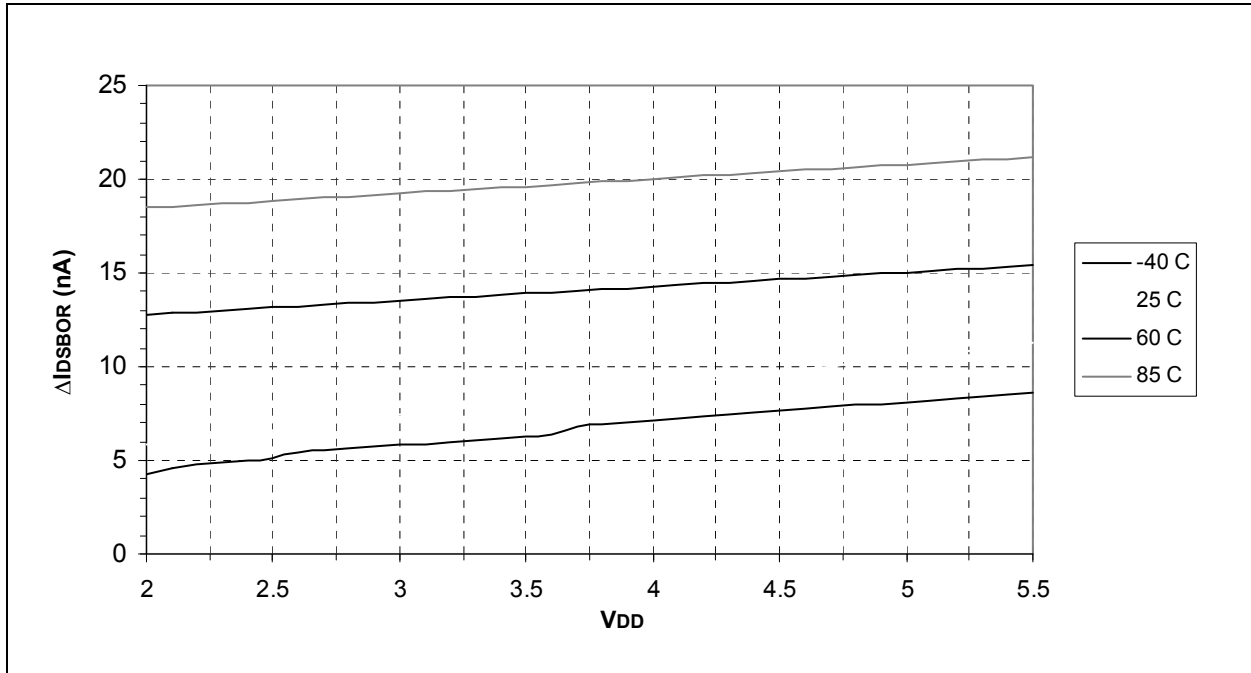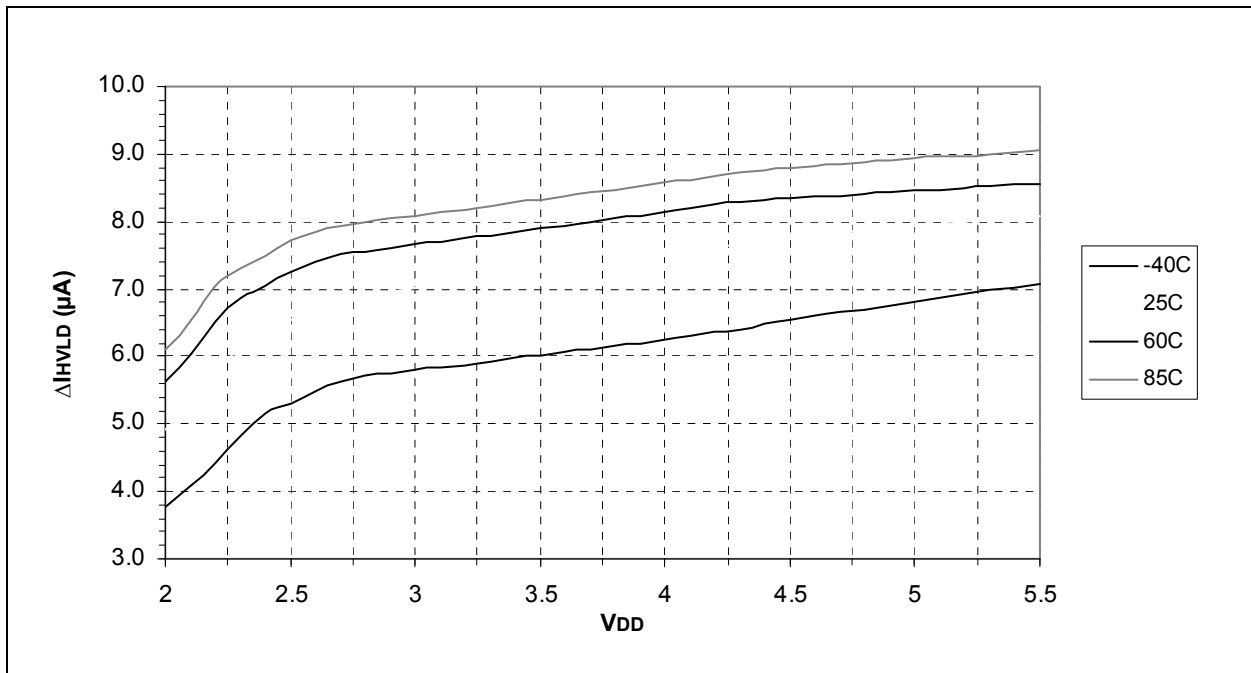**FIGURE 30-21:** TYPICAL ΔI$_{HLVD}$ vs. V$_{DD}$

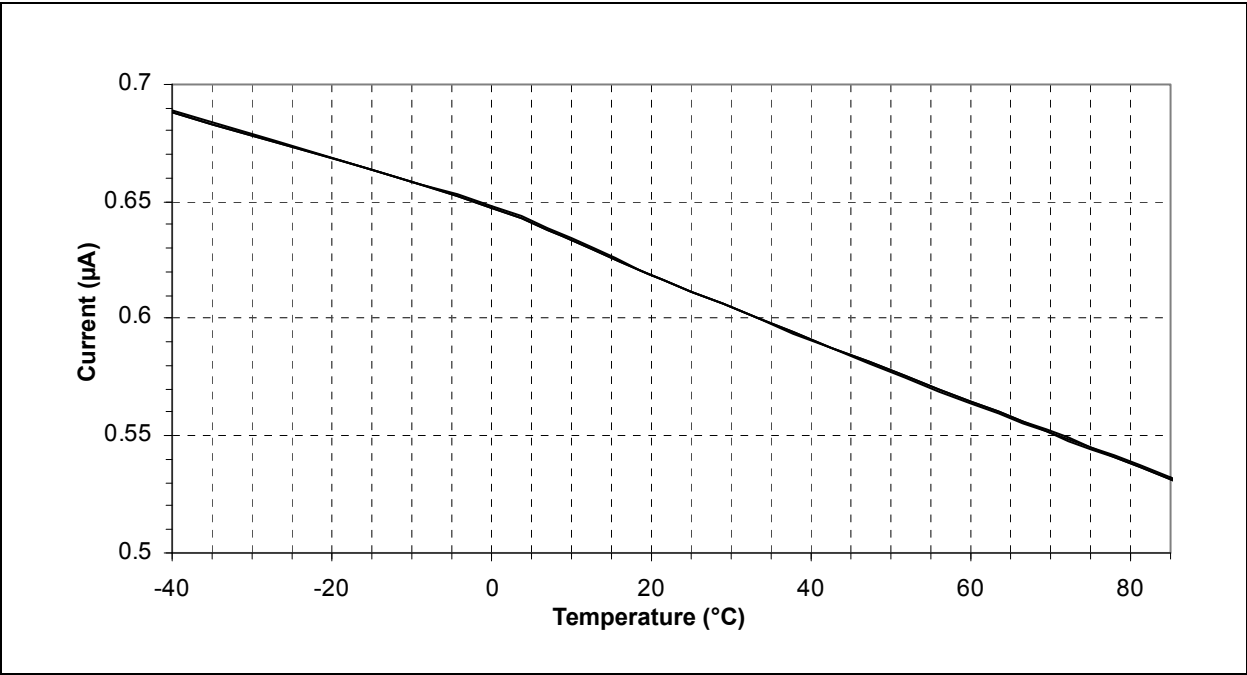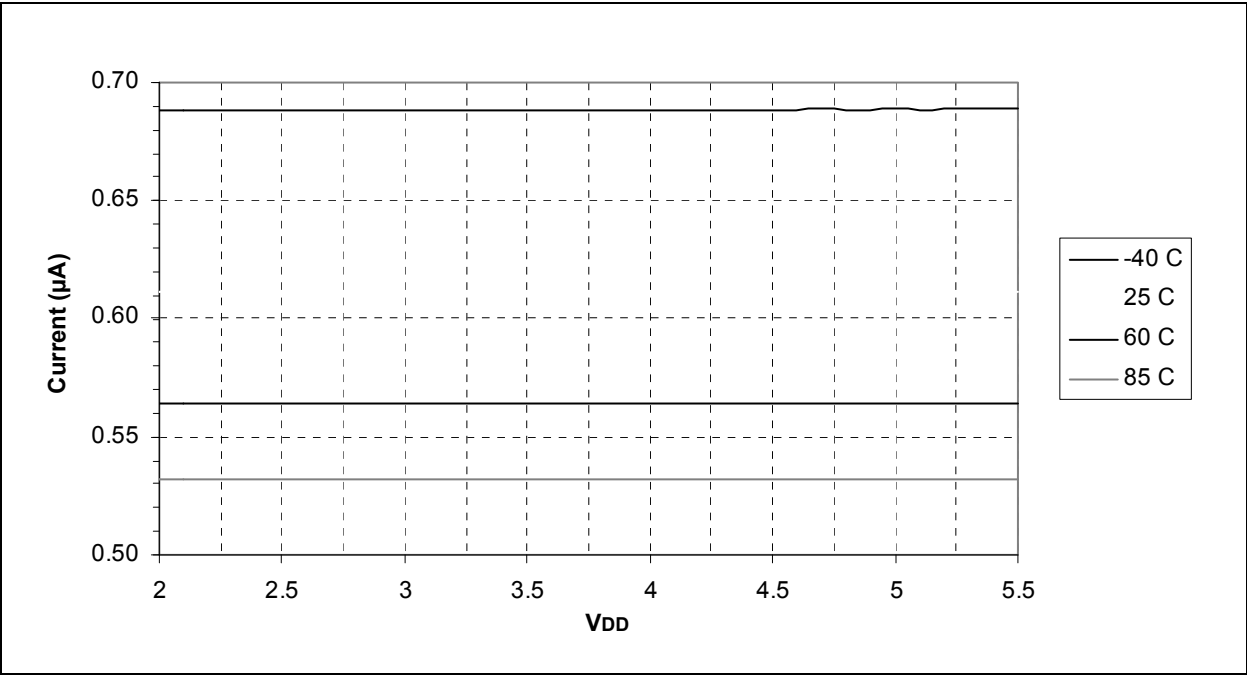**FIGURE 30-38:** CTMU OUTPUT CURRENT vs. TEMPERATURE (IRNG<1:0> = 01, 2.0V ≤ V$_{DD}$ ≤ 5.5V)

FIGURE 30-39: CTMU OUTPUT CURRENT vs. V$_{DD}$ (IRNG<1:0> = 01)

FIGURE 30-53: V_{IL}/V_{IH} vs. V_{DD} (OSCO, TEMPERATURES AS NOTED)
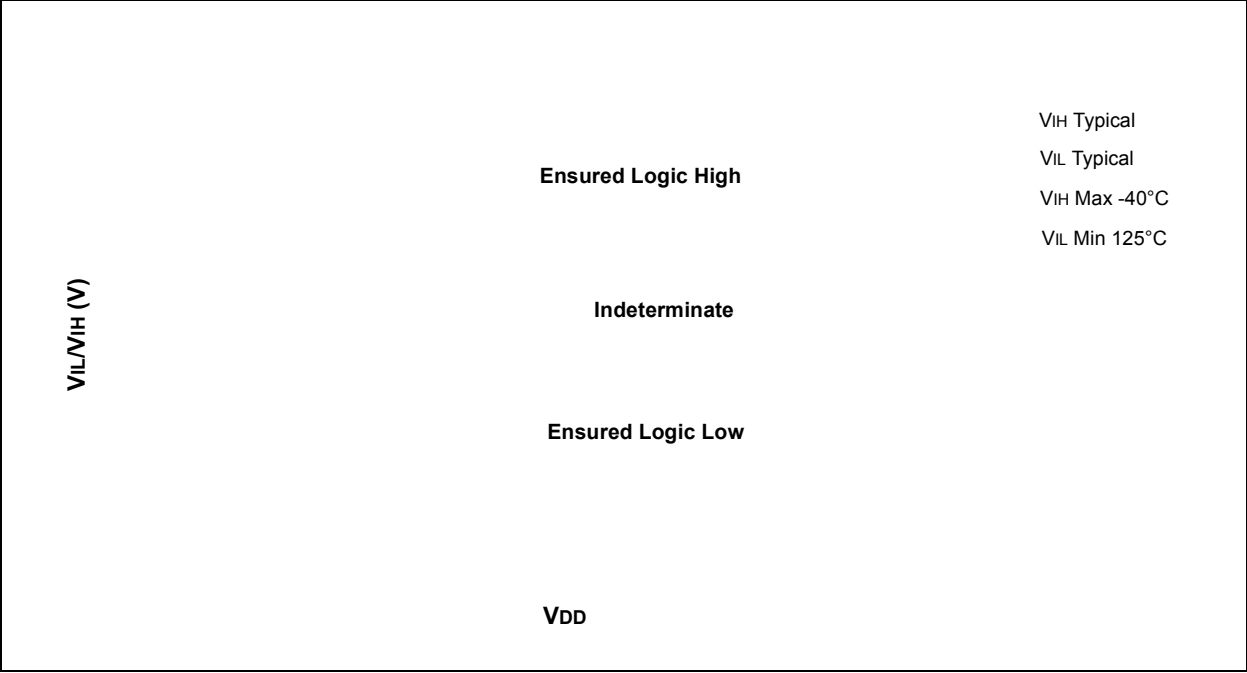
FIGURE 30-54: V_{IL}/V_{IH} vs. V_{DD} (MCLR, TEMPERATURES AS NOTED)
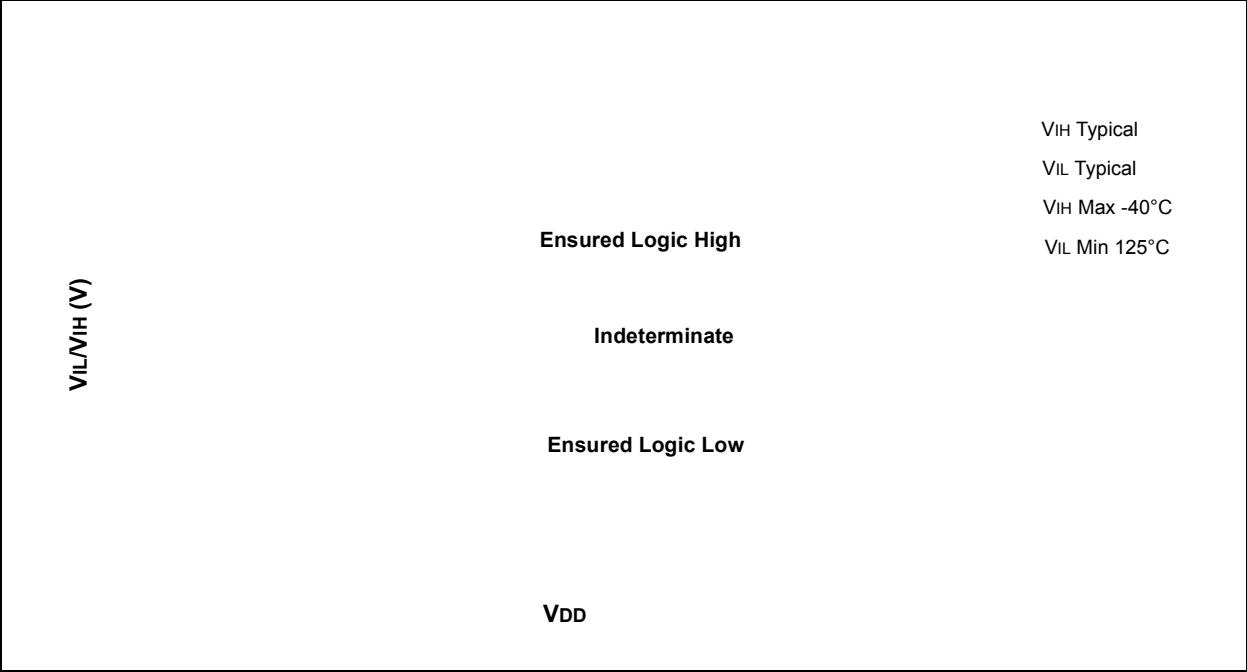
NOTES:

Revision D (March 2013)

Throughout the data sheet: corrected the name of RCON register bit 12 as RETEN, to maintain consistency with other PIC24F devices (was previously LVREN). In addition, changed the description of the bit in the RCON register (Register 7-1) to clarify its function in controlling the Retention Regulator.

Throughout the data sheet: corrected the name of FPOR Configuration register bit 2 as RETCFG, to maintain consistency with other PIC24F devices (was previously LVRCFG). In addition, changed the description of the bit in the FPOR Configuration register (Register 26-6) to clarify its function in enabling the Retention Regulator.

For **Section 10.4 "Voltage Regulator-Based Power-Saving Features"**:

- Removed all references to Fast Wake-up Sleep mode, not implemented in this device
- Changed all references of the High-Voltage Regulator to On-Chip Voltage Regulator
- Removed all references to the Low-Voltage Regulator, which was replaced in most cases with Retention Regulator
- Clarified the Retention Regulator's operation in **Section 10.4.3 "Retention Sleep Mode"** (formerly "Low-Voltage Sleep Mode")
- Modified Table 10-1 for consistency with the above changes

Corrects **Section 26.2 "On-Chip Voltage Regulator"** to clarify the operation of the on-chip regulator in "F" and "FV" families, and include DC parameters and specifications.

For **Section 29.0 "Electrical Characteristics"**:

- Updated captioning on all specification tables to include extended temperature data
- Amended Table 29-8 to include +125°C data for all existing specifications
- Added new Table 29-27 and Figure 29-8 to characterize external clock input specifications for general purpose timers (all subsequent tables and figures are renumbered accordingly)
- Added parameter numbers to several existing but previous unnumbered parameters in multiple tables

Updated **Section 30.0 "DC and AC Characteristics Graphs and Tables"**:

- Added additional graphs for Extended temperature devices (**Section 30.2 "Characteristics for Extended Temperature Devices (-40°C to +125°C)"**, Figure 30-40 through Figure 30-56)
- Replaced Figure 30-32 with an updated graph

Replaced some of the packaging diagrams in **Section 31.0 "Packaging Information"** with the newly revised diagrams.

Updates Product Information System to include extended temperature devices in the information key.

Other minor typographic corrections throughout.