# Microchip Technology - PIC24FV16KA301-E/SO Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 16KB (5.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 20-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16ka301-e-so |

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

### 1.1.4 EASY MIGRATION

Regardless of the memory size, all the devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also helps in migrating to the next larger device. This is true when moving between devices with the same pin count, or even jumping from 20-pin or 28-pin devices to 44-pin/48-pin devices.

The PIC24F family is pin compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex.

## 1.2 Other Special Features

- **Communications:** The PIC24FV32KA304 family incorporates a range of serial communication peripherals to handle a range of application requirements. There is an $I^2C$™ module that supports both the Master and Slave modes of operation. It also comprises UARTs with built-in IrDA® encoders/decoders and an SPI module.
- **Real-Time Clock/Calendar:** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and faster sampling speed. The 16-deep result buffer can be used either in Sleep to reduce power, or in Active mode to improve throughput.
- **Charge Time Measurement Unit (CTMU) Interface:** The PIC24FV32KA304 family includes the new CTMU interface module, which can be used for capacitive touch sensing, proximity sensing, and also for precision time measurement and pulse generation.

## 1.3 Details on Individual Family Members

Devices in the PIC24FV32KA304 family are available in 20-pin, 28-pin, 44-pin and 48-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are different from each other in four ways:

1. Flash program memory (16 Kbytes for PIC24FV16KA devices, 32 Kbytes for PIC24FV32KA devices).
2. Available I/O pins and ports (18 pins on two ports for 20-pin devices, 22 pins on two ports for 28-pin devices and 38 pins on three ports for 44/48-pin devices).
3. Alternate SCLx and SDAx pins are available only in 28-pin, 44-pin and 48-pin devices and not in 20-pin devices.
4. Members of the PIC24FV32KA301 family are available as both standard and high-voltage devices. High-voltage devices, designated with an “FV” in the part number (such as PIC24FV32KA304), accommodate an operating $V_{DD}$ range of 2.0V to 5.5V, and have an on-board Voltage Regulator that powers the core. Peripherals operate at $V_{DD}$. Standard devices, designated by “F” (such as PIC24F32KA304), function over a lower $V_{DD}$ range of 1.8V to 3.6V. These parts do not have an internal regulator, and both the core and peripherals operate directly from $V_{DD}$.

All other features for devices in this family are identical; these are summarized in Table 1-1.

A list of the pin features available on the PIC24FV32KA304 family devices, sorted by function, is provided in Table 1-3.

| **Note:** | Table 1-1 provides the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams on pages 3, 4, 5, 6 and 7 of the data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first. |
|---|---|

## 3.2 CPU Control Registers

**REGISTER 3-1: SR: ALU STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HSC |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | DC |
| bit 15 | | | | | | | bit 8 |

| R/W-0, HSC(1) | R/W-0, HSC(1) | R/W-0, HSC(1) | R-0, HSC | R/W-0, HSC | R/W-0, HSC | R/W-0, HSC | R/W-0, HSC |
|---|---|---|---|---|---|---|---|
| IPL2(2) | IPL1(2) | IPL0(2) | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HSC = Hardware Settable/Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **DC:** ALU Half Carry/Borrow bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th or 8th low-order bit of the result has occurred

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(1,2)
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3 **N:** ALU Negative bit
1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** ALU Overflow bit
1 = Overflow occurred for signed (2's complement) arithmetic in this arithmetic operation
0 = No overflow has occurred

bit 1 **Z:** ALU Zero bit
1 = An operation, which effects the Z bit, has set it at some time in the past
0 = The most recent operation, which effects the Z bit, has cleared it (i.e., a non-zero result)

bit 0 **C:** ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the Most Significant bit (MSb) of the result occurred
0 = No carry-out from the Most Significant bit (MSb) of the result occurred

**Note 1:** The IPLx Status bits are read-only when NSTDIS (INTCON1<15>) = 1.
**2:** The IPL<2:0> Status bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1.

### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address, as shown in Figure 4-2.

Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with data memory space addressing and makes it possible to access data in the program memory space.

### 4.1.2 HARD MEMORY VECTORS

All PIC24F devices reserve the addresses between 00000h and 000200h for hard coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user at 000000h, with the actual address for the start of code at 000002h.

PIC24F devices also have two Interrupt Vector Tables, located from 000004h to 0000FFh and 000104h to 0001FFh. These vector tables allow each of the many device interrupt sources to be handled by separate Interrupt Service Routines (ISRs). A more detailed discussion of the Interrupt Vector Tables (IVT) is provided in **Section 8.1 "Interrupt Vector Table (IVT)"**.

### 4.1.3 DATA EEPROM

In the PIC24FV32KA304 family, the data EEPROM is mapped to the top of the user program memory space, starting at address, 7FFE00, and expanding up to address, 7FFFFF.

The data EEPROM is organized as 16-bit wide memory and 256 words deep. This memory is accessed using table read and write operations similar to the user code memory.

### 4.1.4 DEVICE CONFIGURATION WORDS

Table 4-1 provides the addresses of the device Configuration Words for the PIC24FV32KA304 family. Their location in the memory map is shown in Figure 4-1.

For more information on device Configuration Words, see **Section 26.0 "Special Features"**.

**TABLE 4-1: DEVICE CONFIGURATION WORDS FOR PIC24FV32KA304 FAMILY DEVICES**

| Configuration Words | Configuration Word Addresses |
|---|---|
| FBS | F80000 |
| FGS | F80004 |
| FOSCSEL | F80006 |
| FOSC | F80008 |
| FWDT | F8000A |
| FPOR | F8000C |
| FICD | F8000E |
| FDS | F80010 |

**FIGURE 4-2: PROGRAM MEMORY ORGANIZATION**

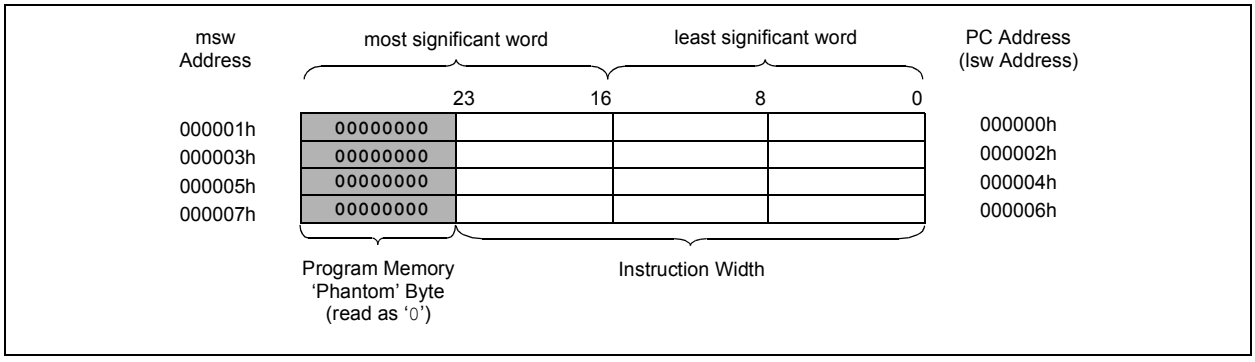


**TABLE 4-3: CPU CORE REGISTERS MAP**

| File Name | Start Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WREG0 | 0000 | WREG0 | | | | | | | | | | | | | | | | 0000 |
| WREG1 | 0002 | WREG1 | | | | | | | | | | | | | | | | 0000 |
| WREG2 | 0004 | WREG2 | | | | | | | | | | | | | | | | 0000 |
| WREG3 | 0006 | WREG3 | | | | | | | | | | | | | | | | 0000 |
| WREG4 | 0008 | WREG4 | | | | | | | | | | | | | | | | 0000 |
| WREG5 | 000A | WREG5 | | | | | | | | | | | | | | | | 0000 |
| WREG6 | 000C | WREG6 | | | | | | | | | | | | | | | | 0000 |
| WREG7 | 000E | WREG7 | | | | | | | | | | | | | | | | 0000 |
| WREG8 | 0010 | WREG8 | | | | | | | | | | | | | | | | 0000 |
| WREG9 | 0012 | WREG9 | | | | | | | | | | | | | | | | 0000 |
| WREG10 | 0014 | WREG10 | | | | | | | | | | | | | | | | 0000 |
| WREG11 | 0016 | WREG11 | | | | | | | | | | | | | | | | 0000 |
| WREG12 | 0018 | WREG12 | | | | | | | | | | | | | | | | 0000 |
| WREG13 | 001A | WREG13 | | | | | | | | | | | | | | | | 0000 |
| WREG14 | 001C | WREG14 | | | | | | | | | | | | | | | | 0000 |
| WREG15 | 001E | WREG15 | | | | | | | | | | | | | | | | 0000 |
| SPLIM | 0020 | SPLIM | | | | | | | | | | | | | | | | xxxx |
| PCL | 002E | PCL | | | | | | | | | | | | | | | | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH | | | | | | | 0000 |
| TBLPAG | 0032 | — | — | — | — | — | — | — | — | TBLPAG | | | | | | | | 0000 |
| PSVPAG | 0034 | — | — | — | — | — | — | — | — | PSVPAG | | | | | | | | 0000 |
| RCOUNT | 0036 | RCOUNT | | | | | | | | | | | | | | | | xxxxx |
| SR | 0042 | — | — | — | — | — | — | — | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | — | — | — | — | — | — | — | — | — | — | — | — | IPL3 | PSV | — | — | 0000 |
| DISICNT | 0052 | — | — | DISICNT | | | | | | | | | | | | | | xxxx |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-4: ICN REGISTER MAP**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CNPD1 | 0056 | CN15PDE(1) | CN14PDE | CN13PDE | CN12PDE | CN11PDE | CN10PDE(1,2) | CN9PDE(1) | CN8PDE(3) | CN7PDE(1) | CN6PDE | CN5PDE | CN4PDE | CN3PDE | CN2PDE | CN1PDE | CN0PDE | 0000 |
| CNPD2 | 0058 | CN31PDE(1,2) | CN30PDE | CN29PDE | CN28PDE(1,2) | CN27PDE(1) | CN26PDE(1,2) | CN25PDE(1,2) | CN24PDE(1) | CN23PDE | CN22PDE | CN21PDE | CN20PDE(1,2) | CN19PDE(1,2) | CN18PDE(1,2) | CN17PDE(1,2) | CN16PDE(1) | 0000 |
| CNPD3 | 005A | — | — | — | — | — | — | — | — | — | — | — | CN36PDE(1,2) | CN35PDE(1,2) | CN34PDE(1,2) | CN33PDE(1,2) | CN32PDE(1,2) | 0000 |
| CNEN1 | 0062 | CN15IE(1) | CN14IE | CN13IE | CN12IE | CN11IE | CN10IE(1,2) | CN9IE(1) | CN8IE(3) | CN7IE(1) | CN6IE | CN5IE | CN4IE | CN3IE | CN2IE | CN1IE | CN0IE | 0000 |
| CNEN2 | 0064 | CN31IE(1,2) | CN30IE | CN29IE | CN28IE(1,2) | CN27IE(1) | CN26IE(1,2) | CN25IE(1,2) | CN24IE(1) | CN23IE | CN22IE | CN21IE | CN20IE(1,2) | CN19IE(1,2) | CN18IE(1,2) | CN17IE(1,2) | CN16IE(1) | 0000 |
| CNEN3 | 0066 | — | — | — | — | — | — | — | — | — | — | — | CN36IE(1,2) | CN35IE(1,2) | CN34IE(1,2) | CN33IE(1,2) | CN32IE(1,2) | 0000 |
| CNPU1 | 006E | CN15PUE(1) | CN14PUE | CN13PUE | CN12PUE | CN11PUE | CN10PUE(1,2) | CN9PUE(1) | CN8PUE(3) | CN7PUE(1) | CN6PUE | CN5PUE | CN4PUE | CN3PUE | CN2PUE | CN1PUE | CN0PUE | 0000 |
| CNPU2 | 0070 | CN31PUE(1,2) | CN30PUE | CN29PUE | CN28PUE(1,2) | CN27PUE(1) | CN26PUE(1,2) | CN25PUE(1,2) | CN24PUE(1) | CN23PUE | CN22PUE | CN21PUE | CN20PUE(1,2) | CN19PUE(1,2) | CN18PUE(1,2) | CN17PUE(1,2) | CN16PUE(1) | 0000 |
| CNPU3 | 0072 | — | — | — | — | — | — | — | — | — | — | — | CN36PUE(1,2) | CN35PUE(1,2) | CN34PUE(1,2) | CN33PUE(1,2) | CN32PUE(1,2) | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These bits are not implemented in 20-pin devices.

**2:** These bits are not implemented in 28-pin devices.

**3:** These bits are not implemented in FV devices.

**REGISTER 8-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)**

bit 2 **OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

**REGISTER 8-17: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T1IP2 | T1IP1 | T1IP0 | — | OC1IP2 | OC1IP1 | OC1IP0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC1IP2 | IC1IP1 | IC1IP0 | — | INT0IP2 | INT0IP1 | INT0IP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **T1IP<2:0>:** Timer1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OC1IP<2:0>:** Output Compare Channel 1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IC1IP<2:0>:** Input Capture Channel 1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **INT0IP<2:0>:** External Interrupt 0 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

**REGISTER 8-28: IPC15: INTERRUPT PRIORITY CONTROL REGISTER 15**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | RTCIP2 | RTCIP1 | RTCIP0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **RTCIP<2:0>:** Real-Time Clock and Calendar Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 9-4: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ROEN | — | ROSSLP | ROSEL | RODIV3 | RODIV2 | RODIV1 | RODIV0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ROEN:** Reference Oscillator Output Enable bit
1 = Reference oscillator is enabled on REFO pin
0 = Reference oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Output Stop in Sleep bit
1 = Reference oscillator continues to run in Sleep
0 = Reference oscillator is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Primary oscillator is used as the base clock(1)
0 = System clock is used as the base clock; base clock reflects any clock switching of the device

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divisor Select bits
1111 = Base clock value divided by 32,768
1110 = Base clock value divided by 16,384
1101 = Base clock value divided by 8,192
1100 = Base clock value divided by 4,096
1011 = Base clock value divided by 2,048
1010 = Base clock value divided by 1,024
1001 = Base clock value divided by 512
1000 = Base clock value divided by 256
0111 = Base clock value divided by 128
0110 = Base clock value divided by 64
0101 = Base clock value divided by 32
0100 = Base clock value divided by 16
0011 = Base clock value divided by 8
0010 = Base clock value divided by 4
0001 = Base clock value divided by 2
0000 = Base clock value

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** The crystal oscillator must be enabled using the FOSC<2:0> bits; the crystal maintains the operation in Sleep mode.

## 10.3 Ultra Low-Power Wake-up

The Ultra Low-Power Wake-up (ULPWU) on pin, RB0, allows a slow falling voltage to generate an interrupt without excess current consumption.

To use this feature:

1. Charge the capacitor on RB0 by configuring the RB0 pin to an output and setting it to '1'.
2. Stop charging the capacitor by configuring RB0 as an input.
3. Discharge the capacitor by setting the ULPEN and ULPSINK bits in the ULPWCON register.
4. Configure Sleep mode.
5. Enter Sleep mode.

When the voltage on RB0 drops below VIL, the device wakes up and executes the next instruction.

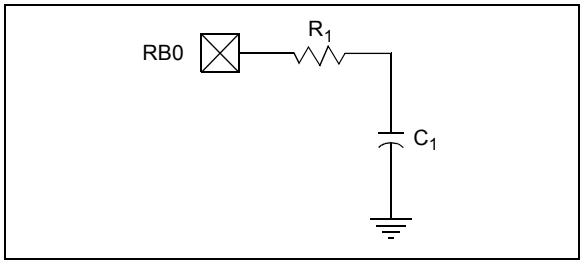
This feature provides a low-power technique for periodically waking up the device from Sleep mode.

The time-out is dependent on the discharge time of the RC circuit on RB0.

When the ULPWU module wakes the device from Sleep mode, the ULPWUIF bit (IFS5<0>) is set. Software can check this bit upon wake-up to determine the wake-up source. See Example 10-3 for initializing the ULPWU module.

A series resistor, between RB0 and the external capacitor, provides overcurrent protection for the RB0/AN0/ULPWU pin and enables software calibration of the time-out (see Figure 10-1).

**FIGURE 10-1: SERIES RESISTOR**




A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired delay in Sleep. This technique compensates for the affects of temperature, voltage and component accuracy. The peripheral can also be configured as a simple, programmable Low-Voltage Detect (LVD) or temperature sensor.

**EXAMPLE 10-3: ULTRA LOW-POWER WAKE-UP INITIALIZATION**

```
//******************************
// 1. Charge the capacitor on RB0
//******************************
    TRISBbits.TRISB0 = 0;
    LATBbits.LATB0 = 1;
    for(i = 0; i < 10000; i++) Nop();
//******************************
//2. Stop Charging the capacitor
//   on RB0
//******************************
    TRISBbits.TRISB0 = 1;
//******************************
//3. Enable ULPWU Interrupt
//******************************
IFS5bits.ULPWUIF = 0;
IEC5bits.ULPWUIE = 1;
IPC21bits.ULPWUIP = 0x7;
//******************************
//4. Enable the Ultra Low Power
//   Wakeup module and allow
//   capacitor discharge
//******************************
    ULPWCONbits.ULPEN = 1;
    ULPWCONbit.ULPSINK = 1;
//******************************
//5. Enter Sleep Mode
//******************************
    Sleep();
//for sleep, execution will
//resume here
```

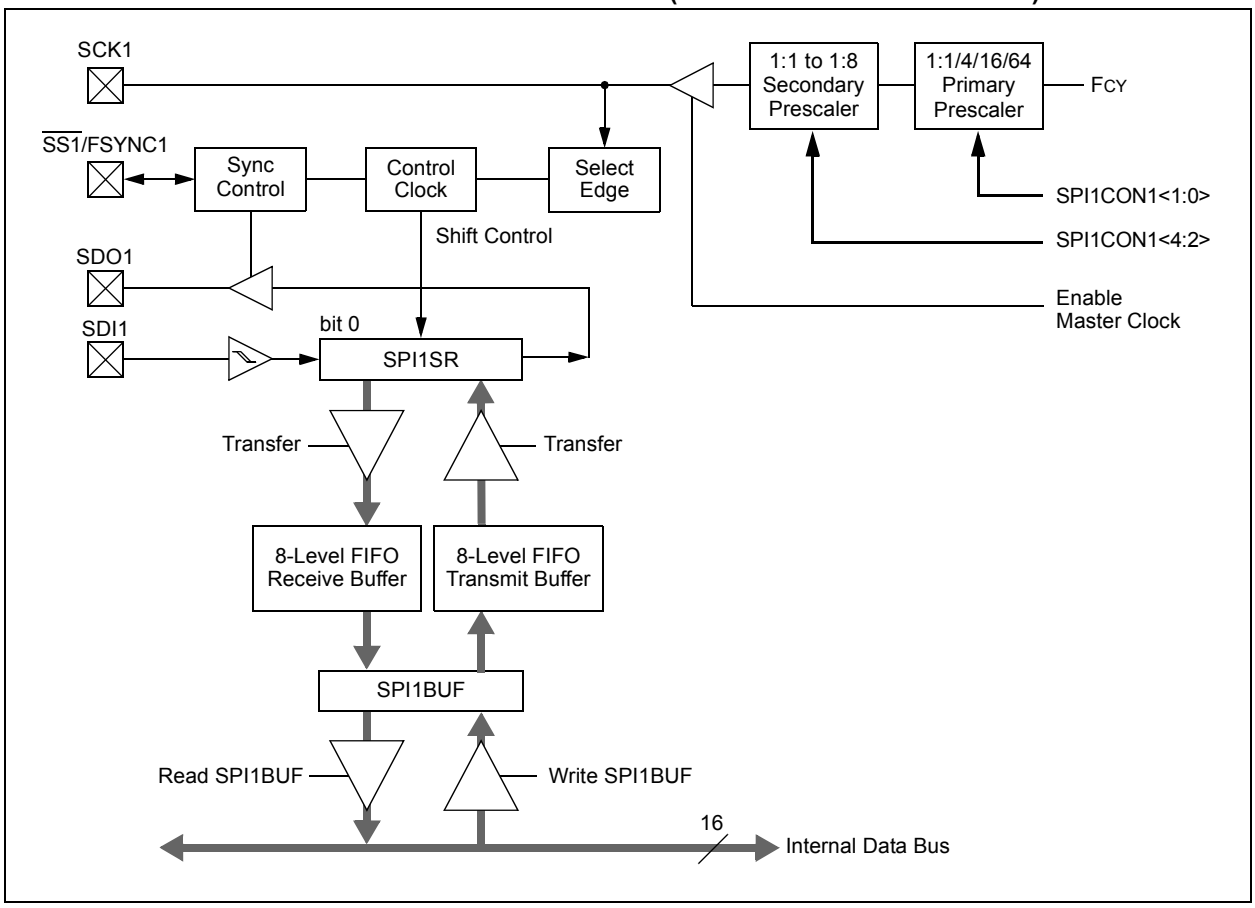
To set up the SPI1 module for the Enhanced Buffer Master (EBM) mode of operation:

1. If using interrupts:
   a) Clear the SPI1IF bit in the IFS0 register.
   b) Set the SPI1IE bit in the IEC0 register.
   c) Write the respective SPI1IPx bits in the IPC2 register.
2. Write the desired settings to the SPI1CON1 and SPI1CON2 registers with the MSTEN bit (SPI1CON1<5>) = 1.
3. Clear the SPIROV bit (SPI1STAT<6>).
4. Select Enhanced Buffer mode by setting the SPIBEN bit (SPI1CON2<0>).
5. Enable SPI operation by setting the SPIEN bit (SPI1STAT<15>).
6. Write the data to be transmitted to the SPI1BUF register. Transmission (and reception) will start as soon as data is written to the SPI1BUF register.

To set up the SPI1 module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPI1BUF register.
2. If using interrupts:
   a) Clear the SPI1IF bit in the IFS0 register.
   b) Set the SPI1IE bit in the IEC0 register.
   c) Write the respective SPI1IPx bits in the IPC2 register to set the interrupt priority.
3. Write the desired settings to the SPI1CON1 and SPI1CON2 registers with the MSTEN bit (SPI1CON1<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the $\overline{SS1}$ pin.
6. Clear the SPIROV bit (SPI1STAT<6>).
7. Select Enhanced Buffer mode by setting the SPIBEN bit (SPI1CON2<0>).
8. Enable SPI operation by setting the SPIEN bit (SPI1STAT<15>).

**FIGURE 16-2: SPI1 MODULE BLOCK DIAGRAM (ENHANCED BUFFER MODE)**



**REGISTER 16-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit has started, SPIxTXB is empty

In Standard Buffer mode:
Automatically set in hardware when the CPU writes the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

In Enhanced Buffer mode:
Automatically set in hardware when the CPU writes the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full
0 = Receive is not complete, SPIxRXB is empty

In Standard Buffer mode:
Automatically set in hardware when the SPIx transfers data from the SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

In Enhanced Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

19.2.5 RTCVAL REGISTER MAPPINGS

**REGISTER 19-4: YEAR: YEAR VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| YRTEN3 | YRTEN2 | YRTEN2 | YRTEN1 | YRONE3 | YRONE2 | YRONE1 | YRONE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to the YEAR register is only allowed when RTCWREN = 1.

**REGISTER 19-5: MTHDY: MONTH AND DAY VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | MTHTEN0 | MTHONE3 | MTHONE2 | MTHONE1 | MTHONE0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | DAYTEN1 | DAYTEN0 | DAYONE3 | DAYONE2 | DAYONE1 | DAYONE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of '0' or '1'.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.

**REGISTER 19-6: WKDYHR: WEEKDAY AND HOURS VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | WDAY2 | WDAY1 | WDAY0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | HRTEN1 | HRTEN0 | HRONE3 | HRONE2 | HRONE1 | HRONE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.

**REGISTER 19-7: MINSEC: MINUTES AND SECONDS VALUE REGISTER**

| U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | MINTEN2 | MINTEN1 | MINTEN0 | MINONE3 | MINONE2 | MINONE1 | MINONE0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | SECTEN2 | SECTEN1 | SECTEN0 | SECONE3 | SECONE2 | SECONE1 | SECONE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit bits
Contains a value from 0 to 9.

**REGISTER 25-2: CTMUCON2: CTMU CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EDG1MOD | EDG1POL | EDG1SEL3 | EDG1SEL2 | EDG1SEL1 | EDG1SEL0 | EDG2STAT | EDG1STAT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| EDG2MOD | EDG2POL | EDG2SEL3 | EDG2SEL2 | EDG2SEL1 | EDG2SEL0 | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **EDG1MOD:** Edge 1 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = Edge 1 source is Comparator 3 output
1110 = Edge 1 source is Comparator 2 output
1101 = Edge 1 source is Comparator 1 output
1100 = Edge 1 source is IC3
1011 = Edge 1 source is IC2
1010 = Edge 1 source is IC1
1001 = Edge 1 source is CTED8
1000 = Edge 1 source is CTED7
0111 = Edge 1 source is CTED6
0110 = Edge 1 source is CTED5
0101 = Edge 1 source is CTED4
0100 = Edge 1 source is CTED3**(2)**
0011 = Edge 1 source is CTED1
0010 = Edge 1 source is CTED2
0001 = Edge 1 source is OC1
0000 = Edge 1 source is Timer1

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the current source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the current source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

**Note 1:** Edge sources, CTED11 and CTED12, are not available on PIC24FV32KA302 devices.
**2:** Edge sources, CTED3, CTED11, CTED12 and CTED13, are not available on PIC24FV32KA301 devices.

## 27.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C® for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

### 27.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

**FIGURE 29-8: TIMER1/2/3/4/5 EXTERNAL CLOCK INPUT TIMING**

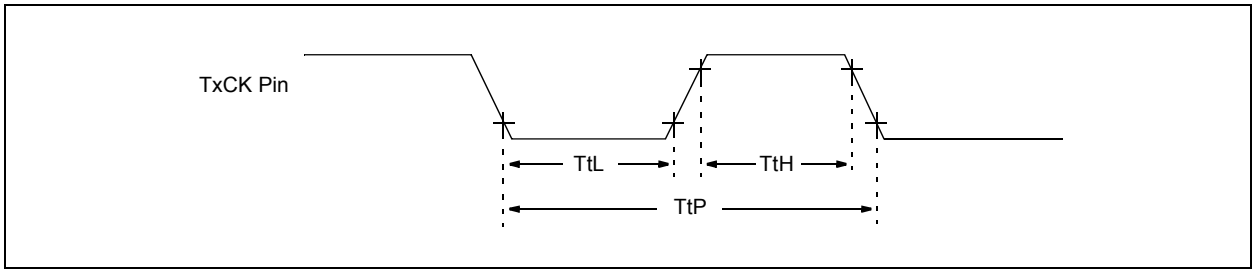



**TABLE 29-27: TIMER1/2/3/4/5 EXTERNAL CLOCK INPUT REQUIREMENTS**

| Param. No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | TtH | TxCK High Pulse Time | Sync w/Prescaler | TCY + 20 | — | ns | Must also meet Parameter Ttp |
| | | | Async w/Prescaler | 10 | — | ns | |
| | | | Async Counter | 20 | — | ns | |
| | TtL | TxCK Low Pulse Time | Sync w/Prescaler | TCY + 20 | — | ns | Must also meet Parameter Ttp |
| | | | Async w/Prescaler | 10 | — | ns | |
| | | | Async Counter | 20 | — | ns | |
| | TtP | TxCK External Input Period | Sync w/Prescaler | 2 * TCY + 40 | — | ns | N = Prescale Value (1, 4, 8, 16) |
| | | | Async w/Prescaler | Greater of: 20 or $\frac{2 * T_{CY} + 40}{N}$ | — | ns | |
| | | | Async Counter | 40 | — | ns | |
| | | Delay for Input Edge to Timer Increment | Synchronous | 1 | 2 | TCY | |
| | | | Asynchronous | — | 20 | ns | |

**FIGURE 29-9: INPUT CAPTURE x TIMINGS**

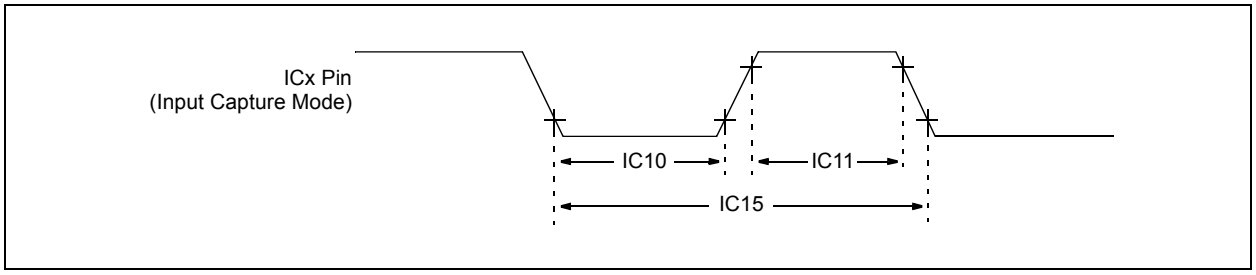



**TABLE 29-28: INPUT CAPTURE x REQUIREMENTS**

| Param. No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| IC10 | TccL | ICx Input Low Time – Synchronous Timer | No Prescaler | TCY + 20 | — | ns | Must also meet Parameter IC15 |
| | | | With Prescaler | 20 | — | ns | |
| IC11 | TccH | ICx Input Low Time – Synchronous Timer | No Prescaler | TCY + 20 | — | ns | Must also meet Parameter IC15 |
| | | | With Prescaler | 20 | — | ns | |
| IC15 | TccP | ICx Input Period – Synchronous Timer | | $\frac{2 * T_{CY} + 40}{N}$ | — | ns | N = prescale value (1, 4, 16) |

**FIGURE 30-14: TYPICAL AND MAXIMUM IPD vs. VDD**

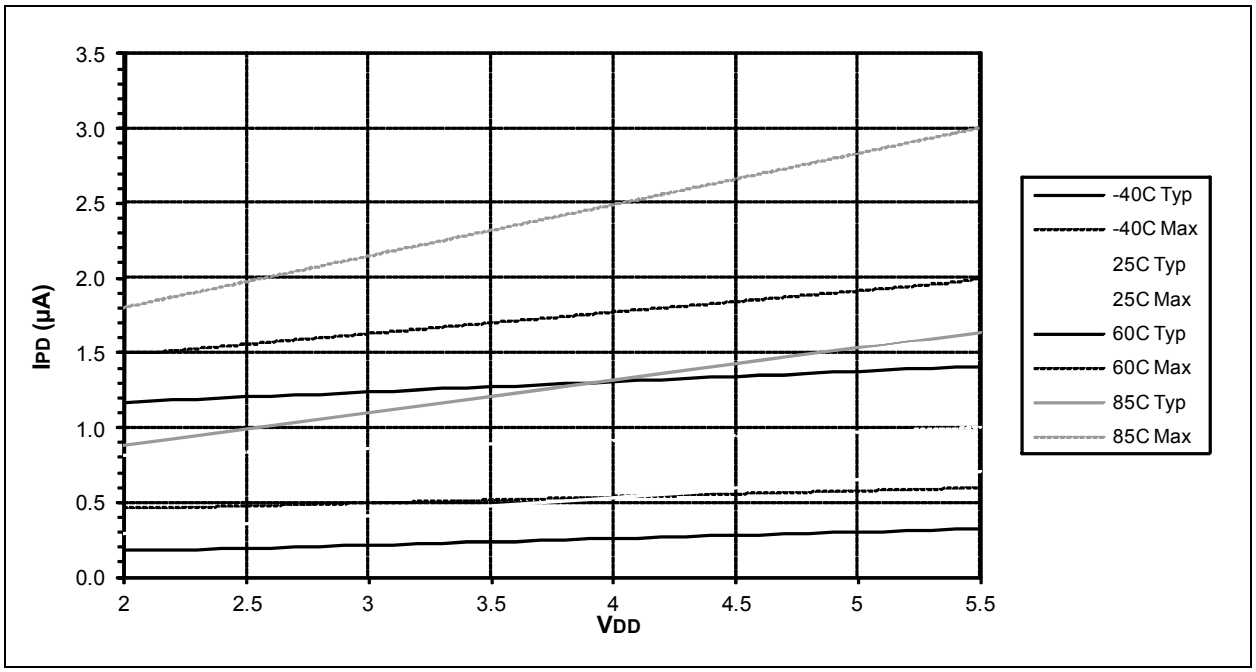



**FIGURE 30-15: TYPICAL AND MAXIMUM IPD vs. TEMPERATURE**

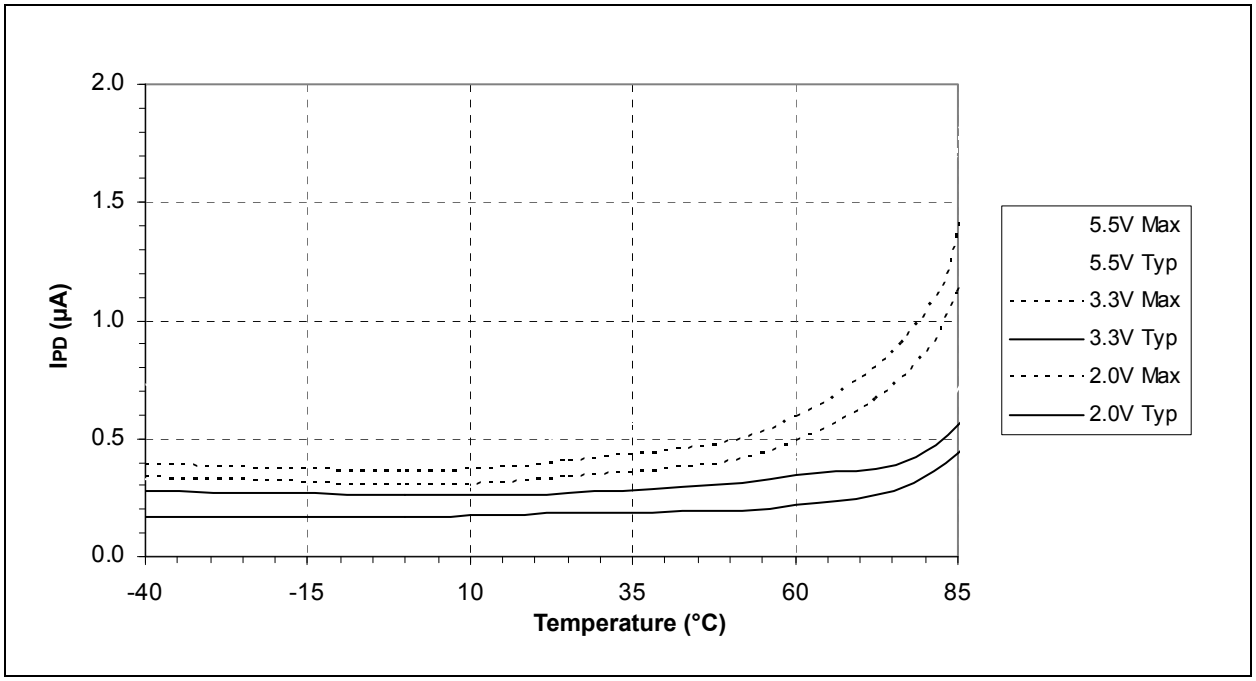


**FIGURE 30-34: TYPICAL VOLTAGE REGULATOR OUTPUT vs. VDD**

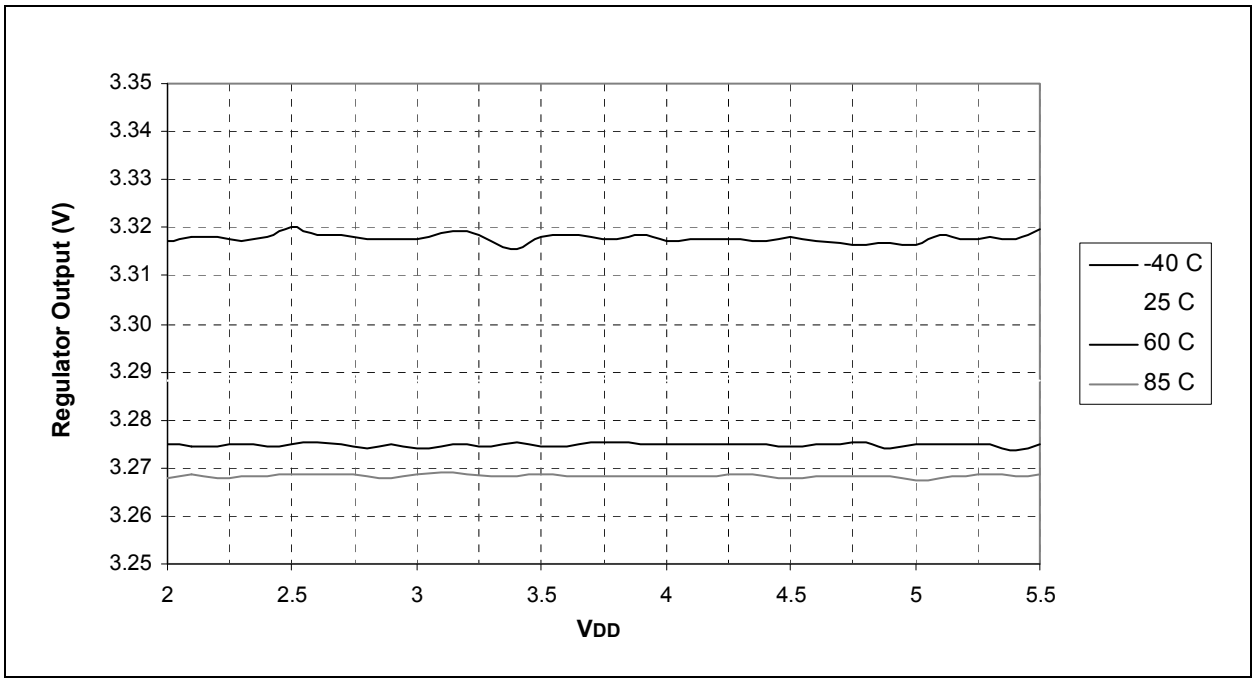
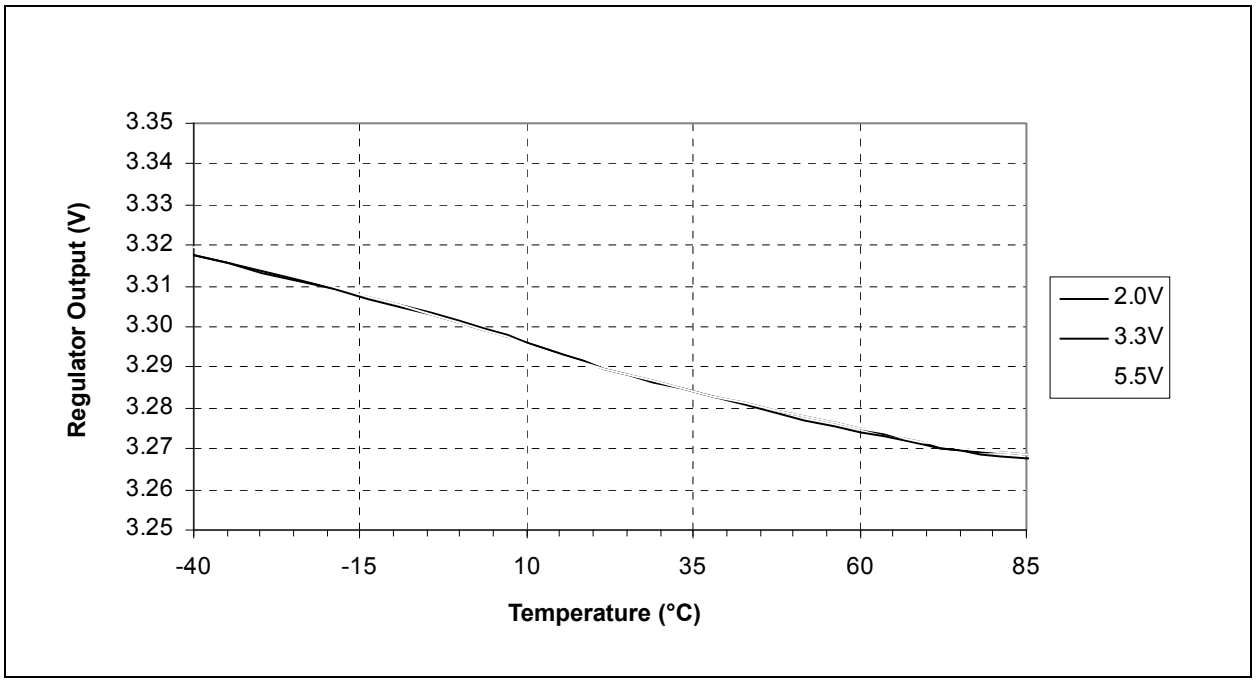



**FIGURE 30-35: TYPICAL VOLTAGE REGULATOR OUTPUT vs. TEMPERATURE**



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