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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16ka301-i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong







REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—		OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1
bit 15							bit 8

R/W-0	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2 ⁽¹⁾	OCM1 ⁽¹⁾	OCM0 ⁽¹⁾
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-14 bit 13	Unimplemented: Read as '0' OCSIDL: Output Compare x Stop in Idle Mode Control bit 1 = Output Compare x halts in CPU Idle mode 0 = Output Compare x continues to operate in CPU Idle mode
bit 12-10	OCTSEL<2:0>: Output Compare x Timer Select bits 111 = System clock 110 = Reserved 101 = Reserved 100 = Timer1 011 = Timer5 010 = Timer4 001 = Timer3 000 = Timer2
bit 9	ENFLT2: Comparator Fault Input Enable bit 1 = Comparator Fault input is enabled 0 = Comparator Fault input is disabled
bit 8	ENFLT1: OCFB Fault Input Enable bit 1 = OCFB Fault input is enabled 0 = OCFB Fault input is disabled
bit 7	ENFLT0: OCFA Fault Input Enable bit 1 = OCFA Fault input is enabled 0 = OCFA Fault input is disabled
bit 6	 OCFLT2: PWM Comparator Fault Condition Status bit 1 = PWM comparator Fault condition has occurred (this is cleared in hardware only) 0 = PWM comparator Fault condition has not occurred (this bit is used only when OCM<2:0> = 111)
bit 5	 OCFLT1: PWM OCFB Fault Input Enable bit 1 = PWM OCFB Fault condition has occurred (this is cleared in hardware only) 0 = PWM OCFB Fault condition has not occurred (this bit is used only when OCM<2:0> = 111)
bit 4	 OCFLT0: PWM OCFA Fault Condition Status bit 1 = PWM OCFA Fault condition has occurred (this is cleared in hardware only) 0 = PWM OCFA Fault condition has not occurred (this bit is used only when OCM<2:0> = 111)
bit 3	TRIGMODE: Trigger Status Mode Select bit 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software 0 = TRIGSTAT is only cleared by software

Note 1: The comparator module used for Fault input varies with the OCx module. OC1 and OC2 use Comparator 1; OC3 and OC4 use Comparator 2; OC5 uses Comparator 3.

19.2 RTCC Module Registers

The RTCC module registers are organized into three categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers

19.2.1 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding register pointers. The RTCC Value Register Window (RTCVALH and RTCVALL) uses the RTCPTR bits (RCFGCAL<9:8>) to select the desired Timer register pair (see Table 19-1).

By writing the RTCVALH byte, the RTCC Pointer value, the RTCPTR<1:0> bits decrement by one until they reach '00'. Once they reach '00', the MINUTES and SECONDS value will be accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

TABLE 19-1: RTCVAL REGISTER MAPPING

	RTCC Value Register Window				
	RTCVAL<15:8>	RTCVAL<7:0>			
00	MINUTES	SECONDS			
01	WEEKDAY	HOURS			
10	MONTH	DAY			
11	_	YEAR			

The Alarm Value Register Window (ALRMVALH and ALRMVALL) uses the ALRMPTRx bits (ALCFGRPT<9:8>) to select the desired Alarm register pair (see Table 19-2).

By writing the ALRMVALH byte, the Alarm Pointer value (ALRMPTR<1:0> bits) decrements by one until they reach '00'. Once they reach '00', the ALRMMIN and ALRMSEC value will be accessible through ALRMVALH and ALRMVALL, until the pointer value is manually changed.

EXAMPLE 19-1:	SETTING THE RTCWREN BIT

TABLE 19-2: ALRMVAL REGISTER MAPPING

ALRMPTR	Alarm Value Register Window			
<1:0>	ALRMVAL<15:8>	ALRMVAL<7:0>		
00	ALRMMIN	ALRMSEC		
01	ALRMWD	ALRMHR		
10	ALRMMNTH	ALRMDAY		
11	PWCSTAB	PWCSAMP		

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL bytes, the ALRMPTR<1:0> value will be decremented. The same applies to the RTCVALH or RTCVALL bytes with the RTCPTR<1:0> being decremented.

Note:	This only applies to read operations and
	not write operations.

19.2.2 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RTCPWC<13>) must be set (see Example 19-1).

Note: To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL<13>) is kept clear at any other time. For the RTCWREN bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN. Therefore, it is recommended that code follow the procedure in Example 19-1.

19.2.3 SELECTING RTCC CLOCK SOURCE

There are four reference source clock options that can be selected for the RTCC using the RTCCSEL<1:0> bits: 00 = Secondary Oscillator, 01 = LPRC, 10 = 50 Hz External Clock and 11 = 60 Hz External Clock.

asm	volatile	("push w7");
asm	volatile	("push w8");
asm	volatile	("disi #5");
asm	volatile	("mov #0x55, w7");
asm	volatile	("mov w7, NVMKEY");
asm	volatile	("mov #0xAA, w8");
asm	volatile	("mov w8, _NVMKEY");
asm	volatile	("bset_RCFGCAL, #13"); //set the RTCWREN bit
asm	volatile	("pop w8");
asm	volatile	("pop w7");

19.2.6 ALRMVAL REGISTER MAPPINGS

REGISTER 19-8: ALMTHDY: ALARM MONTH AND DAY VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15		•			•	•	bit 8
U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7			•	•			bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at POR '1' = Bit is		'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-13	Unimplemented: Read as '0'						
bit 12	MTHTEN0: Binary Coded Decimal Value of Month's Tens Digit bit						
	Contains a value of '0' or '1'.						
bit 11-8	MTHONE<3:0>: Binary Coded Decimal Value of Month's Ones Digit bits						
	Contains a va	lue from 0 to 9			0		
bit 7-6	Unimplemented: Read as '0'						

bit 5-4	DAYTEN<1:0>: Binary Coded Decimal Value of Day's Tens Digit bits
	Contains a value from 0 to 3.
bit 3-0	DAYONE<3:0>: Binary Coded Decimal Value of Day's Ones Digit bits

Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 19-9: ALWDHR: ALARM WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8
U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 bit 10-8	Unimplemented: Read as '0' WDAY<2:0>: Binary Coded Decimal Value of Weekday Digit bits Contains a value from 0 to 6.
bit 7-6	Unimplemented: Read as '0'
bit 5-4	HRTEN<1:0>: Binary Coded Decimal Value of Hour's Tens Digit bits Contains a value from 0 to 2.
bit 3-0	HRONE<3:0>: Binary Coded Decimal Value of Hour's Ones Digit bits Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

22.0 12-BIT A/D CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the 12-Bit A/D Converter with Threshold Detect, refer to the "PIC24F Family Reference Manual", Section 51. "12-Bit A/D Converter with Threshold Detect" (DS39739).

The PIC24F 12-bit A/D Converter has the following key features:

- Successive Approximation Register (SAR)
 Conversion
- Conversion Speeds of up to 100 ksps
- Up to 32 Analog Input Channels (Internal and External)
- Multiple Internal Reference Input Channels
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold (S/H)
 Amplifier
- Automated Threshold Scan and Compare
 Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed-Length (one word per channel), Configurable Conversion Result Buffer
- Four Options for Results Alignment
- Configurable Interrupt Generation
- Operation During CPU Sleep and Idle modes

The 12-bit A/D Converter module is an enhanced version of the 10-bit module offered in some PIC24 devices. Both modules are Successive Approximation Register (SAR) converters at their cores, surrounded by a range of hardware features for flexible configuration. This version of the module extends functionality by providing 12-bit resolution, a wider range of automatic sampling options and tighter integration with other analog modules, such as the CTMU and a configurable results buffer. This module also includes a unique Threshold Detect feature that allows the module itself to make simple decisions based on the conversion results.

A simplified block diagram for the module is illustrated in Figure 22-1.

25.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Charge Measurement Unit, refer to the "PIC24F Family Reference Manual", Section 53. "Charge Time Measurement Unit (CTMU) with Threshold Detect" (DS39743).

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides charge measurement, accurate differential time measurement between pulse sources and asynchronous pulse generation. Its key features include:

- Thirteen external edge input trigger sources
- · Polarity control for each edge source
- · Control of edge sequence
- Control of response to edge levels or edge transitions
- · Time measurement resolution of one nanosecond
- Accurate current source suitable for capacitive measurement

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock. The CTMU module is ideal for interfacing with capacitive-based touch sensors.

The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 enables the module and controls the mode of operation of the CTMU, as well as controlling edge sequencing. CTMUCON2 controls edge source selection and edge source polarity selection. The CTMUICON register selects the current range of current source and trims the current.

25.1 Measuring Capacitance

The CTMU module measures capacitance by generating an output pulse, with a width equal to the time between edge events, on two separate input channels. The pulse edge events to both input channels can be selected from several internal peripheral modules (OC1, Timer1, any input capture or comparator module) and up to 13 external pins (CTED1 through CTED13). This pulse is used with the module's precision current source to calculate capacitance according to the relationship:

EQUATION 25-1:

$$I = C \cdot \frac{dV}{dT}$$

For capacitance measurements, the A/D Converter samples an external capacitor (CAPP) on one of its input channels after the CTMU output's pulse. A Precision Resistor (RPR) provides current source calibration on a second A/D channel. After the pulse ends, the converter determines the voltage on the capacitor. The actual calculation of capacitance is performed in software by the application.

Figure 25-1 illustrates the external connections used for capacitance measurements, and how the CTMU and A/D modules are related in this application. This example also shows the edge events coming from Timer1, but other configurations using external edge sources are possible. A detailed discussion on measuring capacitance and time with the CTMU module is provided in the "*PIC24F Family Reference Manual*".

FIGURE 25-1: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR CAPACITANCE MEASUREMENT



25.2 Measuring Time

Time measurements on the pulse width can be similarly performed using the A/D module's Internal Capacitor (CAD) and a precision resistor for current calibration. Figure 25-2 displays the external connections used for time measurements, and how the CTMU and A/D modules are related in this application. This example also shows both edge events coming from the external CTEDx pins, but other configurations using internal edge sources are possible.

FIGURE 25-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT



CTMUEN — bit 15	CTMUSIDL	TGEN	EDCEN	FROOFOEN				
bit 15			EDGEN	EDGSEQEN	IDISSEN	CTTRIG		
	bit 15 b							
U-0 U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—		—	—	—	—		
bit 7						bit 0		
Legend:								
R = Readable bit	W = Writable b	it	U = Unimpler	mented bit, read	as '0'			
-n = Value at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own		
bit 15 CTMUEN: (CTMU Enable bit							
1 = Module 0 = Module	is enabled							
bit 14 Unimpleme	ented: Read as '0	2						
bit 13 CTMUSIDL	: CTMU Stop in Id	lle Mode bit						
$1 = \text{Discon}^{\dagger}$	tinues module ope	eration when o	device enters le	dle mode				
0 = Continu	ies module opera	tion in Idle mo	ode					
bit 12 TGEN: Time	e Generation Enal	ble bit						
1 = Enable	s edge delay gene	eration						
0 = Disable	is eage delay gen	eration						
1 = Edges	are not blocked							
0 = Edges	are blocked							
bit 10 EDGSEQEI	N: Edge Sequence	e Enable bit						
1 = Edge 1	event must occur	before Edge	2 event can o	ccur				
0 = No edg	0 = No edge sequence is needed							
bit 9 IDISSEN: A	IDISSEN: Analog Current Source Control bit							
1 = Analog 0 = Analog	current source ou	itput is ground itput is not are	ded ounded					
bit 8 CTTRIG: C	TMU Trigger Cont	rol bit						
1 = Trigger	output is enabled							
0 = Triager	output is disabled	1						
÷ 11990								

REGISTER 25-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	
bit 15		•			•		bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	_							
bit 7 bit (
Legend:								
R = Readable	bit	W = Writable I	oit	U = Unimplem	nented bit, read	1 as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown		
bit 15-10 ITRIM<5:0>: Current Source Trim bits 011111 = Maximum positive change from nominal current 011110 000001 = Minimum positive change from nominal current 000000 = Nominal current output specified by IRNG<1:0> 111111 = Minimum negative change from nominal current 100010 100001 = Maximum negative change from nominal current								
bit 9-8	11 = 100 × Base Current 10 = 10 × Base Current 01 = Base Current Level (0.55 μA nominal) 00 = 1000 × Base Current Unimplemented: Read as '0'							

REGISTER 25-3: CTMUICON: CTMU CURRENT CONTROL REGISTER

REGISTER 26-10: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	—	_	—		—	—
bit 23							bit 16
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		—		—		—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R	R	R	R
_		—		REV3	REV2	REV1	REV0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			oit	U = Unimplemented bit, read as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			iown

bit 23-4 Unimplemented: Read as '0'

bit 3-0 **REV<3:0>:** Minor Revision Identifier bits

27.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

27.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

27.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

27.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

27.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command line interface
- · Rich directive set
- · Flexible macro language
- · MPLAB IDE compatibility

DC CHARACTE						
Parameter No.	Device	Typical	Typical Max Units Conditions			Conditions
IDD Current						
D20	PIC24FV32KA3XX	269	450	μA	2.0V	
		465	830	μA	5.0V	0.5 MIPS,
	PIC24F32KA3XX	200	330	μA	1.8V	Fosc = 1 MHz ⁽¹⁾
		410	750	μA	3.3V	
DC22	PIC24FV32KA3XX	490	—	μA	2.0V	
		880	—	μA	5.0V	1 MIPS,
	PIC24F32KA3XX	407	—	μA	1.8V	Fosc = 2 MHz ⁽¹⁾
		800	—	μA	3.3V	
DC24	PIC24FV32KA3XX	13.0	20.0	mA	5.0V	16 MIPS,
	PIC24F32KA3XX	12.0	18.0	mA	3.3V	Fosc = 32 MHz ⁽¹⁾
DC26	PIC24FV32KA3XX	2.0	—	mA	2.0V	
		3.5	—	mA	5.0V	FRC (4 MIPS),
	PIC24F32KA3XX	1.80	—	mA	1.8V	Fosc = 8 MHz
		3.40	—	mA	3.3V	
DC30	PIC24FV32KA3XX	48.0	250	μA	2.0V	
		75.0	450	μA	5.0V	LPRC (15.5 KIPS),
	PIC24F32KA3XX	8.1	28	μA	1.8V	Fosc = 31 kHz
		13.50	150	μA	3.3V	

TABLE 29-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

Legend: Unshaded rows represent PIC24F32KA3XX devices and shaded rows represent PIC24FV32KA3XX devices.

Note 1: Oscillator is in External Clock mode (FOSCSEL<2:0> = 010, FOSC<1:0> = 00).





TABLE 29-32: I²C[™] BUS DATA TIMING REQUIREMENTS (MASTER MODE)

АС СНА		STICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C < TA < +85°C for Industrial					
				$-40^{\circ}C \le TA \le +00^{\circ}C$ for Extended					
Param No.	Symbol	Charac	teristic	Min ⁽¹⁾	Мах	Units	Conditions		
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 1)	_	μs			
			400 kHz mode	Tcy/2 (BRG + 1)	_	μS			
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	_	μS			
IM11	THI:SCL	Clock High Time	100 kHz mode	Tcy/2 (BRG + 1)		μS			
			400 kHz mode	Tcy/2 (BRG + 1)	_	μS			
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	_	μS			
IM20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be		
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF		
			1 MHz mode ⁽²⁾	—	100	ns			
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be		
			400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF		
			1 MHz mode ⁽²⁾	—	300	ns			
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250		ns			
			400 kHz mode	100	_	ns			
			1 MHz mode ⁽²⁾	100	_	ns			
IM26	THD:DAT	Data Input	100 kHz mode	0	_	ns			
		Hold Time	400 kHz mode	0	0.9	μS			
			1 MHz mode ⁽²⁾	0	_	ns			
IM40	TAA:SCL	Output Valid	100 kHz mode	—	3500	ns			
		from Clock	400 kHz mode	—	1000	ns			
			1 MHz mode ⁽²⁾	—		ns			
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7		μS	Time the bus must be		
			400 kHz mode	1.3		μS	free before a new		
			1 MHz mode ⁽²⁾	0.5		μs	transmission can start		
IM50	Св	Bus Capacitive L	oading	—	400	pF			

Note 1: BRG is the value of the I²C Baud Rate Generator. Refer to **Section 17.3 "Setting Baud Rate When Operating as a Bus Master**" for details.

2: Maximum pin capacitance = 10 pF for all I²C pins (for 1 MHz mode only).

FIGURE 30-30: VIL/VIH vs. VDD (OSCO, TEMPERATURES AS NOTED)



FIGURE 30-31: VIL/VIH vs. VDD (MCLR, TEMPERATURES AS NOTED)



28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	INCHES			
Dimension	n Limits	MIN	NOM	MAX
Number of Pins	Ν		28	
Pitch	е		.100 BSC	
Top to Seating Plane	Α	-	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	Е	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

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