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Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16ka302-i-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 4-21: CRC REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	_	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0	CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	_	—	0000
CRCCON2	0642	—	—	—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0		—	_	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0	0000
CRCXORL	0644	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	—	0000
CRCXORH	0646	X31	X30	X29	X28	X27	X26	X25	X24	X23	X22	X21	X20	X19	X18	X17	X16	0000
CRCDATL	0648								CRCDA	TL								XXXX
CRCDATH	064A		CRCDATH										XXXX					
CRCWDATL	064C		CRCWDATL xxx:										XXXX					
CRCWDATH	064E	CRCWDATH										XXXX						

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: CLOCK CONTROL REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	SBOREN	RETEN	—	DPSLP	СМ	PMSLP	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	(Note 1)
OSCCON	0742	_	COSC2	COSC1	COSC0	_	NOSC2	NOSC1	NOSC0	CLKLOCK	_	LOCK	_	CF	SOSCDRV	SOSCEN	OSWEN	(Note 2)
CLKDIV	0744	ROI	DOZE2	DOZE1	DOZE0	DOZEN	RCDIV2	RCDIV1	RCDIV0	_	_	_	_	_	_	_	_	3140
OSCTUN	0748	_	_	_	_	_	_	_	_	_	_	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000
REFOCON	074E	ROEN	_	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	_	_	_	_	_	_	_	_	0000
HLVDCON	0756	HLVDEN	_	HLSIDL	_		_	_	_	VDIR	BGVST	IRVST	_	HLVDL3	HLVDL2	HLVDL1	HLVDL0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: RCON register Reset values are dependent on the type of Reset.

2: OSCCON register Reset values are dependent on the Configuration Fuses and by type of Reset.

TABLE 4-23: DEEP SLEEP REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DSCON	0758	DSEN		—	_	_	—	_	RTCCWDIS		—	—			ULPWDIS	DSBOR	RELEASE	0000
DSWAKE	075A	_	_	_	_	_	_	_	DSINT0	DSFLT	_	_	DSWDT	DSRTCC	DSMCLR	_	DSPOR	0000
DSGPR0 ⁽¹⁾	075C									DSGPR0								0000
DSGPR1 ⁽¹⁾	075E		DSGPR1 000										0000					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The Deep Sleep registers, DSGPR0 and DSGPR1, are only reset on a VDD POR event.

7.0 RESETS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Resets, refer to the "PIC24F Family Reference Manual", Section 40. "Reset with Programmable Brown-out Reset" (DS39728).

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Pin Reset
- SWR: RESET Instruction
- WDTR: Watchdog Timer Reset
- · BOR: Brown-out Reset
- Low-Power BOR/Deep Sleep BOR
- TRAPR: Trap Conflict Reset
- · IOPUWR: Illegal Opcode Reset
- UWR: Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 7-1.

Any active source of Reset will make the SYSRST signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on Power-on Reset (POR) and unchanged by all other Resets.

Note: Refer to the specific peripheral or Section 3.0 "CPU" of this data sheet for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). A Power-on Reset will clear all bits except for the BOR and POR bits (RCON<1:0>) which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer (WDT) and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

FIGURE 7-1: RESET SYSTEM BLOCK DIAGRAM



INE OID I EIN	0-4.						
R/W-0	R-0, HSC	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	_			_		_
bit 15	·				•	•	bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	—	—	—		INT2EP	INT1EP	INT0EP
bit 7	·	•				•	bit 0
Legend:		HSC = Hardw	are Settable/C	learable bit			
R = Readabl	le bit	W = Writable I	oit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15	ALTIVT: Enat	ole Alternate Int	errupt Vector 7	Table bit			
	1 = Uses Alte	rnate Interrupt '	Vector Table (A	AIVT)			
	0 = Uses stan	idard (default) I	nterrupt Vector	r Table (IVT)			
bit 14	DISI: DISI In	struction Status	s bit				
	1 = DISI inst	ruction is active) 				
	0 = DISI INSt	ruction is not ad	Ctive				
bit 13-3	Unimplemen	ted: Read as ')^				
bit 2	INT2EP: Exte	rnal Interrupt 2	Edge Detect F	Polarity Select b	bit		
	1 = Interrupt i	s on the negatives on the positive	ve edge				
bit 1		s on the positiv	E euge Edge Detect [Palarity Salaat k	sit		
DILI	1 = Interrunt i	s on the negative			JIL		
	0 = Interrupt i	s on the positiv	e edge				
bit 0	INT0EP: Exte	rnal Interrupt 0	Edge Detect F	Polarity Select b	oit		
	1 = Interrupt i	s on the negativ	ve edge				
	0 = Interrupt i	s on the positiv	e edge				

REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER2

REGISTER 8-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	U-0
U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	—	OC3IF	_
bit 15							bit 8
U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0	R/W-0
—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF
bit 7							bit 0
Legend:		HS = Hardwar	e Settable hit]
R = Readable	bit	W = Writable I	nit	U = Unimplem	nented bit read	1 as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15	U2TXIF: UAR	T2 Transmitter	Interrupt Flag	Status bit			
	1 = Interrupt n	equest has occ	urred				
	0 = Interrupt r	equest has not	occurred				
bit 14	U2RXIF: UAR	RT2 Receiver In	terrupt Flag St	atus bit			
	1 = Interrupt n	equest has occ	occurred				
bit 13	INT2IF: Extern	nal Interrupt 2 P	Flag Status bit				
	1 = Interrupt r	equest has occ	urred				
	0 = Interrupt r	equest has not	occurred				
bit 12	T5IF: Timer5	Interrupt Flag S	Status bit				
	1 = Interrupt r	equest has occ	urred				
	0 = Interrupt r	equest has not	occurred				
bit 11	T4IF: Timer4	Interrupt Flag S	Status bit				
	1 = Interrupt n	equest has occ	surred				
bit 10		equest has not	occurred				
bit 9		it Compare Ch) annel 3 Interru	nt Elan Status k	sit		
bit 9	1 = Interrupt r	equest has occ	urred	pri lag Status r	Л		
	0 = Interrupt r	equest has not	occurred				
bit 8-5	Unimplement	ted: Read as '0)'				
bit 4	INT1IF: Exter	nal Interrupt 1 I	-lag Status bit				
	1 = Interrupt r	equest has occ	urred				
	0 = Interrupt r	equest has not	occurred				
bit 3	CNIF: Input C	hange Notificat	tion Interrupt F	lag Status bit			
	1 = Interrupt n	equest has occ	curred				
hit 2	CMIE: Compa	equest has not arator Interrunt	Elan Status hit				
Dit 2	1 = Interrupt n	equest has occ	urred				
	0 = Interrupt r	equest has not	occurred				
bit 1	MI2C1IF: Mas	ster I2C1 Event	Interrupt Flag	Status bit			
	1 = Interrupt r	equest has occ	urred				
1	0 = Interrupt r	equest has not	occurred				
Dit U	SI2C1IF: Slav	e I2C1 Event li	nterrupt Flag S	itatus bit			
	1 = interrupt r 0 = Interrupt r	equest has occ equest has not	occurred				

REGISTER	8-17: IPC0	: INTERRUPT		ONTROL R	EGISTER 0		
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	T1IP2	T1IP1	T1IP0	_	OC1IP2	OC1IP1	OC1IP0
bit 15		·	·		·	·	bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	IC1IP2	IC1IP1	IC1IP0	_	INT0IP2	INT0IP1	INT0IP0
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
							-
bit 15	Unimpleme	nted: Read as '	0'				
bit 14-12	T1IP<2:0>:	Timer1 Interrupt	Priority bits				
	111 = Interro	upt is Priority 7 (highest priority	interrupt)			
	•			• •			
	•						
		upt is Priority 1	ablad				
bit 11		ntod: Read as '	ableu				
		Cutout Compo	u vro Channol 1 li	otorrunt Driori	ity bite		
DIL 10-0	111 = Intern	unt is Priority 7 (highest priority	interrunt)	ity Dits		
	•		nightest phoney	interrupt)			
	• 001 = Interru	upt is Priority 1					
	000 = Interre	upt source is dis	abled				
bit 7	Unimpleme	nted: Read as '	0'				
bit 6-4	IC1IP<2:0>:	Input Capture C	Channel 1 Interr	upt Priority bi	its		
	111 = Interru	upt is Priority 7 (highest priority	interrupt)			
	•						
	• 001 - Intorn	unt is Priority 1					
	000 = Interr	upt is i nonty i upt source is dis	abled				
bit 3	Unimpleme	nted: Read as '	0'				
bit 2-0	INT0IP<2:0>	External Interr	upt 0 Priority bi	its			
	111 = Interro	upt is Priority 7 (highest priority	interrupt)			
	•						
	•						
		upt is Priority 1	abled				
		upt 300100 13 018	adicu				



FIGURE 15-1: OUTPUT COMPARE x BLOCK DIAGRAM (16-BIT MODE)

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—		OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1
bit 15							bit 8

R/W-0	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2 ⁽¹⁾	OCM1 ⁽¹⁾	OCM0 ⁽¹⁾
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 15-14 bit 13	Unimplemented: Read as '0' OCSIDL: Output Compare x Stop in Idle Mode Control bit 1 = Output Compare x halts in CPU Idle mode 0 = Output Compare x continues to operate in CPU Idle mode
bit 12-10	OCTSEL<2:0>: Output Compare x Timer Select bits 111 = System clock 110 = Reserved 101 = Reserved 100 = Timer1 011 = Timer5 010 = Timer4 001 = Timer3 000 = Timer2
bit 9	ENFLT2: Comparator Fault Input Enable bit 1 = Comparator Fault input is enabled 0 = Comparator Fault input is disabled
bit 8	ENFLT1: OCFB Fault Input Enable bit 1 = OCFB Fault input is enabled 0 = OCFB Fault input is disabled
bit 7	ENFLT0: OCFA Fault Input Enable bit 1 = OCFA Fault input is enabled 0 = OCFA Fault input is disabled
bit 6	 OCFLT2: PWM Comparator Fault Condition Status bit 1 = PWM comparator Fault condition has occurred (this is cleared in hardware only) 0 = PWM comparator Fault condition has not occurred (this bit is used only when OCM<2:0> = 111)
bit 5	 OCFLT1: PWM OCFB Fault Input Enable bit 1 = PWM OCFB Fault condition has occurred (this is cleared in hardware only) 0 = PWM OCFB Fault condition has not occurred (this bit is used only when OCM<2:0> = 111)
bit 4	 OCFLT0: PWM OCFA Fault Condition Status bit 1 = PWM OCFA Fault condition has occurred (this is cleared in hardware only) 0 = PWM OCFA Fault condition has not occurred (this bit is used only when OCM<2:0> = 111)
bit 3	TRIGMODE: Trigger Status Mode Select bit 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software 0 = TRIGSTAT is only cleared by software

Note 1: The comparator module used for Fault input varies with the OCx module. OC1 and OC2 use Comparator 1; OC3 and OC4 use Comparator 2; OC5 uses Comparator 3.

19.2.5 RTCVAL REGISTER MAPPINGS

REGISTER 19-4: YEAR: YEAR VALUE REGISTER⁽¹⁾

| U-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-x |
| YRTEN3 | YRTEN2 | YRTEN2 | YRTEN1 | YRONE3 | YRONE2 | YRONE1 | YRONE0 |
| bit 7 | | | | | | | bit 0 |

Legend:

Ecgenia.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

- bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits Contains a value from 0 to 9.
- bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 19-5: MTHDY: MONTH AND DAY VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15						•	bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12	MTHTEN0: Binary Coded Decimal Value of Month's Tens Digit bit Contains a value of '0' or '1'.
bit 11-8	MTHONE<3:0>: Binary Coded Decimal Value of Month's Ones Digit bits
	Contains a value from 0 to 9.
bit 7-6	Unimplemented: Read as '0'
bit 5-4	DAYTEN<1:0>: Binary Coded Decimal Value of Day's Tens Digit bits
	Contains a value from 0 to 3.
bit 3-0	DAYONE<3:0>: Binary Coded Decimal Value of Day's Ones Digit bits
	Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

NOTES:

Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
GOTO	GOTO	Expr	Go to Address	2	2	None
	GOTO	Wn	Go to Indirect	1	2	None
INC	INC	f	f = f + 1	1	1	C, DC, N, OV, Z
	INC	f,WREG	WREG = f + 1	1	1	C, DC, N, OV, Z
	INC	Ws,Wd	Wd = Ws + 1	1	1	C, DC, N, OV, Z
INC2	INC2	f	f = f + 2	1	1	C, DC, N, OV, Z
	INC2	f,WREG	WREG = f + 2	1	1	C, DC, N, OV, Z
	INC2	Ws,Wd	Wd = Ws + 2	1	1	C, DC, N, OV, Z
IOR	IOR	f	f = f .IOR. WREG	1	1	N, Z
	IOR	f,WREG	WREG = f .IOR. WREG	1	1	N, Z
	IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N, Z
	IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N, Z
	IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N, Z
LNK	LNK	#lit14	Link Frame Pointer	1	1	None
LSR	LSR	f	f = Logical Right Shift f	1	1	C, N, OV, Z
	LSR	f,WREG	WREG = Logical Right Shift f	1	1	C, N, OV, Z
	LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C, N, OV, Z
	LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N, Z
	LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N, Z
MOV	MOV	f,Wn	Move f to Wn	1	1	None
	MOV	[Wns+Slit10],Wnd	Move [Wns+Slit10] to Wnd	1	1	None
	MOV	f	Move f to f	1	1	N, Z
	MOV	f,WREG	Move f to WREG	1	1	N, Z
	MOV	#lit16,Wn	Move 16-bit Literal to Wn	1	1	None
	MOV.b	#lit8,Wn	Move 8-bit Literal to Wn	1	1	None
	MOV	Wn,f	Move Wn to f	1	1	None
	MOV	Wns,[Wns+Slit10]	Move Wns to [Wns+Slit10]	1	1	None
	MOV	Wso,Wdo	Move Ws to Wd	1	1	None
	MOV	WREG, f	Move WREG to f	1	1	N, Z
	MOV.D	Wns,Wd	Move Double from W(ns):W(ns+1) to Wd	1	2	None
	MOV.D	Ws,Wnd	Move Double from Ws to W(nd+1):W(nd)	1	2	None
MUL	MUL.SS	Wb,Ws,Wnd	{Wnd+1, Wnd} = Signed(Wb) * Signed(Ws)	1	1	None
	MUL.SU	Wb,Ws,Wnd	{Wnd+1, Wnd} = Signed(Wb) * Unsigned(Ws)	1	1	None
	MUL.US	Wb,Ws,Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Signed(Ws)	1	1	None
	MUL.UU	Wb,Ws,Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Unsigned(Ws)	1	1	None
	MUL.SU	Wb,#lit5,Wnd	{Wnd+1, Wnd} = Signed(Wb) * Unsigned(lit5)	1	1	None
	MUL.UU	Wb,#lit5,Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Unsigned(lit5)	1	1	None
	MUL	f	W3:W2 = f * WREG	1	1	None
NEG	NEG	f	$f = \overline{f} + 1$	1	1	C, DC, N, OV, Z
	NEG	f,WREG	WREG = [+ 1	1	1	C, DC, N, OV, Z
	NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1	C, DC, N, OV, Z
NOP	NOP		No Operation	1	1	None
	NOPR		No Operation	1	1	None
POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
	POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
	POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd+1)	1	2	None
	POP.S		Pop Shadow Registers	1	1	All
PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
	PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
	PUSH.D	Wns	Push W(ns):W(ns+1) to Top-of-Stack (TOS)	1	2	None
	PUSH.S		Push Shadow Registers	1	1	None

TARI E 28-2.	INSTRUCTION SET OVERVIEW (CONTINUED
TADLL 20-2.		

Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	2	None
TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
ULNK	ULNK		Unlink Frame Pointer	1	1	None
XOR	XOR	f	f = f .XOR. WREG	1	1	N, Z
	XOR	f,WREG	WREG = f .XOR. WREG	1	1	N, Z
	XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N, Z
	XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N, Z
	XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N, Z
ZE	ZE	Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C, Z, N

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC24FV32KA304 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FV32KA304 family devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings^(†)

Ambient temperature under bias	40°C to +135°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss (PIC24FVXXKA30X)	0.3V to +6.5V
Voltage on VDD with respect to Vss (PIC24FXXKA30X)	0.3V to +4.5V
Voltage on any combined analog and digital pin with respect to Vss	0.3V to (VDD + 0.3V)
Voltage on any digital only pin with respect to Vss	0.3V to (VDD + 0.3V)
Voltage on MCLR/VPP pin with respect to Vss	-0.3V to +9.0V
Maximum current out of Vss pin	
Maximum current into VDD pin ⁽¹⁾	250 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports ⁽¹⁾	200 mA

Note 1: Maximum allowable current is a function of the device maximum power dissipation (see Table 29-1).

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 29-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $PI/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(Tj — Ta)/θja			W

TABLE 29-2: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур	Мах	Unit	Notes
Package Thermal Resistance, 20-Pin SPDIP	θJA	62.4		°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θJA	60	-	°C/W	1
Package Thermal Resistance, 20-Pin SSOP	θJA	108	_	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θJA	71		°C/W	1
Package Thermal Resistance, 20-Pin SOIC	θJA	75	_	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θJA	80.2	_	°C/W	1
Package Thermal Resistance, 28-Pin QFN	θJA	32	_	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θJA	29	_	°C/W	1
Package Thermal Resistance, 48-Pin UQFN	θJA		_	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

TABLE 29-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DC10	Vdd	Supply Voltage	1.8	_	3.6	V	For F devices
			2.0		5.5	V	For FV devices
DC12	Vdr	RAM Data Retention	1.5		—	V	For F devices
		Voltage ⁽²⁾	1.7		—	V	For FV devices
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	Vss	—	0.7	V	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	_		V/ms	0-3.3V in 0.1s 0-2.5V in 60 ms

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which VDD can be lowered without losing RAM data.



			Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX						
AC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Max Units Conditions			
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC mode)	DC 4	_	32 8	MHz MHz	EC ECPLL		
OS15		Oscillator Frequency	0.2 4 4 31		4 25 8 33	MHz MHz MHz kHz	XT HS XTPLL SOSC		
OS20	Tosc	Tosc = 1/Fosc	—	—	_	-	See Parameter OS10 for Fosc value		
OS25	TCY	Instruction Cycle Time ⁽²⁾	62.5	—	DC	ns			
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x Tosc	—	_	ns	EC		
OS31	TosR, TosF	External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC		
OS40	TckR	CLKO Rise Time ⁽³⁾	—	6	10	ns			
OS41	TckF	CLKO Fall Time ⁽³⁾		6	10	ns			

TABLE 29-19: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Min." values with an external clock applied to the OSCI/CLKI pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 TCY) and high for the Q3-Q4 period (1/2 TCY).



FIGURE 29-19: SPIX MODULE MASTER MODE TIMING CHARACTERISTICS (CKE = 1)

TABLE 29-37: SPIX MODULE MASTER MODE TIMING REQUIREMENTS (CKE = 1)

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
SP10	TscL	SCKx Output Low Time ⁽²⁾	TCY/2	_		ns		
SP11	TscH	SCKx Output High Time ⁽²⁾	TCY/2	_	_	ns		
SP20	TscF	SCKx Output Fall Time ⁽³⁾	_	10	25	ns		
SP21	TscR	SCKx Output Rise Time ⁽³⁾	-	10	25	ns		
SP30	TdoF	SDOx Data Output Fall Time ⁽³⁾	_	10	25	ns		
SP31	TdoR	SDOx Data Output Rise Time ⁽³⁾	_	10	25	ns		
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge		—	30	ns		
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	_	_	ns		

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns; therefore, the clock generated in Master mode must not violate this specification.

3: This assumes a 50 pF load on all SPIx pins.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	INCHES				
Dimension Limits		MIN	NOM	MAX	
Number of Pins	Ν	28			
Pitch e .100			.100 BSC		
Top to Seating Plane	Α	-	-	.200	
Molded Package Thickness	A2	.120	.135	.150	
Base to Seating Plane	A1	.015	-	-	
Shoulder to Shoulder Width	E	.290	.310	.335	
Molded Package Width	E1	.240	.285	.295	
Overall Length	D	1.345	1.365	1.400	
Tip to Seating Plane	L	.110	.130	.150	
Lead Thickness	С	.008	.010	.015	
Upper Lead Width	b1	.040	.050	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eB	-	-	.430	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimensio	n Limits	MIN	NOM	MAX	
Number of Pins	Ν	20			
Pitch	е	0.65 BSC			
Overall Height	А	-	-	2.00	
Molded Package Thickness	A2	1.65	1.75	1.85	
Standoff	A1	0.05	-	-	
Overall Width	Е	7.40	7.80	8.20	
Molded Package Width	E1	5.00	5.30	5.60	
Overall Length	D	6.90	7.20	7.50	
Foot Length	L	0.55	0.75	0.95	
Footprint	L1	1.25 REF			
Lead Thickness	с	0.09	-	0.25	
Foot Angle	φ	0°	4°	8°	
Lead Width	b	0.22	_	0.38	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
 Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Number of Pins		28			
Pitch	е	0.65 BSC			
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.20 REF			
Overall Width	E	6.00 BSC			
Exposed Pad Width	E2	3.65	3.70	4.20	
Overall Length	D	6.00 BSC			
Exposed Pad Length	D2	3.65	3.70	4.20	
Terminal Width	b	0.23	0.30	0.35	
Terminal Length	L	0.50	0.55	0.70	
Terminal-to-Exposed Pad	K	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105C Sheet 2 of 2

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension Limits		MIN	NOM	MAX	
Contact Pitch E		0.65 BSC			
Optional Center Pad Width	W2			4.25	
Optional Center Pad Length	T2			4.25	
Contact Pad Spacing	C1		5.70		
Contact Pad Spacing	C2		5.70		
Contact Pad Width (X28)	X1			0.37	
Contact Pad Length (X28)	Y1			1.00	
Distance Between Pads		0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

Revision D (March 2013)

Throughout the data sheet: corrected the name of RCON register bit 12 as RETEN, to maintain consistency with other PIC24F devices (was previously LVREN). In addition, changed the description of the bit in the RCON register (Register 7-1) to clarify its function in controlling the Retention Regulator.

Throughout the data sheet: corrected the name of FPOR Configuration register bit 2 as RETCFG, to maintain consistency with other PIC24F devices (was previously LVRCFG). In addition, changed the description of the bit in the FPOR Configuration register (Register 26-6) to clarify its function in enabling the Retention Regulator.

For Section 10.4 "Voltage Regulator-Based Power-Saving Features":

- Removed all references to Fast Wake-up Sleep mode, not implemented in this device
- Changed all references of the High-Voltage Regulator to On-Chip Voltage Regulator
- Removed all references to the Low-Voltage Regulator, which was replaced in most cases with Retention Regulator
- Clarified the Retention Regulator's operation in Section 10.4.3 "Retention Sleep Mode" (formerly "Low-Voltage Sleep Mode")
- Modified Table 10-1 for consistency with the above changes

Corrects Section 26.2 "On-Chip Voltage Regulator" to clarify the operation of the on-chip regulator in "F" and "FV" families, and include DC parameters and specifications.

For Section 29.0 "Electrical Characteristics":

- Updated captioning on all specification tables to include extended temperature data
- Amended Table 29-8 to include +125°C data for all existing specifications
- Added new Table 29-27 and Figure 29-8 to characterize external clock input specifications for general purpose timers (all subsequent tables and figures are renumbered accordingly)
- Added parameter numbers to several existing but previous unnumbered parameters in multiple tables

Updated Section 30.0 "DC and AC Characteristics Graphs and Tables":

- Added additional graphs for Extended temperature devices (Section 30.2 "Characteristics for Extended Temperature Devices (-40°C to +125°C)", Figure 30-40 through Figure 30-56)
- Replaced Figure 30-32 with an updated graph

Replaced some of the packaging diagrams in **Section 31.0** "**Packaging Information**" with the newly revised diagrams.

Updates Product Information System to include extended temperature devices in the information key.

Other minor typographic corrections throughout.