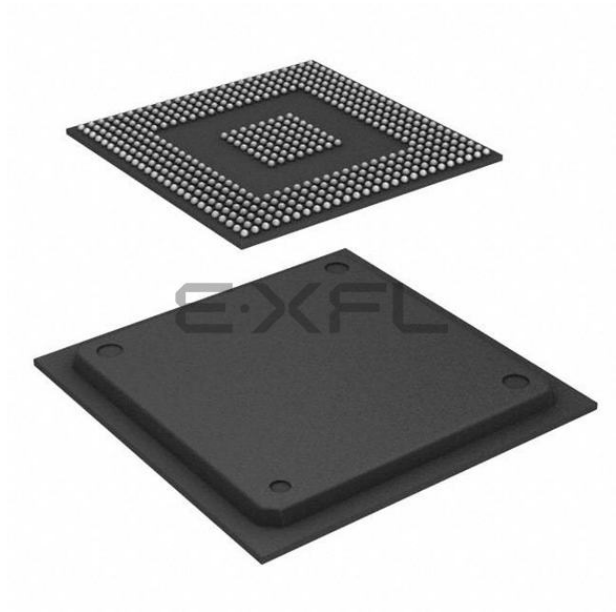

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Details	
Product Status	Active
Applications	Graphics Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	Jade
RAM Size	64K x 8
Interface	ADC, ATA, CAN, EBI/EMI, I²C, I²S, Media LB, PWM, SD Card, UART/USART, USB
Number of I/O	24
Voltage - Supply	1.1V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	484-BGA
Supplier Device Package	484-BGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/fujitsu/mb86r01pb-gse1

Revision History

Date	Ver.	Contents
2007/07/12	1.0	Newly issued
2007/08/20	1.1	8.3.1. Recommended Power On/Off Sequence • Revised the last line of description (PLL reference clock part) 8.4.3. ADC • Revised value of table 8-16 • Revised and deleted descriptive content of note • Revised footnote (*2) of table 8-17 8.4.4. I^2C Bus Fast Mode I/O • Revised table 8-18 and footnote • Deleted footnote (*3) 8.5.9. I^2C Bus Timing • Revised footnote (*2) of table 8-37 8.5.12. MLB Signal Timing • Revised MLB to MediaLB • Revised footnote of table 8-42, 8-45
2007/11/09	1.2	4. Function list • Revised contents of the list 6. Pin assignment • Revised figures in 1-8/1-9 pages • Added "top view" statement 7.1. Pin Multiplex • Revised description of note • Added mode setting description to pin multiplex group #1 ~ #5 • Revised table of pin multiplex group #2 and #4 7.2.4. USB 2.0 Host/Function related pin • Revised description of USB_EXT12K pin 7.2.5. External interrupt controller related pin • Revised title 7.2.12. A/D converter related pin • Revised pin name: AD_AVD0 → AD_AVD, AD_AVS1 → AD_AVS 7.2.24. Unused pin • Added this section 7.2.25. Unused pin with pin multiplex function in the duplex case • Added this section 8.4.2. DDR2SDRAM IF I/O (SSTL_18) • Revised table 8-12 8.5.1. Memory Controller Signal Timing • Revised table 8-21 • Revised figure 8-8 and 8-9 • Added figure 8-10, 8-11, and 8-12 8.5.6.2. Input Signal • Revised figure 8-23
2008/02/07	1.3	6. Pin assignment • Revised figure and table 7.2.2. IDE66 related pin • Revised type • Revised status pin after reset 7.2.3. SD memory controller related pin • Unified SD_DAT[0] and SD_DAT[3:1] 7.2.7. CAN related pin • Revised type

Date	Ver.	Contents
2008/02/07	1.3	7.2.8. I2S related pin • Revised type • Revised status pin after reset 7.2.10. SPI related pin • Revised type 7.2.11. PWM related pin • Revised type • Added comment 7.2.13. DDR2 related pin • Revised resistance value of *2 7.2.15. Video captured related pin • Revised type • Added comment 7.2.18. ICE related pin • Revised status pin after reset of XSRST 7.2.20. ETM related pin • Revised pin name in description column of TRACECLK 7.2.22. MediaLB related pin • Revised pin name • Revised type 7.2.24. Unused pin • Revised process • Deleted BIGEND • Revised pin name of B17, B16, C17, C16, and D16 7.2.25. Unused pin with pin multiplex function in the duplex case • Revised process 8.1. Maximum Ratings • Revised table 8-1
2009/07/07	1.4	7.2.14. DISPLAY related pin • Added note 8.1. Maximum Ratings • Revised table 8-1 8.3.2. Power On Reset • Revised figure 8-3 • Revised description 8.5.5.1. Clock • Revised table 8-28 8.5.7. I2S Signal Timing • Revised table 8-34 and 8-35 8.5.10. SPI Signal Timing • Revised table 8-38

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AHB1 bus

Following resources are connected.

- CPU core: Bus masters of instruction (I)/data (D)
- GDC: GDC register part
- AHB2AXI: AXI port for main memory access
- CCPB: Encrypted ROM decoding block
- External BUS I/F: External bus interface (connected through CCPB)
- SRAM: General purpose internal SRAM 32KB × 2
- DMAC: General purpose DMA × 8ch
  It operates as bus master at data transfer
- Boot ROM: Built-in boot ROM
- I2S_0/1/2: Serial audio controller × 3ch
- USB 2.0 Function DMAC: USB function DMAC
  It operates as bus master at data transfer
- USB2.0 Host: It operates as USB2.0 EHCI, USB1.1 OHCI bus masters
- IDE66/IDE66DMAC: Register part of IDE host controller and built-in DMAC
  The DMAC part operates as bus master at data transfer
- MLB: MediaLB controller
- AHB2
- APBBRG0/1/2: AHB-APB bridge circuit × 3ch

AHB2 bus

- CCPB: Encrypted ROM decoding block
- USB 2.0 Function: USB 2.0 function controller's register part
- USB 2.0 Host: USB 2.0 host controller's register part
- SDMC: SD memory controller
- DDR2 controller: DDR2 controller's register part

APB_TOP_0

This block bridges between APBBRG0 bus and AHB1 bus, and following low-speed peripheral resources are connected.

- Interrupt controller (IRC) × 2ch
- External interrupt controller (EXTIRC)
- Clock reset generator (CRG)
- UART (ch0 and ch1) × 2ch
- Remap boot controller (RBC)
- 32 bit general-purpose timer (32 bit timer) × 2ch

APB_TOP_1

This block bridges between APBBRG1 bus and AHB1 bus, and following low-speed peripheral resources are connected.

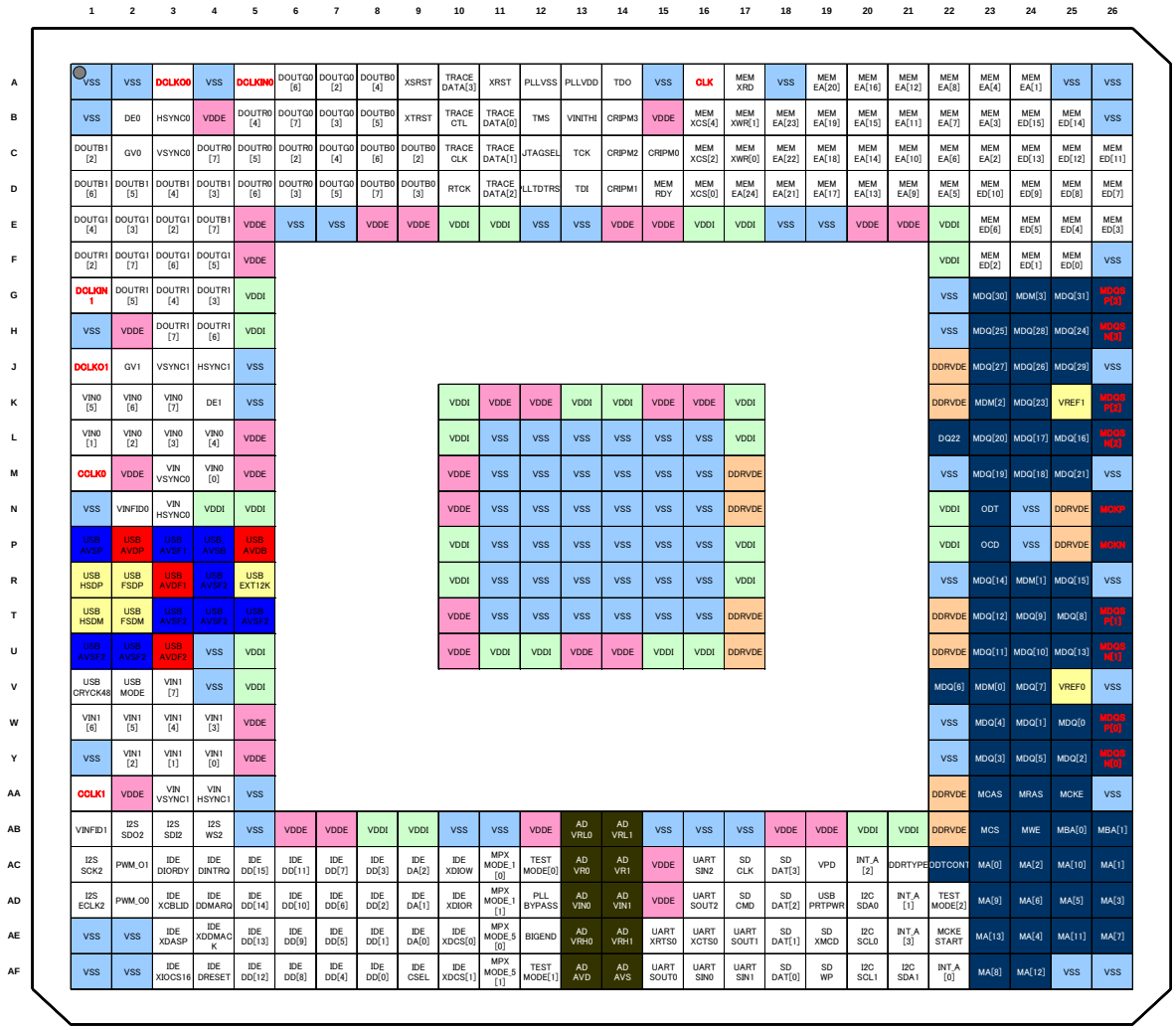
- I^2C controller × 2ch
- CAN controller × 2ch
- UART (ch2 and ch3) × 2ch
- A/D converter (ADC) × 2ch

APB_TOP_2

This block bridges between APBBRG2 bus and AHB1 bus, and following low-speed peripheral resources are connected.

- PWM controller (PWM)
- SPI controller (SPI)
- CCNT
- UART (ch4 and ch5) × 2ch

(Top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VSS	VSS	DCLKO0	VSS	DCLKIN0	DOUTG0 [6]	DOUTG0 [2]	DOUTB0 [4]	XSRST	TRACE DATA[3]	XRST	PLLVSS	PLLVDD	TDO	VSS	CLK	MEM XRD	VSS	MEM EA[20]	MEM EA[16]	MEM EA[12]	MEM EA[8]	MEM EA[4]	MEM EA[1]	VSS	VSS
B	VSS	DE0	HSYNC0	VDDE	DOUTR0 [4]	DOUTG0 [7]	DOUTG0 [3]	DOUTB0 [5]	XTRST	TRACE CTL	TRACE DATA[0]	TMS	VINITHI	CRIPM3	VDDE	MEM XCS[4]	MEM XWR[1]	MEM EA[23]	MEM EA[19]	MEM EA[15]	MEM EA[11]	MEM EA[7]	MEM EA[3]	MEM ED[15]	MEM ED[14]	VSS
C	DOUTB1 [2]	GV0	VSYNC0	DOUTR0 [7]	DOUTR0 [5]	DOUTR0 [2]	DOUTG0 [4]	DOUTB0 [6]	DOUTB0 [2]	TRACE CLK	TRACE DATA[1]	JTAGSEL	TCK	CRIPM2	CRIPM0	MEM XCS[2]	MEM XWR[0]	MEM EA[22]	MEM EA[18]	MEM EA[14]	MEM EA[10]	MEM EA[6]	MEM EA[2]	MEM ED[13]	MEM ED[12]	MEM ED[11]
D	DOUTB1 [6]	DOUTB1 [5]	DOUTB1 [4]	DOUTB1 [3]	DOUTR0 [6]	DOUTR0 [3]	DOUTG0 [5]	DOUTB0 [7]	DOUTB0 [3]	RTCK	TRACE DATA[2]	TLLTDTRS	TDI	CRIPM1	MEM RDY	MEM XCS[0]	MEM EA[24]	MEM EA[21]	MEM EA[17]	MEM EA[13]	MEM EA[9]	MEM EA[5]	MEM ED[10]	MEM ED[9]	MEM ED[8]	MEM ED[7]
E	DOUTG1 [4]	DOUTG1 [3]	DOUTG1 [2]	DOUTB1 [7]	VDDE	VSS	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	VDDE	VDDI	MEM ED[6]	MEM ED[5]	MEM ED[4]	MEM ED[3]
F	DOUTR1 [2]	DOUTG1 [7]	DOUTG1 [6]	DOUTG1 [5]	VDDE																	VDDI	MEM ED[2]	MEM ED[1]	MEM ED[0]	VSS
G	DCLKIN 1	DOUTR1 [5]	DOUTR1 [4]	DOUTR1 [3]	VDDI																	VSS	MDQ[30]	MDM[3]	MDQ[31]	MDQS P[3]
H	VSS	VDDE	DOUTR1 [7]	DOUTR1 [6]	VDDI																	VSS	MDQ[25]	MDQ[28]	MDQ[24]	MDQS N[3]
J	DCLKO1	GV1	VSYNC1	HSYNC1	VSS																	DDRVDE	MDQ[27]	MDQ[26]	MDQ[29]	VSS
K	VIN0 [5]	VIN0 [6]	VIN0 [7]	DE1	VSS					VDDI	VDDE	VDDE	VDDI	VDDI	VDDE	VDDE	VDDI					DDRVDE	MDM[2]	MDQ[23]	VREF1	MDQS P[2]
L	VIN0 [1]	VIN0 [2]	VIN0 [3]	VIN0 [4]	VDDE					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					DQ22	MDQ[20]	MDQ[17]	MDQ[16]	MDQS N[2]
M	CCLK0	VDDE	VIN VSYNC0	VIN0 [0]	VDDE					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					VSS	MDQ[19]	MDQ[18]	MDQ[21]	VSS
N	VSS	VINFID0	VIN HSYNC0	VDDI	VDDI					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					VDDI	ODT	VSS	DDRVDE	MCKP
P	USB AVSP	USB AVDP	USB AVSF1	USB AVSF	USB AVDF					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					VDDI	OCD	VSS	DDRVDE	MCKN
R	USB HSDP	USB FSDP	USB AVDF1	USB AVSF2	USB EXT12K					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					VSS	MDQ[14]	MDM[1]	MDQ[15]	VSS
T	USB HSDM	USB FSDM	USB AVSF2	USB AVSF2	USB AVSF2					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					DDRVDE	MDQ[12]	MDQ[9]	MDQ[8]	MDQS P[1]
U	USB AVSF2	USB AVSF2	USB AVDF2	VSS	VDDI					VDDE	VDDI	VDDI	VDDE	VDDE	VDDI	VDDI	DDRVDE					DDRVDE	MDQ[11]	MDQ[10]	MDQ[13]	MDQS N[1]
V	USB CRYCK48	USB MODE	VIN1 [7]	VSS	VDDI																	MDQ[6]	MDM[0]	MDQ[7]	VREF0	VSS
W	VIN1 [6]	VIN1 [5]	VIN1 [4]	VIN1 [3]	VDDE																	VSS	MDQ[4]	MDQ[1]	MDQ[0	MDQS P[0]
Y	VSS	VIN1 [2]	VIN1 [1]	VIN1 [0]	VDDE																	VSS	MDQ[3]	MDQ[5]	MDQ[2]	MDQS N[0]
AA	CCLK1	VDDE	VIN VSYNC1	VIN HSYNC1	VSS																	DDRVDE	MCAS	MRAS	MCKE	VSS
AB	VINFID1	I2S SDO2	I2S SDI2	I2S WS2	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	AD VRL0	AD VRL1	VSS	VSS	VSS	VDDE	VDDE	VDDI	VDDI	DDRVDE	MCS	MWE	MBA[0]	MBA[1]
AC	I2S SCK2	PWM_O1	IDE DIORDY	IDE DINTRQ	IDE DD[15]	IDE DD[11]	IDE DD[7]	IDE DD[3]	IDE DA[2]	IDE XDIOW	MPX MODE_1 [0]	TEST MODE[0]	AD VR0	AD VR1	VDDE	UART SIN2	SD CLK	SD DAT[3]	VPD	INT_A [2]	DDRTYPE	ODTCONT	MA[0]	MA[2]	MA[10]	MA[1]
AD	I2S ECLK2	PWM_O0	IDE XCBLID	IDE DDMARQ	IDE DD[14]	IDE DD[10]	IDE DD[6]	IDE DD[2]	IDE DA[1]	IDE XDIOR	MPX MODE_1 [1]	PLL BYPASS	AD VIN0	AD VIN1	VDDE	UART SOUT2	SD CMD	SD DAT[2]	USB PRTPWR	I2C SDA0	INT_A [1]	TEST MODE[2]	MA[9]	MA[6]	MA[5]	MA[3]
AE	VSS	VSS	IDE XDASP	IDE XDDMACK	IDE DD[13]	IDE DD[9]	IDE DD[5]	IDE DD[1]	IDE DA[0]	IDE XDCS[0]	MPX MODE_5 [0]	BIGEND	AD VRH0	AD VRH1	UART XRTS0	UART XCTS0	UART SOUT1	SD DAT[1]	SD XMCD	I2C SCL0	INT_A [3]	MCKE START	MA[13]	MA[4]	MA[11]	MA[7]
AF	VSS	VSS	IDE XIOCS16	IDE DRESET	IDE DD[12]	IDE DD[8]	IDE DD[4]	IDE DD[0]	IDE CSEL	IDE XDCS[1]	MPX MODE_5 [1]	TEST MODE[1]	AD AVD	AD AVS	UART SOUT0	UART SIN0	UART SIN1	SD DAT[0]	SD WP	I2C SCL1	I2C SDA1	INT_A [0]	MA[8]	MA[12]	VSS	VSS

7. Pin function

External pin function of MB86R01 is described below.

7.1. Pin Multiplex

This LSI adopts pin multiplex function, and a part of external pin function is multiplexed.
The external pin function is categorized into following five groups. Each group is able to set the external pin function individually; therefore, the function can be flexibly set depending on the peripheral I/O resource to be used.

1. Pin multiplex group #1 (setting pin: MPX_MODE_1[1:0])
   - Mode 0: Pin related to DISPLAY1
   - Mode 1: Pin related to external bus interface
   - Mode 2: Pin related to I2S0, GPIO, and DISPLAY0 data width extension
2. Pin multiplex group #2 (setting register: CMUX_MD.MPX_MODE_2[2:0])
   - Mode 0: Pin related to CAP1, CAP0 synchronizing signal, PWM, and I2S2
   - Mode 1: Pin related to CAP1 (NRGB666)
   - Mode 2: Pin related to GPIO, CAN, I2S1, MediaLB, and I2S2
   - Mode 3: Pin related to GPIO, CAN, I2S1, MediaLB, and SPI
   - Mode 4: Pin related to GPIO, CAN, I2S1, MediaLB, and I2S2 (input)
3. Pin multiplex group #3 (setting pin: USB_MODE)
   - Mode 0: Pin related to USB 2.0 host
   - Mode 1: Pin related to USB 2.0 function
4. Pin multiplex group #4 (setting register: CMUX_MD.MPX_MODE_4[1:0])
   - Mode 0: Pin related to IDE
   - Mode 1: Pin related to I2S1, CAN, GPIO, and PWM
5. Pin multiplex group #5 (setting pin: MPX_MODE_5[1:0])
   - Mode 0: Pin related to ETM
   - Mode 1: Pin related to UART3, UART4, and UART5
   - Mode 2: Pin related to UART3, UART4, and PWM

Note:
Mode should be changed when each pin is not in operation.
PWM, I2S1, and CAN pins may be duplicated and allocated to external pin depending on group combination; in this case, use either of them. For unused pin, follow the procedure in 1.6.27, unused pin with pin multiplex function in the duplex case.

7.2. Pin Function

Format

Pin function list is shown in the following format.

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description

Meaning of item and sign

Pin name

Name of external pin.

I/O

Input/Output signal's distinction based on this LSI.

- I: Pin that can be used as input
- O: Pin that can be used as output
- IO: Pin that can be used as input and output (interactive pin)

Polarity

Active polarity of external pin's input/output signals

- P: "H" active pin (positive logic)
- N: "L" active pin (negative logic)
- PN: "H" and "L" active pins

Analog/Digital

Signal type of external pin

- A: Analog signal
- D: Digital signal

Type

Input/Output circuit type of external pin.

- CLK:
- POD: Pseudo Open Drain
- PU: Pull Up
- PD: Pull Down
- ST: Schmitt Type
- Tri: Tri-state

Pin status after reset

Pin status after external pin reset

- H: "H" level
- L: "L" level
- HiZ: High impedance
- X: "H" level or "L" level
- A: Clock output

Description

Outline of external pin function

7.2.13. DDR2 related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
MA[13:0]	O	P	D	-	H	Address
MBA[1:0]	O	P	D	-	H	Bank address
MDQ[31:0]	IO	P	D	-	H	Data (*5)
MDM[3:0]	O	P	D	-	HiZ	Data mask (*6)
MDQSP[3:0]	IO	P	D	-	HiZ	Data strobe (*5)
MDQSN[3:0]	IO	N	D	-	HiZ	Data strobe (*5)
MCKP	O	P	D	CLK	L	Clock output
MCKN	O	N	D	CLK	H	Clock output
MCKE	O	P	D	-	L	Clock enable
MCS	O	N	D	-	L	Chip select
MRAS	O	N	D	-	H	Row address strobe
MCAS	O	N	D	-	H	Column address strobe
MWE	O	N	D	-	H	Write enable
DDRVDE	I	-	A	-	-	SSTL_18 1.8V power supply
VREF1	I	-	A	-	-	Reference voltage input (DDRVDE/2)
VREF0	I	-	A	-	-	Reference voltage input (DDRVDE/2)
OCD	O	-	A	-	-	Off chip driver reference voltage input (*1)
ODT	O	-	A	-	-	On-die termination reference voltage input (*2)
ODTCONT	O	P	D	-	L	On-die termination control (*3)
MCKE_START	I	P	D	-	-	Set a state of MCKE in reset 0: Low (*4) 1: High (reserved)
DDRTYPE	I	P	D	-	-	Pull-up pin to VDDE via high resistance

*1: Pull up the pin to DDRVDE (1.8V power supply), via 200Ω resistance
*2: PCB impedance Z = 100Ω or 50Ω: Pull up pin to DDRVDE (1.8V power supply), via a 180Ω resistance.
PCB impedance Z = 150Ω or 75Ω: Pull up pin to DDRVDE (1.8V power supply), via a 240Ω resistance.
*3: It connects it with the ODT pin of DDR2SDRAM
*4: Pull down pin to VSS, via high resistance
*5: This is process of unused pin at 16 bit mode. Pull down the pin to VSS via high resistance.
Unused pins at 16 bit mode are as follows:
"MDQ[31:16], MDQSP[3:2], MDQSN[3:2]"
*6: This is process of MDM[3:2] at 16 bit mode. Be sure to open this pin.

7.2.22. MediaLB related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
MLB_DATA	IO	P	D	PD	HiZ	Data (optional) (*1)
MLB_SIG	IO	P	D	PD	HiZ	Control (optional) (*1)
MLB_CLK	I	-	D	CLK	-	Clock (optional) (*1)

*1: MediaLB pin of this LSI uses 3.3[V] I/O; therefore, when connecting bus's voltage is not 3.3[V], level conversion at external side is needed.

7.2.23. GPIO related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
GPIO_PD[23:0]	IO	-	D	PD (*1)	HiZ	General purpose I/O port (optional)

*1: GPIO_PD[12:6] is not applicable.

Pin No.	JEDEC	Pin name	Process
200	K3	VIN0[7]	Pull up to VDDE or pull down to VSS through high resistance.
201	L3	VIN0[3]	
202	M3	VINVSYNC0, GI1[5], MLB_DATA	Keep the pin open.
203	N3	VINHSYNC0, GI1[4], MLB_SIG	
204	P3	USB_AVSF1	Connect to VSS.
205	R3	USB_AVDF1	Connect to VDDE.
206	T3	USB_AVSF2	Connect to VSS.
207	U3	USB_AVDF2	Connect to VDDI.
208	V3	VIN1[7], RI1[7], GPIO_PD[5]	Keep the pin open.
209	W3	VIN1[4], RI1[4], CAN_RX0	
210	Y3	VIN1[1], GI1[7], I2S_SCK1	
211	AA3	VINVSYNC1, I2S_ECLK1	Pull up to VDDE or pull down to VSS through high resistance.
212	AB3	I2S_SDI2, BI1[2], SPI_DI	
213	AC3	IDE_DIORDY, Reserved (input)	
214	AD3	IDE_XCBLID, I2S_SCK1	Keep the pin open.
215	AD4	IDE_DDMARQ, I2S_ECLK1	Pull up to VDDE or pull down to VSS through high resistance.
216	AD5	IDE_DD[14], CAN_RX0	Keep the pin open.
217	AD6	IDE_DD[10], GPIO_PD[22]	
218	AD7	IDE_DD[6], GPIO_PD[18]	
219	AD8	IDE_DD[2], GPIO_PD[14]	
220	AD9	IDE_DA[1], PWM_O1	
221	AD10	IDE_XDIOR, Reserved (output)	
222	AD11	MPX_MODE_1[1]	Pull up to VDDE or pull down to VSS through high resistance.
224	AD13	AD_VIN0	Connect to VSS.
225	AD14	AD_VIN1	
227	AD16	UART_SOUT2	Keep the pin open.
228	AD17	SD_CMD	Pull up to VDDE or pull down to VSS through high resistance.
229	AD18	SD_DAT[2]	
230	AD19	USB_PRTPWR	Keep the pin open.
231	AD20	I2C_SDA0	Pull up to VDDE or pull down to VSS through high resistance.
232	AD21	INT_A[1]	
234	AD23	MA[9]	Keep the pin open.
235	AD24	MA[6]	
236	AC24	MA[2]	
237	AB24	MWE	
238	AA24	MRAS	
239	Y24	MDQ[5]	Pull down to VSS through high resistance.
240	W24	MDQ[1]	
241	V24	MDQ[7]	
242	U24	MDQ[10]	
243	T24	MDQ[9]	

8. Electrical Characteristics

8.1. Maximum Ratings

Table 8-1, Table 8-2, and Table 8-3 show the maximum ratings.

Table 8-1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	VDDI, PLLVDD VDDE DDRVDE	-0.5 to 1.8 (*1) -0.5 to 4.0 (*2) -0.5 to 2.5 (*3)	V
Input voltage	V_I	-0.5 to VDDI + 0.5 (< 1.8V) -0.5 to VDDE + 0.5 (< 4.0V) -0.5 to DDRVDE + 0.5 (< 2.5V)	V
Output voltage	V_O	-0.5 to VDDI + 0.5 (< 1.8V) -0.5 to VDDE + 0.5 (< 4.0V) -0.5 to DDRVDE + 0.5 (< 2.5V)	V
Storage temperature	T_{ST}	-55 to 125	°C
Junction temperature	T_J	-40 to 125	°C
Power consumption	P_D	1.5	W
Supply current	I_D	1.2V: 690.1 (*4) 1.8V: 508 (*4) 3.3V: 125.3 (*4)	mA

*1: Power supply for internal part or PLL
*2: Power supply for I/O part
*3: Power supply for SSTL_18 I/O part
*4: Current specification necessary for each voltage power supply

Note:

- Applying stress exceeding the maximum ratings (voltage, current, temperature, etc.) may cause damage to semiconductor devices. Never exceed the ratings above.
- Since thermal destruction of elements might occur, do not connect IC output or I/O pin directly, or connect them to V_{DD} or V_{SS} directly, except the pin designed output timing to prevent such incident.
- Provide ESD protection, such as grounding when handling the product; otherwise externally-charged electric charge flows into the IC and discharges, which may cause circuit destruction.
- Applying voltage higher than V_{DD} or lower than V_{SS} to I/O pins of CMOS IC, or applying voltage higher than the ratings between V_{DD} and V_{SS} may cause latch up. The latch up increases supply current, resulting in thermal destruction of elements. When handling the product, never exceed the maximum ratings.

8.4.1.2. 3.3V Standard CMOS I/O V-I Characteristic (Driving Capability 2)

Conditions	MIN:	Process = Slow	T_J = 125°C	VDDE = 3.0 V
	TYP:	Process = Typical	T_J = 25°C	VDDE = 3.3 V
	MAX:	Process = Fast	T_J = -40°C	VDDE = 3.6 V

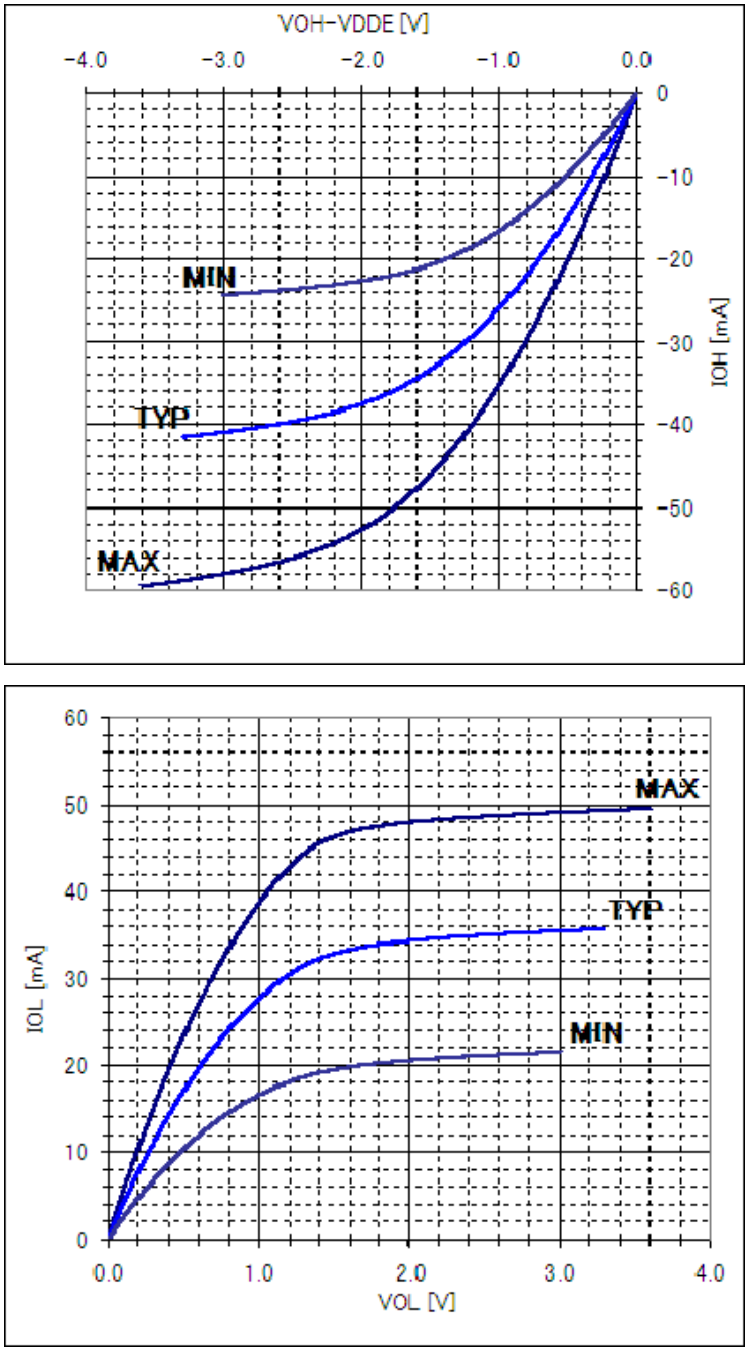


Figure 8-5 3.3V Standard CMOS I/O V-I Characteristic (Driving Capability 2)

8.5. AC CHARACTERISTIC

In this chapter, the AC timing of external ports is described.

8.5.1. Memory Controller Signal Timing

Table 8-21 Memory Controller AC Timing

Signal Name	Symbol	Description	Value			Unit
			Min	Typ	Max	
MEM_XCS0 MEM_XCS2 MEM_XCS4	t_{cso}	Chip Select delay time	–	–	10	ns
MEM_EA[24:1]	t_{ao}	Address delay time	–	–	11	ns
MEM_ED[31:0]	t_{do}	Data output delay time	–	–	11	ns
	t_{doz}	Data output HiZ time	–	–	12	ns
	t_{dsr}	SRAM/NOR Flash data setup time	12	–	–	ns
	t_{dhr}	SRAM/NOR Flash data hold time	0	–	–	ns
	t_{dsp}	NOR Flash page Read data setup time	13	–	–	ns
	t_{dhp}	NOR Flash page Read data hold time	0	–	–	ns
MEM_XRD	t_{rdo}	XRD delay time	–	–	10	ns
MEM_XWR[3:0]	t_{wro}	XWR delay time	–	–	10	ns

Standard clock of output delay is internal clock.
Standard clock of MEM_RDY is internal clock.

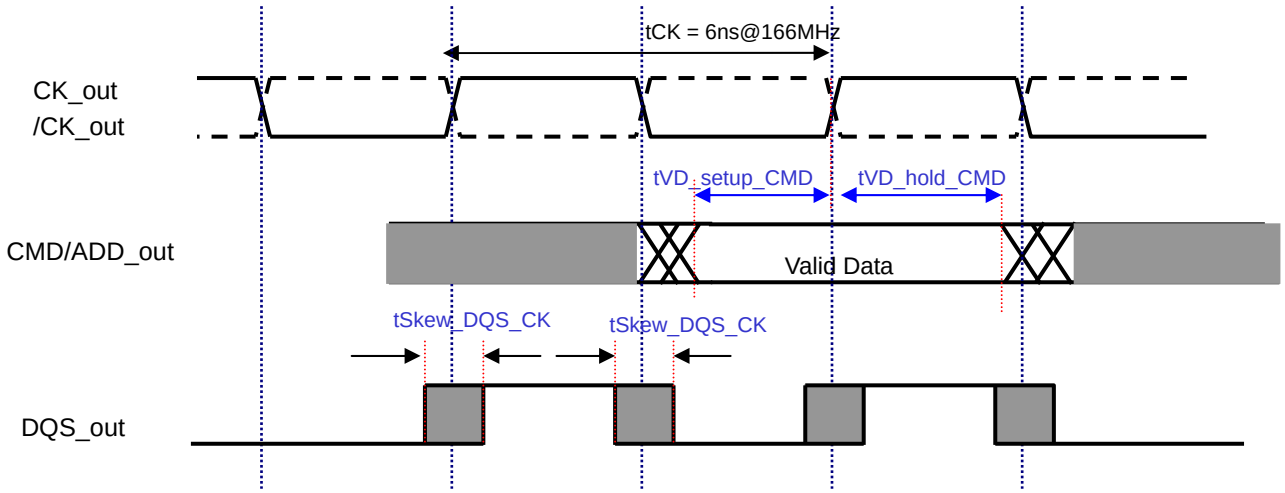


Figure 8-14 Write Spec (1 and 2): CK-CMD/ADD and CK-DQS

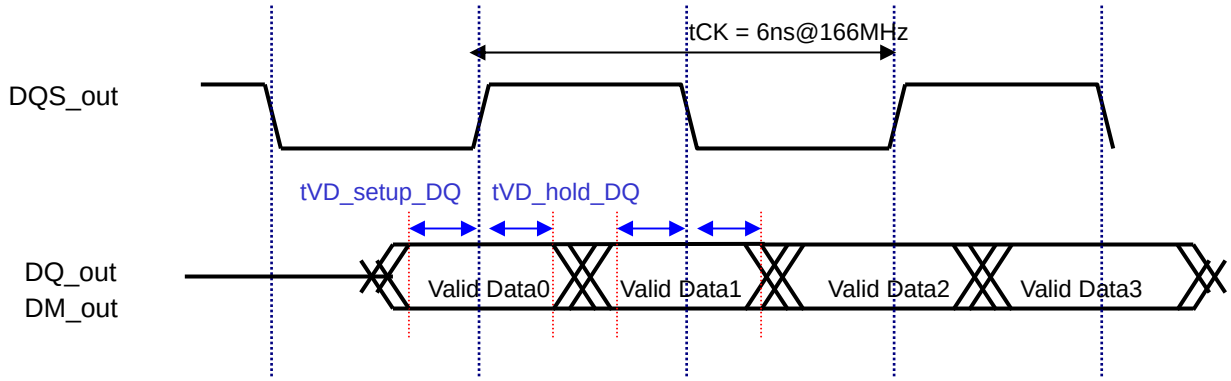


Figure 8-15 Write Spec (3): DQ-DQS

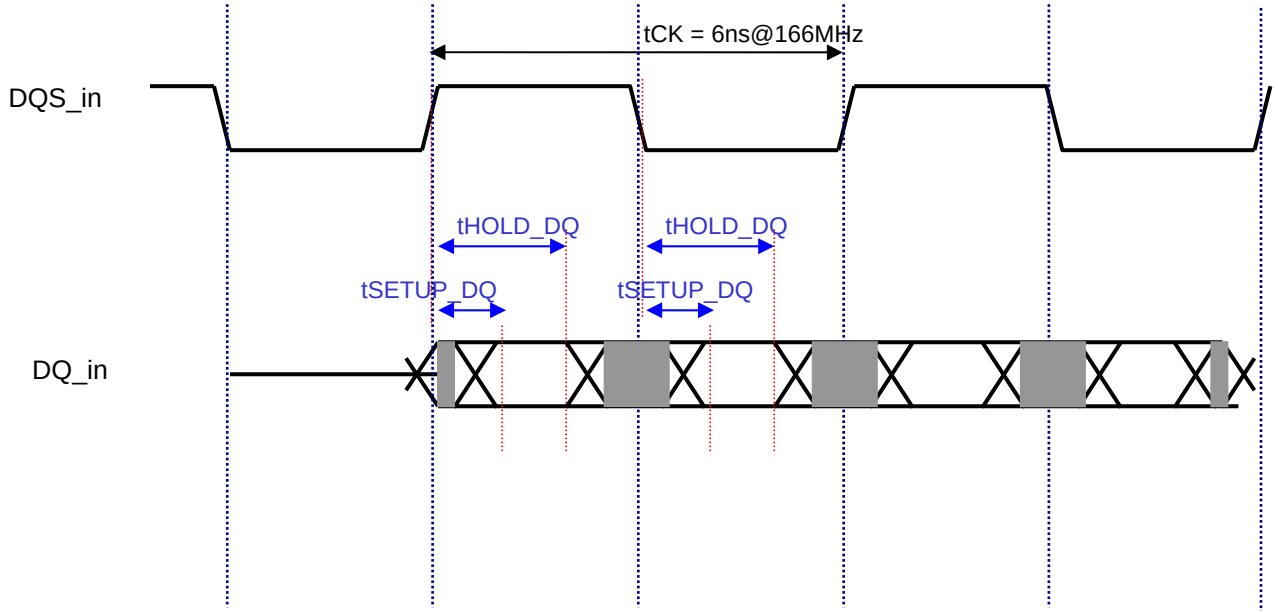


Figure 8-16 Read Spec (1): DQ-DQS

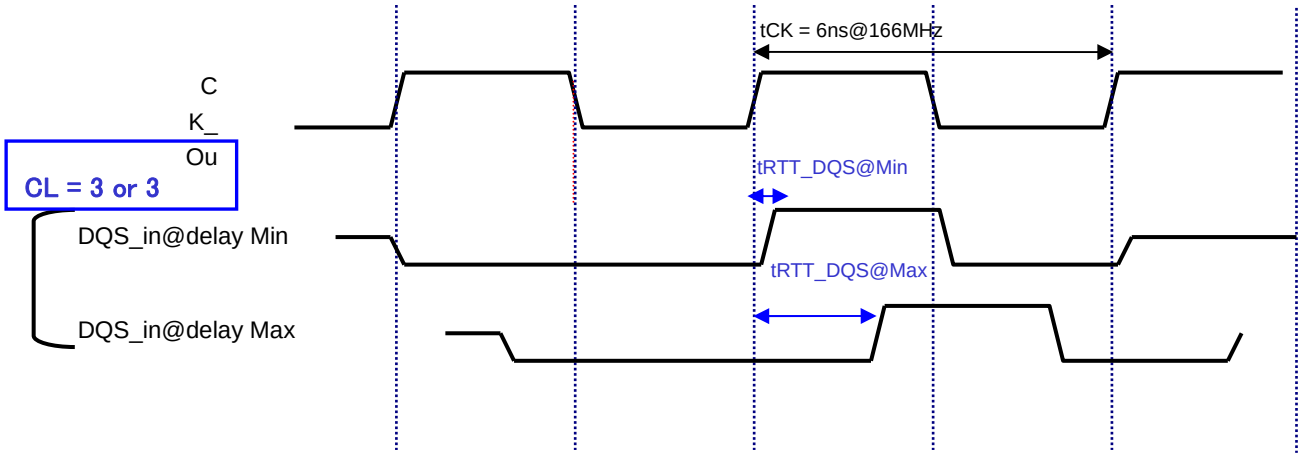


Figure 8-17 Read Spec (2): DQS-R.T.T (RoundTrip Time)

8.5.4. PWM Signal Timing

8.5.4.1. Output Signal

Table 8-27 AC Timing of Ide Data Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
PWM_O0	T0	Output delay of PWM_O0 based on APB-BusClock	2.0	–	14.0	ns
PWM_O1	T1	Output delay of PWM_O1 based on APB-BusClock	2.0	–	14.0	ns

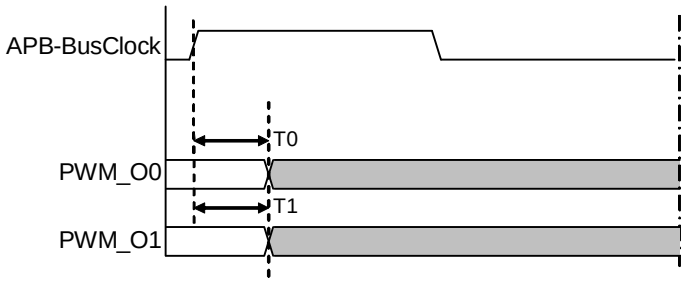


Figure 8-19 PWM Output Timing

8.5.5.3. Output Signal

Table 8-31 AC Timing of Video Interface Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
DOUTR0[5:0], DOUTG0[5:0], DOUTB0[5:0]	Tdrgb0	RGB output delay time	0	–	5.5	ns
DOUTR1[5:0], DOUTG1[5:0], DOUTB1[5:0]	Tdrgb1	RGB output delay time	0	–	5.5	ns
HSYNC0 (o)	Tdhsync0	HSYNC output delay time	0	–	5.5	ns
HSYNC1 (o)	Tdhsync1	HSYNC output delay time	0	–	5.5	ns
VSYNC0 (o)	Tdvsync0	VSYNC output delay time	0	–	5.5	ns
VSYNC1 (o)	Tdvsync1	VSYNC output delay time	0	–	5.5	ns
CSYNC0	Tdcsync0	CSYNC output delay time	0	–	5.5	ns
CSYNC1	Tdcsync1	CSYNC output delay time	0	–	5.5	ns
GV0	Tdgv0	GV output delay time	0	–	5.5	ns
GV1	Tdgv1	GV output delay time	0	–	5.5	Ns

Note: If hold time is deficient, inverting DCLKO clock is recommended.

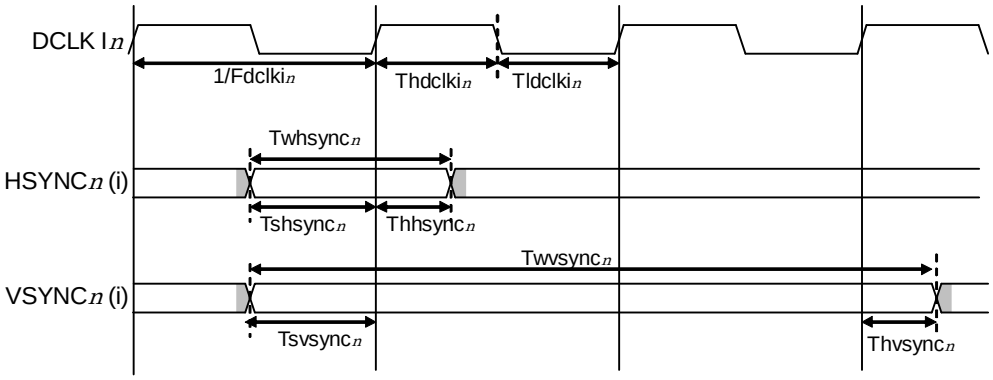


Figure 8-20 Display Input Signal Timing

8.5.11. CAN Signal Timing

Table 8-39 CAN AC Timing

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
CAN_TX0 CAN_TX1	t_{do}	Data output delay time	–	–	17	ns
CAN_RX0 CAN_RX1	t_{dw}	Input data width	1000	–	–	ns

Internal clock is the standard of output delay.

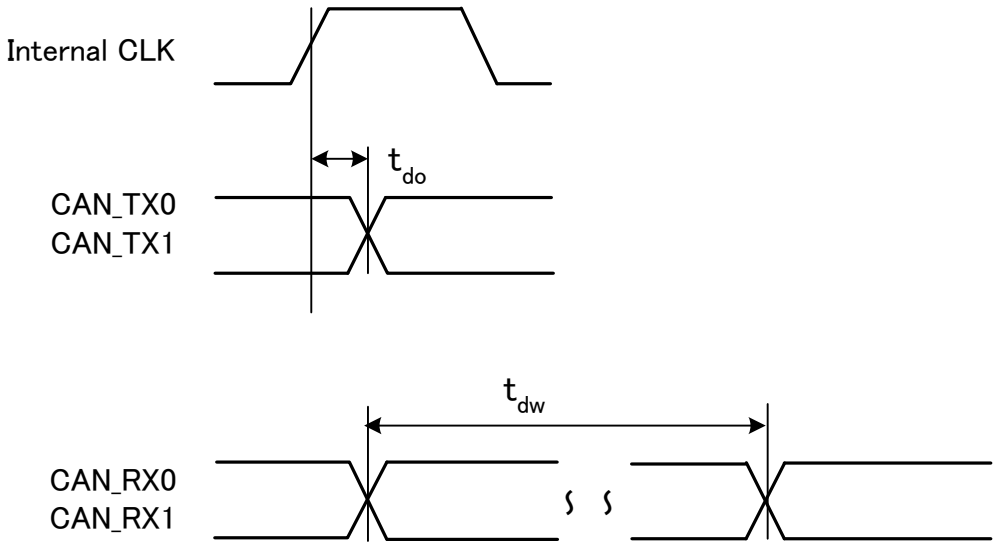


Figure 8-29 CAN Timing

8.5.12.2. MediaLB AC Spec Type B

Ground = 0V, Load capacitance = 40pF, MediaLB speed = 1024Fs, and Fs = 48kHz.
All timing parameters are specified from the valid voltage threshold as listed below; unless otherwise noted.

8.5.12.2.1. Clock

Table 8-43 AC Timing of Clock Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBCLK	f_{mck}	MLBCLK operating frequency (*1)	45.056 – –	– 49.152 –	– – 49.2544	MHz	1024xFs at 44.0kHz 1024xFs at 48.0kHz 1024xFs at 48.1kHz
	t_{mckr}	MLBCLK rising time	–	–	1	ns	V_{IL} to V_{IH}
	t_{mckf}	MLBCLK falling time	–	–	1	ns	V_{IH} to V_{IL}
	t_{mckc}	MLBCLK cycle time	–	20.3	–	ns	
	t_{mckl}	MLBCLK low time	6.8	7.8	–	ns	
	t_{mckh}	MLBCLK high time	9.7	10.4	–	ns	
	t_{mpwv}	MLBCLK pulse width variation	–	–	0.5	ns pp	(*2)

*1: The controller can shut off MLBCLK to place MediaLB in a low-power state.
*2: Pulse width variation is measured at 1.25V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).

8.5.12.2.2. Input Signal

Table 8-44 AC Timing of Input Signal

Signal Name	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBSIG, MLBDAT input	t_{dsmcf}	MLBSIG and MLBDAT input valid to MLBCLK falling	1	–	–	ns	
	t_{dhmcf}	MLBSIG and MLBDAT input hold from MLBCLK low	0	–	–	ns	

8.5.12.2.3. Output signal

Table 8-45 AC Timing of Output Signal

Signal Name	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBSIG, MLBDAT Output	t_{mcfdz}	MLBSIG and MLBDAT output high impedance from MLBCLK low	0	–	t_{mckl}	ns	
	t_{mdzh}	Bus hold time	2	–	–	ns	(*1)

*1: The board must be designed to ensure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

8.5.17. EXIRC Signal Timing

Table 8-55 AC Timing

Signal Name	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
INT_A[3:0]	t_{dw}	Input data-width	A	–	–	ns

The case that external interrupt input request is edge (rising edge and falling edge), input data width (tdw) is regulated as follows. When level ("H" or "L") is selected as the request, it should be held until interrupt process is completed.
A indicates APB bus clock cycle.

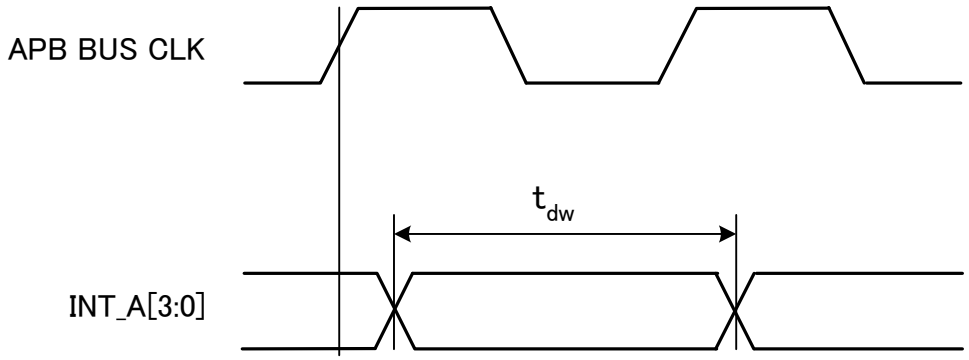


Figure 8-39 EXIRC Timing