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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

**Embedded - Microcontrollers - Application Specific** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Obsolete |
| Applications | Automotive Mirror Control |
| Core Processor | HC08 |
| Program Memory Type | FLASH (16kB) |
| Controller Series | 908E |
| RAM Size | 512 x 8 |
| Interface | SCI, SPI |
| Number of I/O | 13 |
| Voltage - Supply | 8V ~ 18V |
| Operating Temperature | -40°C ~ 115°C |
| Mounting Type | Surface Mount |
| Package / Case | 54-SSOP (0.295", 7.50mm Width) Exposed Pad |
| Supplier Device Package | 54-SOIC-EP |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e626avdwb |

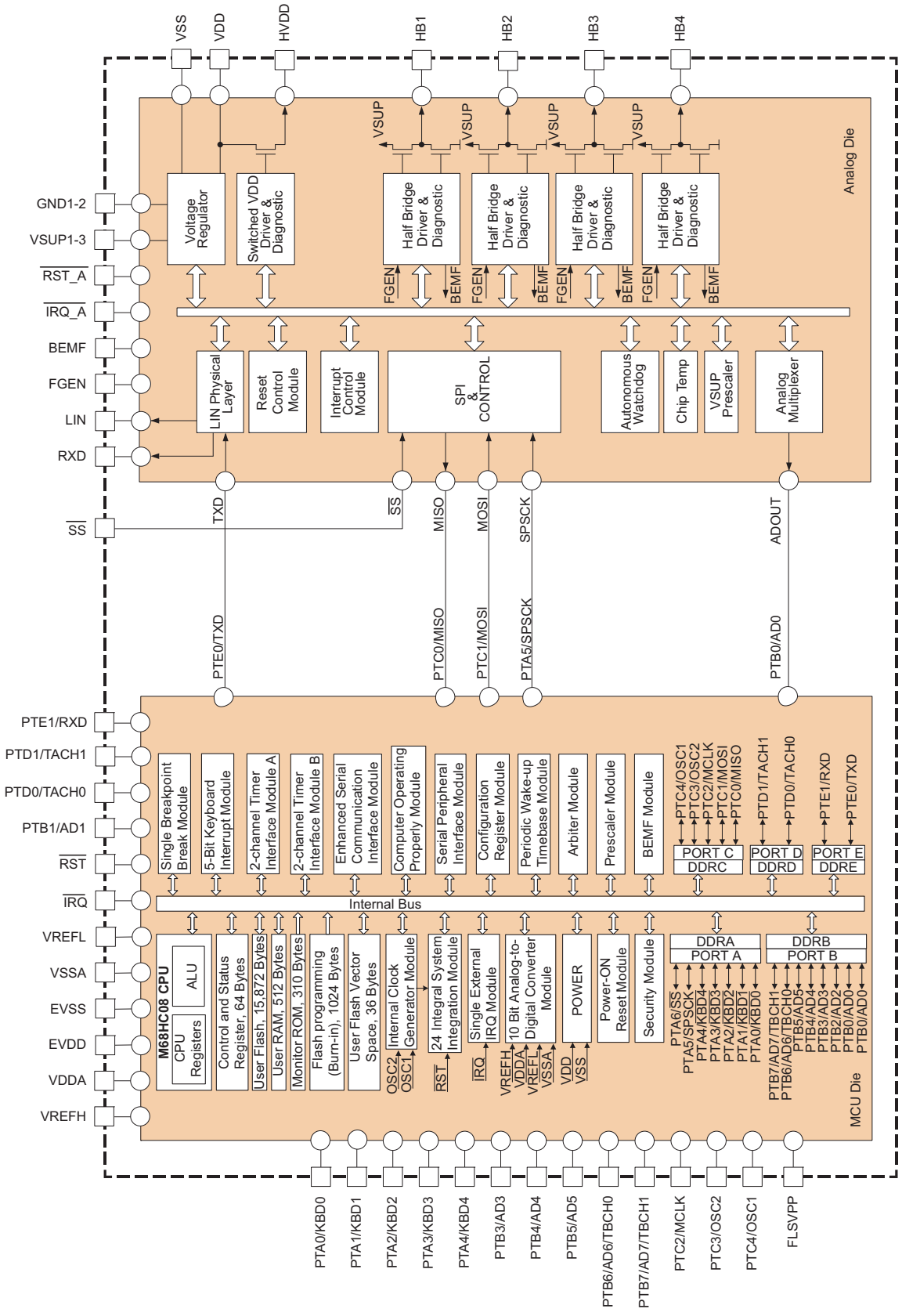



**Figure 2. 908E626 Simplified Internal Block Diagram**

# ELECTRICAL CHARACTERISTICS

## *MAXIMUM RATINGS*

**Table 2. MAXIMUM RATINGS**

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| **ELECTRICAL RATINGS** | | | |
| Supply Voltage | | | V |
| Analog Chip Supply Voltage under Normal Operation (Steady-state) | $V_{SUP(SS)}$ | -0.3 to 28 | |
| Analog Chip Supply Voltage under Transient Conditions (1) | $V_{SUP(PK)}$ | -0.3 to 40 | |
| Microcontroller Chip Supply Voltage | $V_{DD}$ | -0.3 to 6.0 | |
| Input Pin Voltage | | | V |
| Analog Chip | $V_{IN(ANALOG)}$ | -0.3 to 5.5 | |
| Microcontroller Chip | $V_{IN(MCU)}$ | $V_{SS}$-0.3 to $V_{DD}$+0.3 | |
| Maximum Microcontroller Current per Pin | | | mA |
| All Pins Except VDD, VSS, PTA0:PTA6, PTC0:PTC1 | $I_{PIN(1)}$ | ±15 | |
| Pins PTA0:PTA6, PTC0:PTC1 | $I_{PIN(2)}$ | ±25 | |
| Maximum Microcontroller $V_{SS}$ Output Current | $I_{MVSS}$ | 100 | mA |
| Maximum Microcontroller $V_{DD}$ Input Current | $I_{MVDD}$ | 100 | mA |
| LIN Supply Voltage | | | V |
| Normal Operation (Steady-state) | $V_{BUS(SS)}$ | -18 to 28 | |
| Transient Conditions (1) | $V_{BUS(DYNAMIC)}$ | 40 | |
| ESD Voltage | | | V |
| Human Body Model (2) | $V_{ESD1}$ | ±3000 | |
| Machine Model (3) | $V_{ESD2}$ | ±150 | |
| Charge Device Model (4) | $V_{ESD3}$ | ±500 | |

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω).
4. ESD3 testing is performed in accordance with Charge Device Model, robotic ($C_{ZAP}$ = 4.0 pF).

**Table 2. MAXIMUM RATINGS**

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| **THERMAL RATINGS** | | | |
| Storage Temperature | $T_{STG}$ | -40 to 150 | °C |
| Operating Case Temperature (5) | $T_C$ | -40 to 115 | °C |
| Operating Junction Temperature(6) | $T_J$ | -40 to 135 | °C |
| Peak Package Reflow Temperature During Solder Mounting (7)(8) | $T_{PPRT}$ | Note 8 | °C |

Notes

5. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
6. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150 °C under these conditions
7. Pin soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

## DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS**

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ $V_{SUP}$ ≤ 16 V, -40 °C ≤ $T_J$ ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **LIN PHYSICAL LAYER** | | | | | |
| Propagation Delay (14), (15) | | | | | µs |
| TXD LOW to LIN LOW | $t_{TXD-LIN-LOW}$ | – | – | 6.0 | |
| TXD HIGH to LIN HIGH | $t_{TXD-LIN-HIGH}$ | – | – | 6.0 | |
| LIN LOW to RXD LOW | $t_{LIN-RXD-LOW}$ | – | 4.0 | 8.0 | |
| LIN HIGH to RXD HIGH | $t_{LIN-RXD-HIGH}$ | – | 4.0 | 8.0 | |
| TXD Symmetry | $t_{TXD-SYM}$ | -2.0 | – | 2.0 | |
| RXD Symmetry | $t_{RXD-SYM}$ | -2.0 | – | 2.0 | |
| Output Falling Edge Slew Rate (14), (16) | $SR_F$ | | | | V/µs |
| 80% to 20% | | -1.0 | -2.0 | -3.0 | |
| Output Rising Edge Slew Rate (14), (16) | $SR_R$ | | | | V/µs |
| 20% to 80%, $R_{BUS}$ > 1.0 kΩ, $C_{BUS}$ < 10 nF | | 1.0 | 2.0 | 3.0 | |
| LIN Rise/Fall Slew Rate Symmetry (14), (16) | $SR_S$ | -2.0 | – | 2.0 | µs |
| **AUTONOMOUS WATCHDOG (AWD)** | | | | | |
| AWD Oscillator Period | $t_{OSC}$ | – | 40 | – | µs |
| AWD Period Low = 512 $t_{OSC}$ | $t_{AWDPH}$ | | | | ms |
| TJ < 25 °C | | 16 | 27 | 34 | |
| TJ ≥ 25 °C | | 16 | 22 | 28 | |
| AWD Period High = 256 $t_{OSC}$ | $t_{AWDPL}$ | | | | ms |
| TJ < 25 °C | | 8.0 | 13.5 | 17 | |
| TJ ≥ 25 °C | | 8.0 | 11 | 14 | |
| AWD Cyclic Wake-up On Time | $t_{AWDHPON}$ | – | 90 | – | µs |

Notes
14. All LIN characteristics are for initial LIN slew rate selection (20 kbaud) (SRS0:SRS1= 00).
15. See Figure 4, page 12.
16. See Figure 5, page 13.

## MICROCONTROLLER PARAMETRICS

**Table 5. MICROCONTROLLER**

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

| Module | Description |
|---|---|
| Core | High Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz |
| Timer | Two 16-Bit Timers with Two Channels (TIM A and TIM B) |
| Flash | 16 k Bytes |
| RAM | 512 Bytes |

**Table 5. MICROCONTROLLER**

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

| Module | Description |
|---|---|
| ADC | 10 Bit Analog-to-Digital Converter |
| SPI | SPI Module |
| ESCI | Standard Serial Communication Interface (SCI) Module<br>Bit-Time Measurement<br>Arbitration<br>Prescaler with Fine Baud Rate Adjustment |
| ICG | Internal Clock Generation Module |
| BEMF Counter | Special Counter for *SMARTMOS* BEMF Output |

## TIMING DIAGRAMS

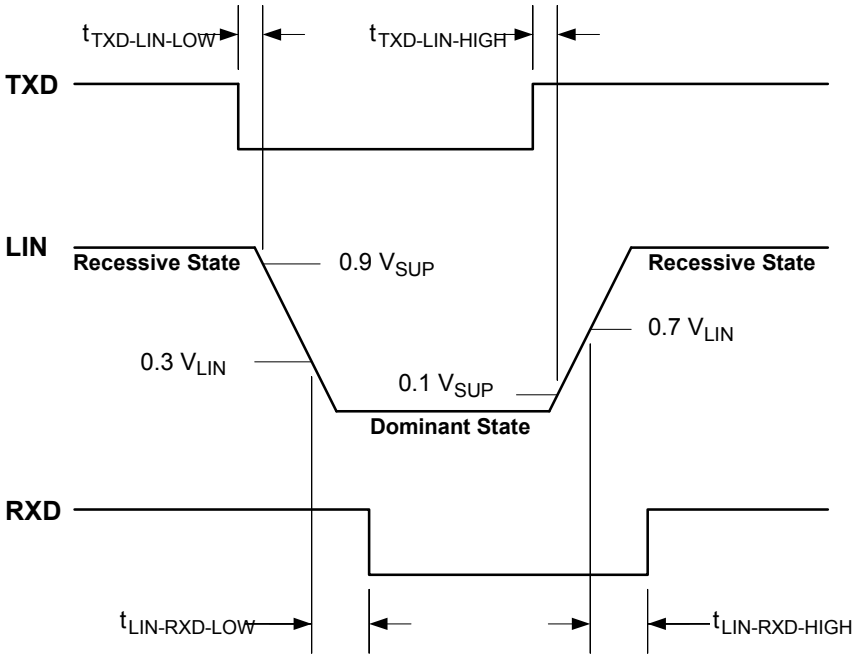
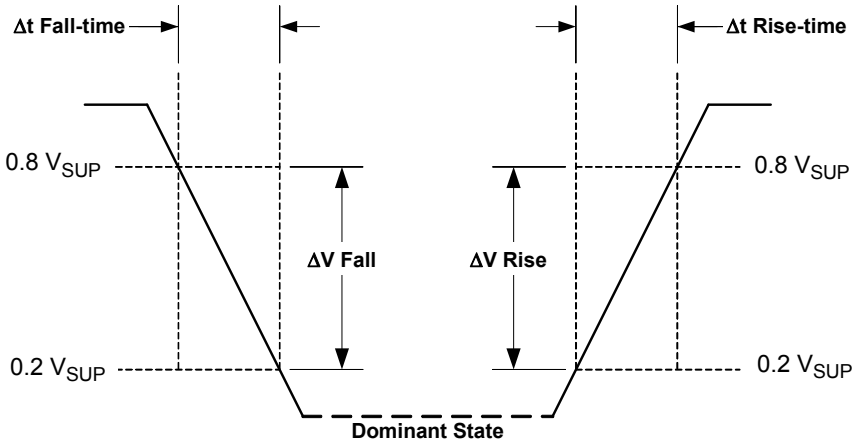



**Figure 4. LIN Timing Description**




$$SR_F = \frac{\Delta V\ Fall}{\Delta t\ Fall\text{-}time} \qquad SR_R = \frac{\Delta V\ Rise}{\Delta t\ Rise\text{-}time}$$

**Figure 5. LIN Slew Rate Description**

## *FUNCTIONAL DIAGRAMS*

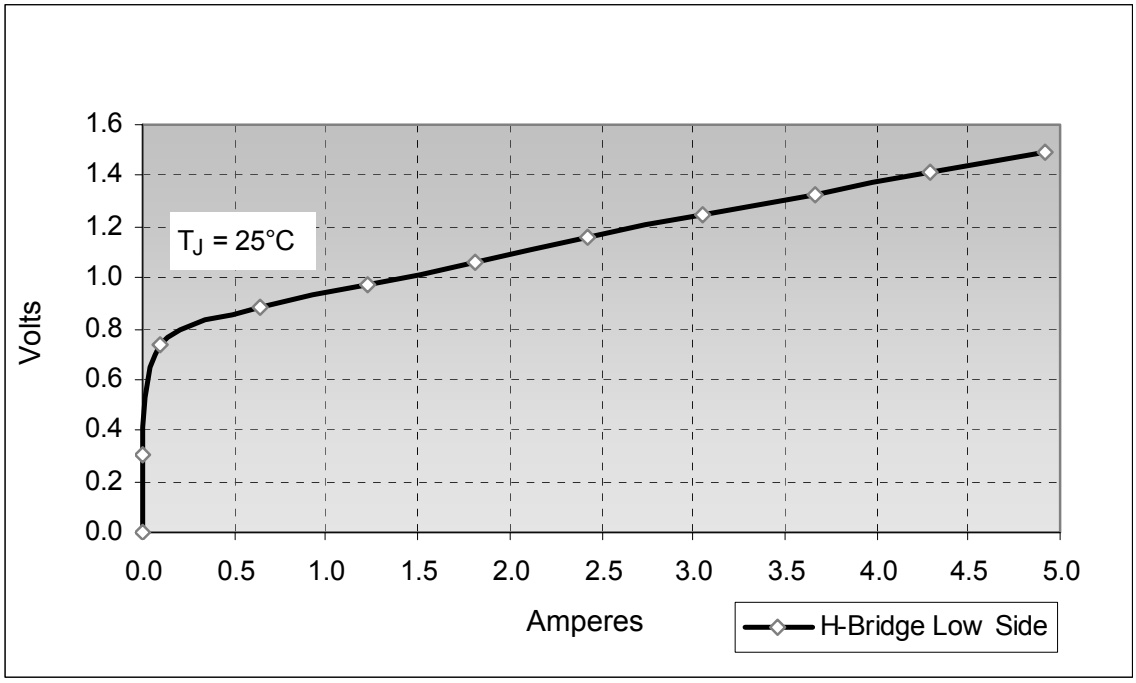



**Figure 6. Free Wheel Diode Forward Voltage**

# FUNCTIONAL DESCRIPTION

## INTRODUCTION

The 908E626 device was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E626 is well suited to perform stepper motor control, e.g. for climate or light-levelling control via a 3-wire LIN bus.

This device combines an standard HC08 MCU core (68HC908EY16) with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as four half-bridge outputs. Other ports are also provided including a selectable HVDD pin. An internal voltage regulator is provided on the *SMARTMOS* IC chip, which provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables the device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and the third for ground.

## FUNCTIONAL PIN DESCRIPTION

See Figures 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on Figures 3 for a depiction of the pin locations on the package.

### PORT A I/O PINS (PTA0:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins, KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die. The PTA6/$\overline{SS}$ pin is likewise not accessible.

For details refer to the 68HC908EY16 datasheet.

### PORT B I/O PINS (PTB1, PTB3:7)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module. The PTB6:PTB7 pins are also shared with the Timer B module.

PTB0/AD0 is internally connected to the ADOUT pin of the analog die, allowing diagnostic measurements to be calculated; e.g., current recopy, $V_{SUP}$, etc. The PTB2/AD2 pin is not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

### PORT C I/O PINS (PTC2:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details refer to the 68HC908EY16 datasheet.

### PORT D I/O PINS (PTD0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special function, bidirectional I/O port pins that can also be programmed to be timer pins.

In step motor applications, the PTD0 pin should be connected to the BEMF output of the analog die, to evaluate the BEMF signal with a special BEMF module of the MCU.

PTD1 pin is recommended for use as an output pin for generating the FGEN signal (PWM signal), if required by the application.

### PORT E I/O PIN (PTE1)

PTE1/RXD and PTE0/TXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die.The connection for the receiver must be done externally.

### EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

### EXTERNAL RESET PIN ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

### CURRENT LIMITATION FREQUENCY INPUT PIN (FGEN)

Input pin for the half-bridge current limitation PWM frequency. This input is not a real PWM input pin; it should just supply the period of the PWM. The duty cycle will be generated automatically.

**Important** The recommended FGEN frequency should be in the range of 0.1 kHz to 20 kHz.

### BACK ELECTROMAGNETIC FORCE OUTPUT PIN (BEMF)

This pin gives the user information about back electromagnetic force (BEMF). This feature allows stall detection and coil failures in step motor applications. In order to evaluate this signal the pin must be directly connected to pin PTD0/TACH0/BEMF.

### RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset pin of the analog die. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

### INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

### SLAVE SELECT PIN ($\overline{\text{SS}}$)

This pin is the SPI Slave Select pin for the analog chip. All other SPI connections are done internally. $\overline{\text{SS}}$ must be connected to PTB1 or any other logic I/O of the microcontroller.

### LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

### HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E626 device includes power MOSFETs configured as four half-bridge driver outputs. The HB1:HB4 outputs may be configured for step motor drivers, DC motor drivers, or as high side and low side switches.

The HB1:HB4 outputs are short-circuit and overtemperature protected, and they feature current recopy, current limitation, and BEMF generation. Current limitation and recopy are done on the low side MOSFETs.

### POWER SUPPLY PINS (VSUP1:VSUP3)

VSUP1:VSUP3 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

### POWER GROUND PINS (GND1 AND GND2)

GND1 and GND2 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

### SWITCHABLE $V_{DD}$ OUTPUT PIN (HVDD)

The HVDD pin is a switchable $V_{DD}$ output for driving resistive loads requiring a regulated 5.0 V supply; The output is short-circuit protected.

### +5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

**Important** The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD, VDDA, and VREFH pins must be connected together.

### VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors).

**Important** VSS, EVSS, VSSA, and VREFL pins must be connected together.

### LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

### ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

**Important** VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

### ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

**Important** VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces.

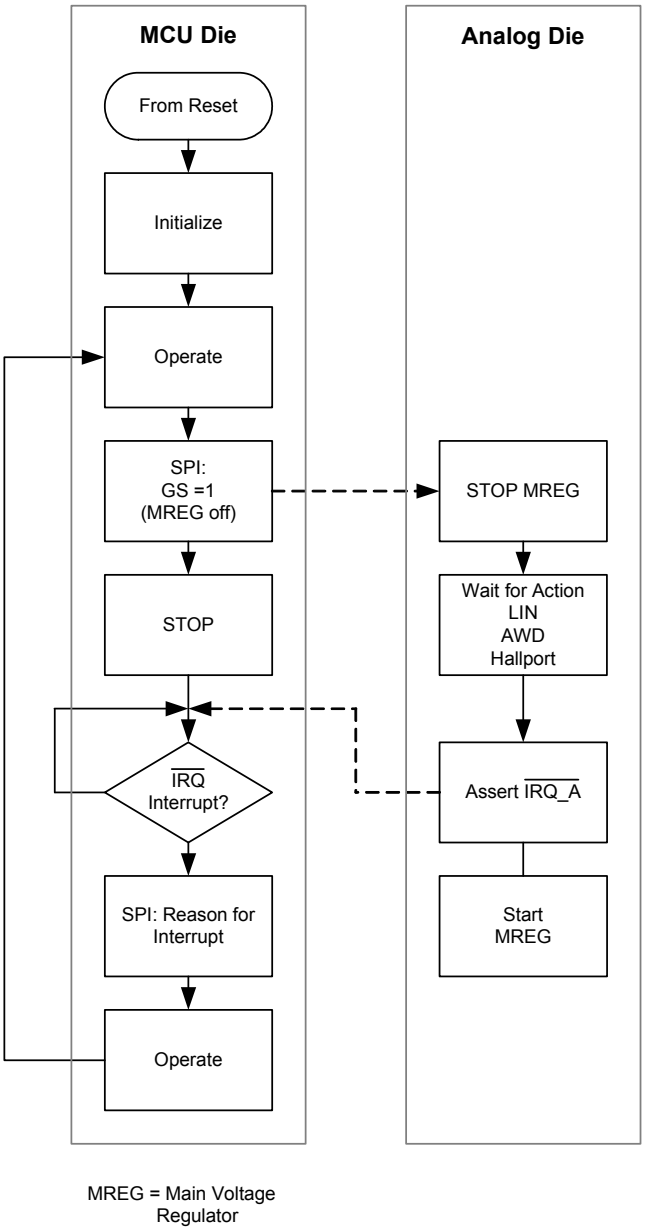



**Figure 8. STOP Mode/Wake-up Procedure**

## INTERRUPT FLAG REGISTER (IFR)

**Register Name and Address: IFR - $05**

| | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | LINF | HTF | LVF | HVF | OCF | 0 |
| Write | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### LINF—LIN FLAG BIT

This read/write flag is set on the falling edge at the LIN data line. Clear LINF by writing a logic [1] to LINF. Reset clears the LINF bit. Writing a logic [0] to LINF has no effect.

- 1 = Falling edge on LIN data line has occurred.
- 0 = Falling edge on LIN data line has not occurred since last clear.

### HTF—HIGH TEMPERATURE FLAG BIT

This read/write flag is set on a high temperature condition. Clear HTF by writing a logic [1] to HTF. If a high temperature condition is still present while writing a logic [1] to HTF, the writing has no effect. Therefore, a high temperature interrupt cannot be lost due to inadvertent clearing of HTF. Reset clears the HTF bit. Writing a logic [0] to HTF has no effect.

- 1 = High temperature condition has occurred.

## HALF-BRIDGES

Outputs HB1:HB4 provide four low resistive half-bridge output stages. The half-bridges can be used in H-Bridge, high side, or low side configurations.

Reset clears all bits in the H-Bridge Output Register (HBOUT) owing to the fact that all half-bridge outputs are switched off.

HB1:HB4 output features:

- Short-circuit (overcurrent) protection on high side and low side MOSFETs.
- Current recopy feature (low side MOSFET).
- Overtemperature protection.
- Overvoltage and undervoltage protection.
- Current limitation feature (low side MOSFET).

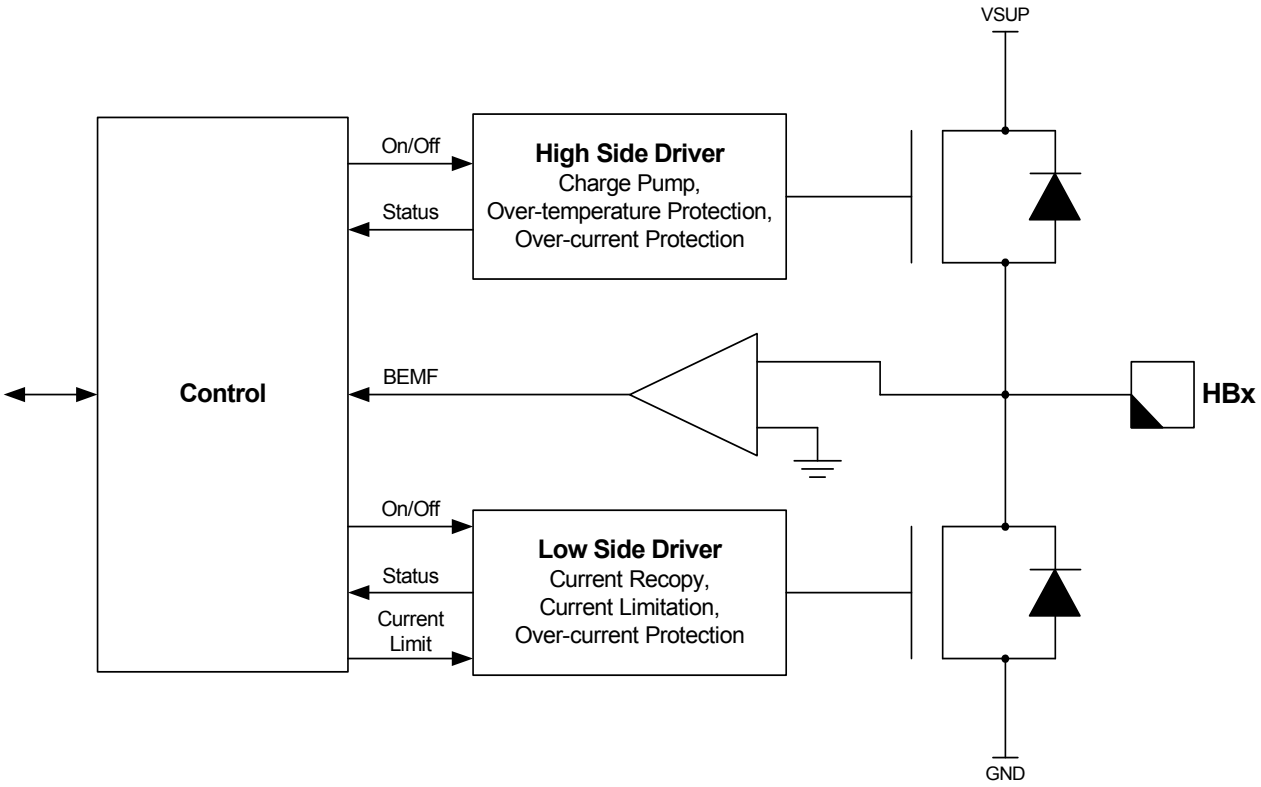



**Figure 12. Half-bridge Push-Pull Output Driver**

### Half-bridge Control

Each output MOSFET can be controlled individually. The general enable of the circuitry is done by setting PSON in the System Control Register (SYSCTL). HBx_L and HBx_H form one half-bridge. It is not possible to switch on both MOSFETs in one half-bridge at the same time. If both bits are set, the high side MOSFET has a higher priority.

To avoid both MOSFETs (high side and low side) of one half-bridge being on at the same time, a break-before-make circuit exists.Switching the high side MOSFET on is inhibited as long as the potential between gate and $V_{SS}$ is not below a certain threshold. Switching the low side MOSFET on is blocked as long as the potential between gate and source of the high side MOSFET did not fall below a certain threshold.

### Half-bridge Output Register (HBOUT)

**Register Name and Address: HBOUT - $01**

| | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | HB4_H | HB4_L | HB3_H | HB3_L | HB2_H | HB2_L | HB1_H | HB1_L |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### HBx_L—Low Side On/Off Bits

These read/write bits turn on the low side MOSFETs. Reset clears the HBx_L bits.

- 1 = Low side MOSFET turned on for half-bridge output x.
- 0 = Low side MOSFET turned off for half-bridge output x.

### HBx_H—High Side On/Off Bits

These read/write bits turn on the high side MOSFETs. Reset clears the HBx_H bits.

- 1 = High side MOSFET turned on for half-bridge output x.
- 0 = High side MOSFET turned on for half-bridge output x.

## HALF-BRIDGE CURRENT LIMITATION

Each low side MOSFET offers a current limit or constant current feature. This features is realized by a pulse width modulation on the low side MOSFET. The pulse width modulation on the outputs is controlled by the FGEN input and the load characteristics. The FGEN input provides the PWM frequency, whereas the duty cycle is controlled by the load characteristics.

The recommended frequency range for the FGEN and the PWM is 0.1 kHz to 20 kHz.

### Functionality

Each low side MOSFET switches off if a current above the selected current limit was detected. The 908E626 offers five different current limits (refer to Table 8, for current limit values). The low side MOSFET switches on again if a rising edge on the FGEN input was detected (Figure 13).

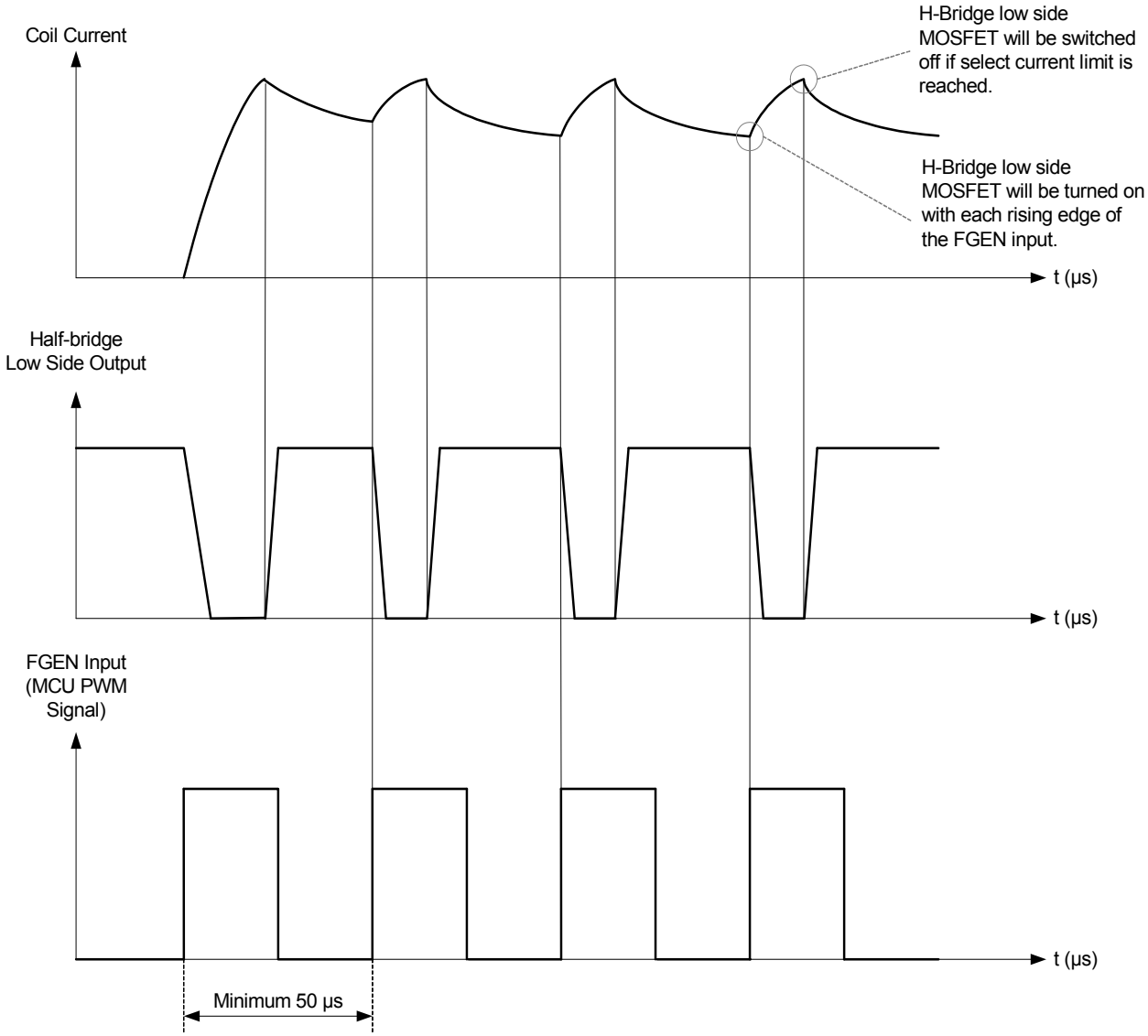



**Figure 13. Half-bridge Current Limitation**

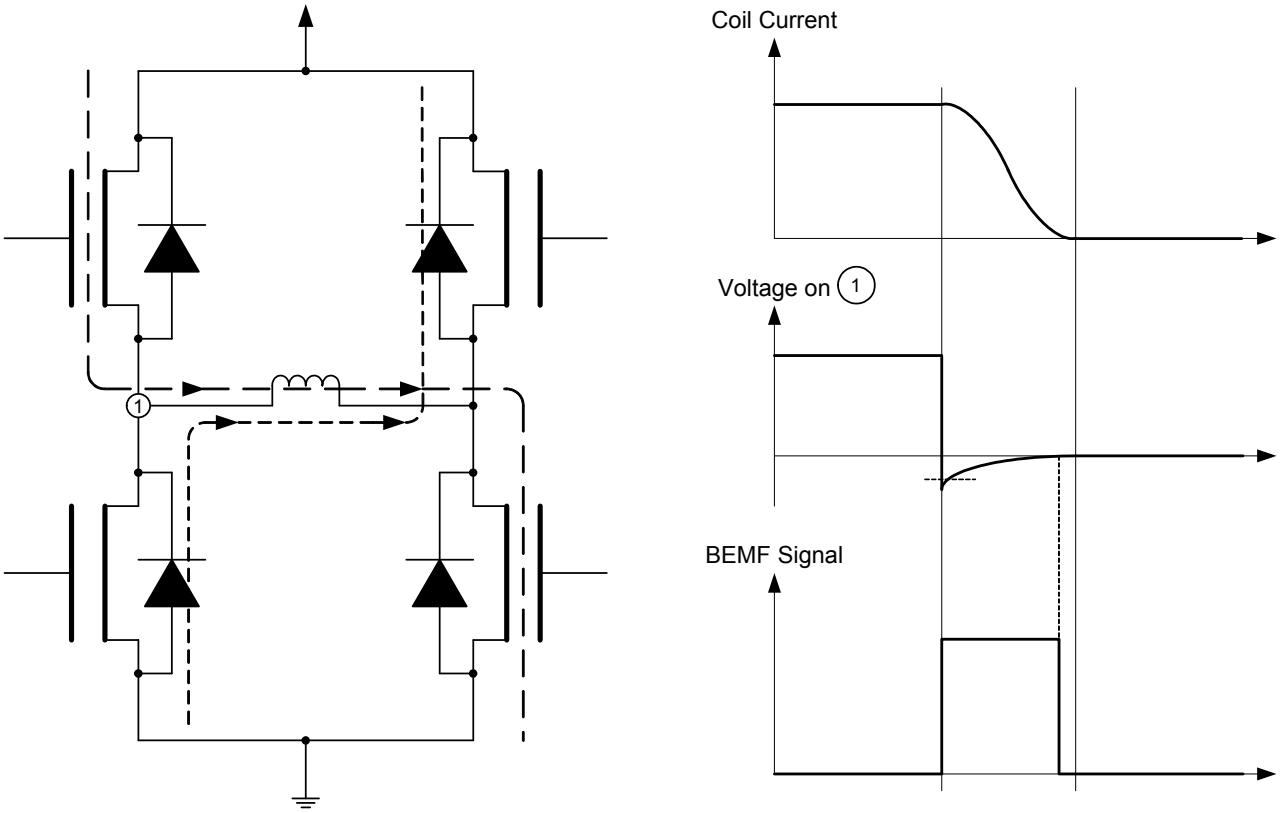



**Figure 15. BEMF Signal Generation**

## HALF-BRIDGE OVERTEMPERATURE PROTECTION

The half-bridge outputs provide an overtemperature prewarning with the HTF in the Interrupt Flag Register (IFR). In order to protect the outputs against overtemperature, the High Temperature Reset must be enabled. If this value is reached, the part generates a reset and disables all power outputs.

## HALF-BRIDGE OVERCURRENT PROTECTION

The half-bridges are protected against short to GND, short to VSUP, and load shorts.

In the event an overcurrent on the high side is detected, the high side MOSFETs on all HB high side MOSFETs are switched off automatically. In the event an overcurrent on the low side is detected, all HB low side MOSFETs are switched off automatically. In both cases, the overcurrent status flag HB_OCF in the System Status Register (SYSSTAT) is set.

The overcurrent status flag is cleared (and the outputs re-enabled) by writing a logic [1] to the HB_OCF flag in the System Status Register or by reset.

## HALF-BRIDGE OVERVOLTAGE/UNDERVOLTAGE

The half-bridge outputs are protected against undervoltage and overvoltage conditions. This protection is done by the low and high voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the outputs are automatically disabled.

The overvoltage/undervoltage status flags are cleared (and the outputs re-enabled) by writing a logic [1] to the LVF/HVF flags in the Interrupt Flag Register or by reset. Clearing this flag is useless as long as a high or low voltage condition is present.

### Half-bridge Control Register (HBCTL)

**Register Name and Address: HBCTL - $02**

| | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Read | OFC_EN | CSA | 0 | 0 | 0 | CLS2 | CLS1 | CLS0 |
| Write | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### OFC_EN—H-bridge Offset Chopping Enable Bit

This read/write bit enables offset chopping. Reset clears the OFC_EN bit.

- 1 = Offset chopping enabled.
- 0 = Offset chopping disabled.

### CSA—H-bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-bridges. Reset clears the CSA bit.

## VOLTAGE REGULATOR

The 908E626 chip contains a low power, low drop voltage regulator to provide internal power and external power for the MCU. The $V_{DD}$ regulator accepts a unregulated input supply and provides a regulated $V_{DD}$ supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Note: Under loss of power conditions, the discharge of the $V_{DD}$ capacitor may occur relatively slow. Based on the selected external components and external $V_{DD}$ load, additional external load may be required guarantee the MCU POR threshold being reached before the next power up.

### RUN Mode

During RUN mode, the main voltage regulator is on. It provides a regulated supply to all digital sections.

### STOP Mode

During STOP mode the STOP mode regulator supplies a regulated output voltage. The STOP mode regulator has a very limited output current capability. The output voltage will be lower than the output voltage of the main voltage regulator.

## *FACTORY TRIMMING AND CALIBRATION*

To enhance the ease-of-use of the 908E626, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the *empty* (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

### Trim Values

Below the usage of the trim values located in the flash memory is explained

### Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as ±25%, due to process, temperature, and voltage dependencies. To compensate this dependencies a ICG trim values is located at address $FDC2. After trimming the ICG is a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100 nF) and stabilized (4.7 µF) $V_{DD}$ = 5.0 V, $T_{AMBIENT}$~25 °C) and will vary over temperature and voltage (VDD) as indicated in the 68HC908EY16 datasheet.

To trim the ICG this values has to be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

**Important** The value has to be copied after every reset.

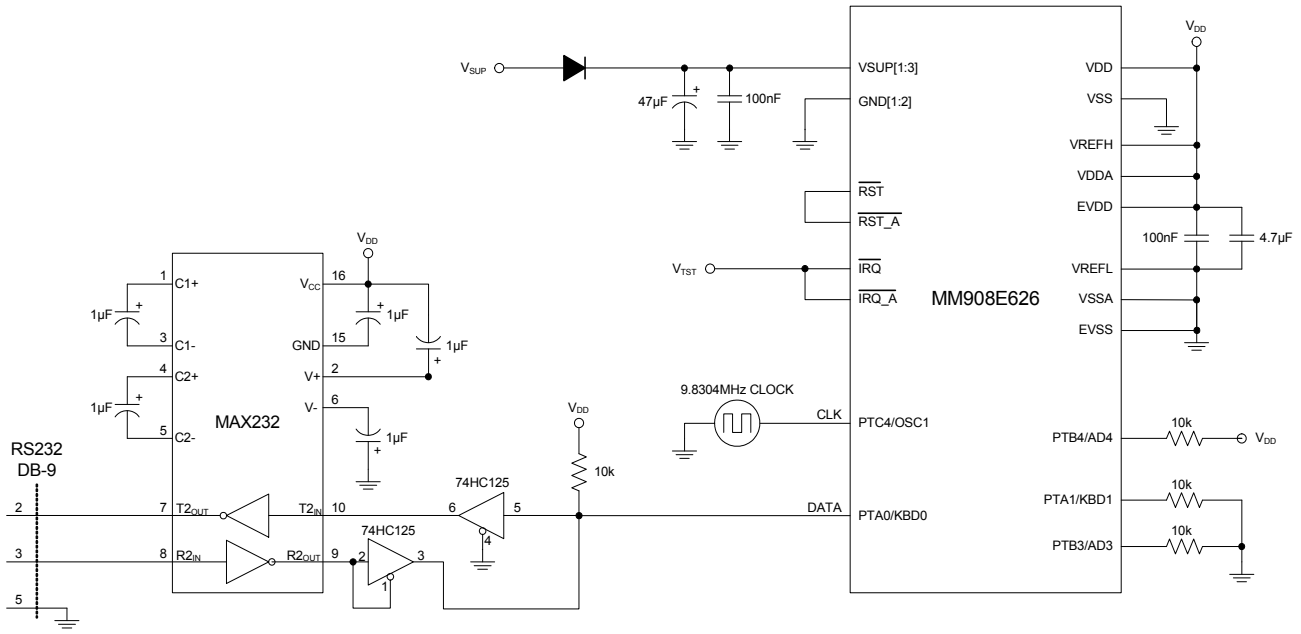



**Figure 17. Normal Monitor Mode Circuit**

Table 10 summarizes the possible configurations and the necessary setups.

**Table 10. Monitor Mode Signal Requirements and Options**

| Mode | IRQ | RST | Reset Vector | Serial Communication | | Mode Selection | | ICG | COP | Normal Request Timeout | Communication Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PTA0 | PTA1 | PTB3 | PTB4 | | | | External Clock | Bus Frequency | Baud Rate |
| Normal Monitor | $V_{TST}$ | $V_{DD}$ | X | 1 | 0 | 0 | 1 | OFF | disabled | disabled | 9.8304 MHz | 2.4576 MHz | 9600 |
| Forced Monitor | $V_{DD}$ | $V_{DD}$ | $FFFF (blank) | 1 | 0 | X | X | OFF | disabled | disabled | 9.8304 MHz | 2.4576 MHz | 9600 |
| | GND | | | | | | | ON | disabled | disabled | — | Nominal 1.6 MHz | Nominal 6300 |
| User | $V_{DD}$ | $V_{DD}$ | not $FFFF (not blank) | X | X | X | X | ON | enabled | enabled | — | Nominal 1.6 MHz | Nominal 6300 |

Notes

19. PTA0 must have a pull-up resistor to $V_{DD}$ in monitor mode
20. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1
21. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
22. X = don't care
23. $V_{TST}$ is a high voltage $V_{DD} + 3.5\ V \leq V_{TST} \leq V_{DD} + 4.5\ V$

## EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be found on the Freescale web site, www.freescale.com.

### VSUP Pins (VSUP1:VSUP3)

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

### LIN Pin

For DPI (Direct Power Injection) and ESD (Electrostatic Discharge) its recommended to place a high quality ceramic decoupling capacitor near the LIN pin. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

### Voltage Regulator Output Pins (VDD and AGND)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

### MCU digital supply pins (EVDD and EVSS)

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

### MCU analog supply pins (VREFH, VDDA, VREFL, and VSSA)

To avoid noise on the analog supply pins its important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 18 and Figure 19 show the recommendations on schematics and layout level and Table 11 indicates recommended external components and layout considerations.

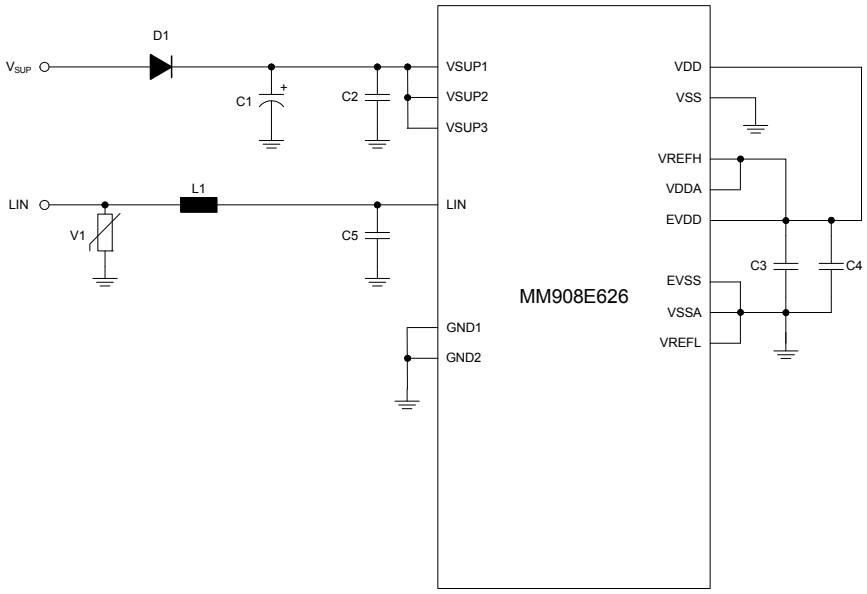



**Figure 18. EMC/EMI Recommendations**

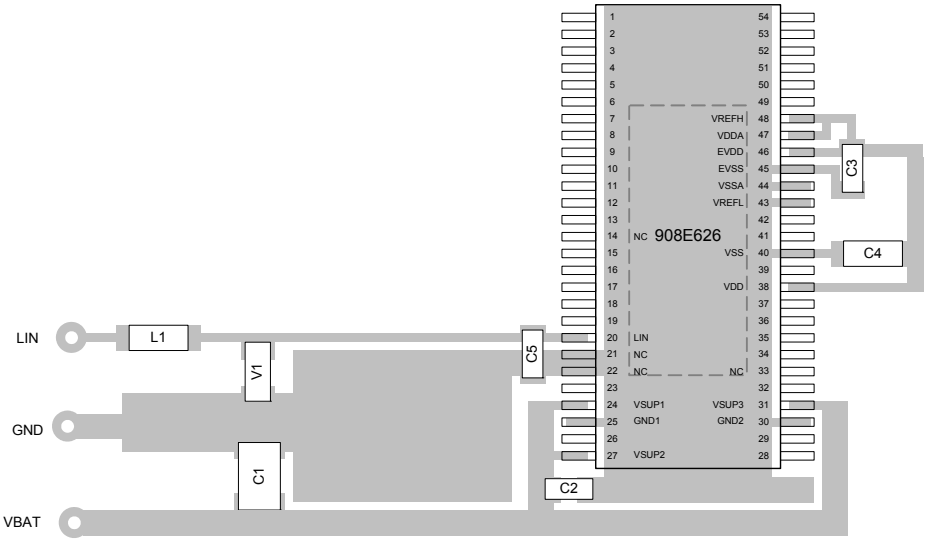



**Figure 19. PCB Layout Recommendations**

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**Table 11. Component Value Recommendation**

| Component | Recommended Value[24] | Comments / Signal Routing |
|---|---|---|
| C1 | Bulk Capacitor | |
| C2 | 100 nF, SMD Ceramic, Low ESR | Close (<5.0 mm) to the VSUP1, VSUP2 pins with good ground return |
| C3 | 100 nF, SMD Ceramic, Low ESR | Close (<3.0 mm) to the digital supply pins (EVDD, EVSS) with good ground return.<br>The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3. |
| C4 | 4,7 µF, SMD Ceramic, Low ESR | Bulk Capacitor |
| C5 | 180 pF, SMD Ceramic, Low ESR | Close (<5.0 mm) to LIN pin.<br>Total Capacitance on LIN has to be below 220 pF.<br>($C_{TOTAL}$ = $C_{LIN-PIN}$ + C5 + $C_{VARISTOR}$ ~ 10 pF + 180 pF + 15 pF) |
| V1[25] | Varistor Type TDK AVR-M1608C270MBAAB | Optional (close to LIN connector) |
| L1[25] | SMD Ferrite Bead Type TDK MMZ2012Y202B | Optional, (close to LIN connector) |

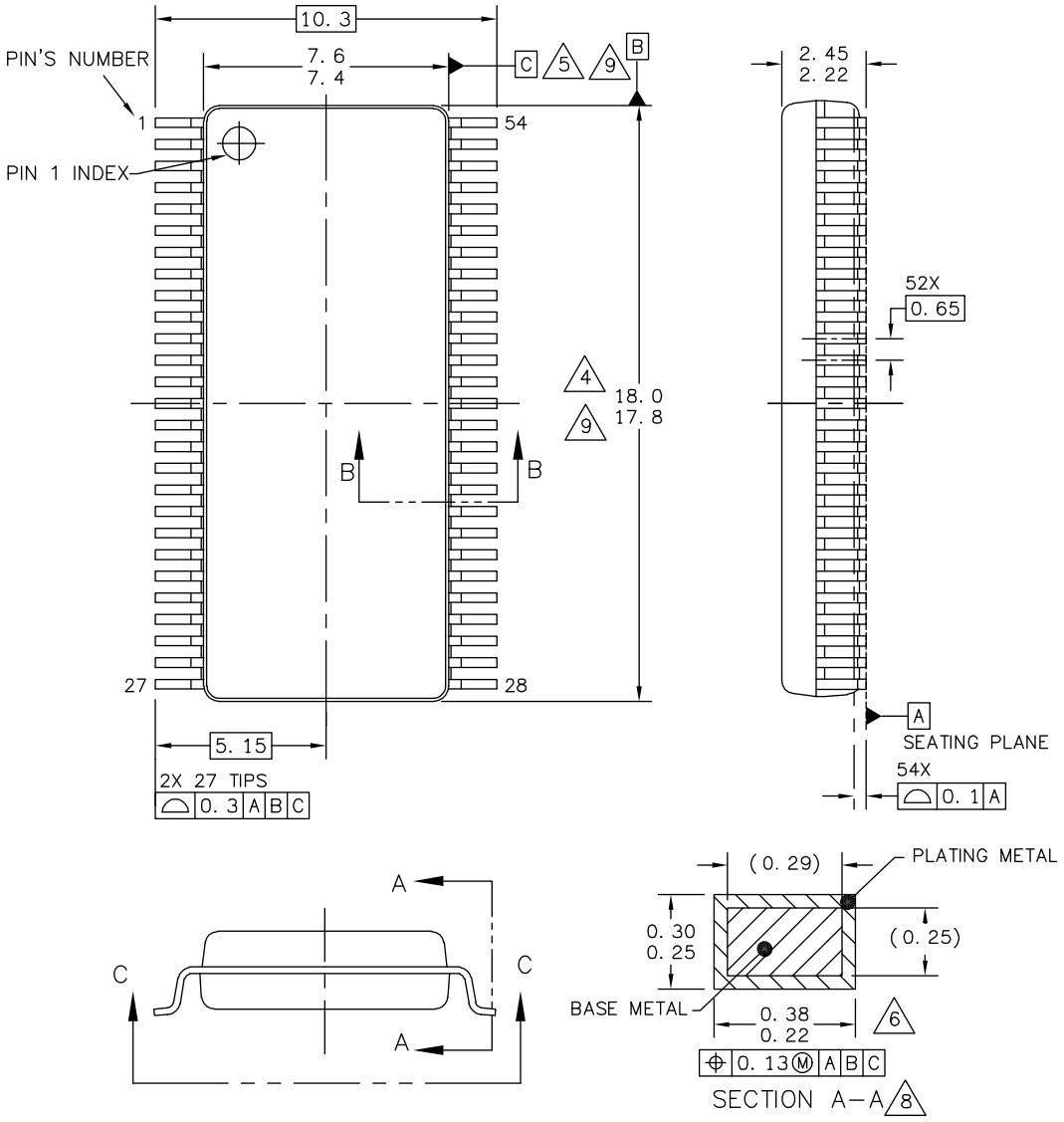
Notes

24. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
25. Components are recommended to improve EMC and ESD performance.

# PACKAGING

## PACKAGING DIMENSIONS

**Important:** For the most current revision of the package, visit www.freescale.com and perform a keyword search on 98ARL10519D. Dimensions shown are provided for reference ONLY.




| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|---|
| TITLE: 54LD SOIC W/B, 0. 65 PITCH 5. 1 X 10. 3 EXPOSED PAD, CASE–OUTLINE | DOCUMENT NO: 98ARL10519D | REV: D |
| | CASE NUMBER: 1400–03 | 02 MAY 2008 |
| | STANDARD: NON–JEDEC | |

EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D

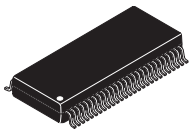
**908E626**

# ADDITIONAL DOCUMENTATION

## *THERMAL ADDENDUM (REV 1.0)*

**908E626**

**54-PIN
SOICW-EP**



**98ARL10519D
54-PIN SOICW-EP**

**Note** For package dimensions, refer to 98ARL10519D.

### Introduction

This thermal addendum ia provided as a supplement to the MM908E626 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

### Package and Thermal Considerations

This MM908E626 is a dual die package. There are two heat sources in the package independently heating with $P_1$ and $P_2$. This results in two junction temperatures, $T_{J1}$ and $T_{J2}$, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with $P_1$.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with $P_2$. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

### Standards

**Table 12. Thermal Performance Comparison**

| Thermal Resistance | 1 = Power Chip, 2 = Logic Chip [°C/W] | | |
|---|---|---|---|
| | ***m*** **= 1,** ***n*** **= 1** | ***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1** | ***m*** **= 2,** ***n*** **= 2** |
| $R_{\theta JAmn}$ (1)(2) | 23 | 20 | 24 |
| $R_{\theta JBmn}$ (2)(3) | 9.0 | 6.0 | 10 |
| $R_{\theta JAmn}$ (1)(4) | 52 | 47 | 52 |
| $R_{\theta JCmn}$ (5) | 1.0 | 0 | 2.0 |

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.

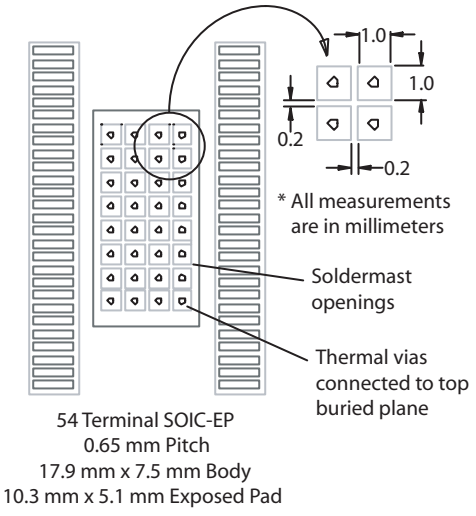
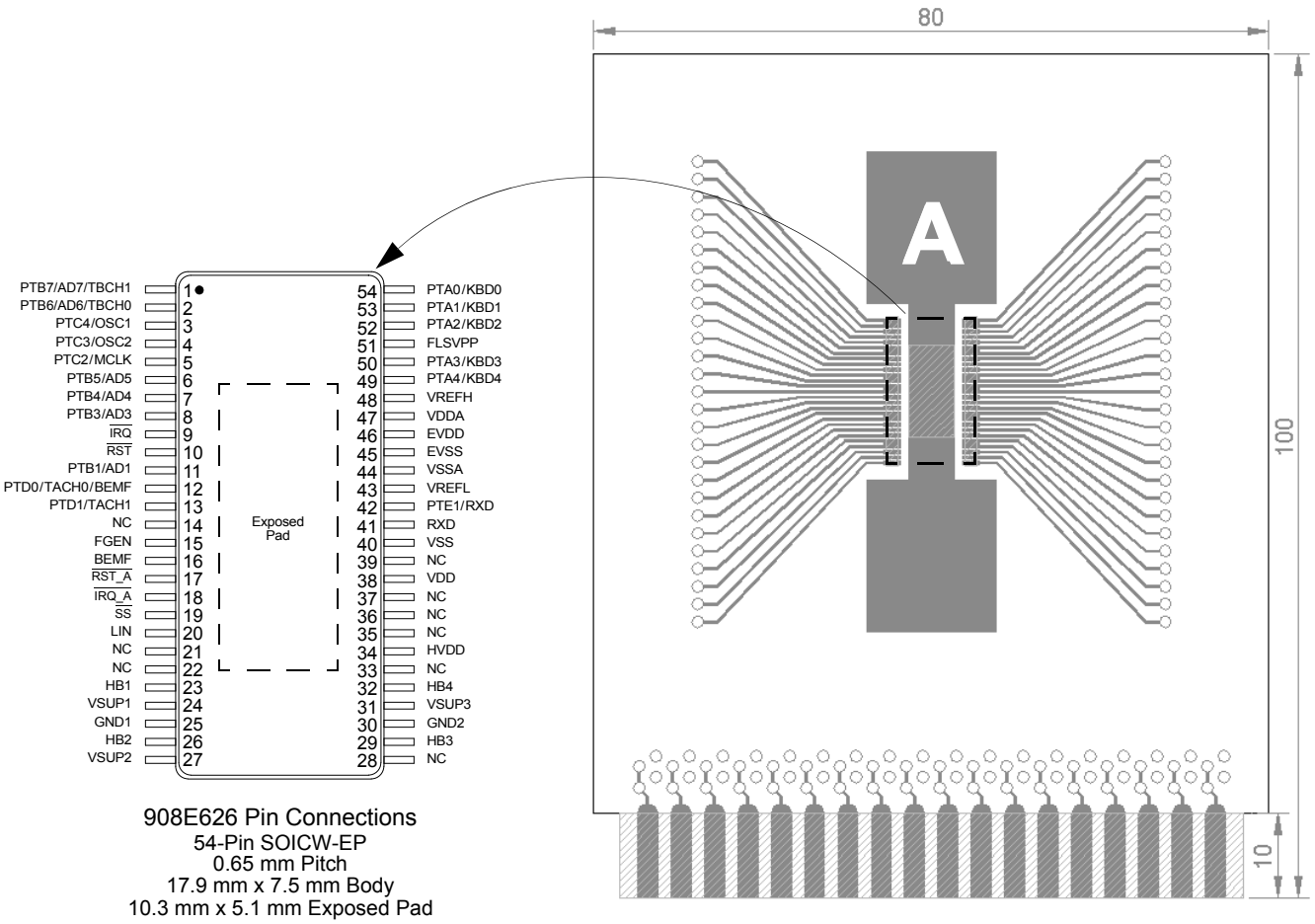



**Figure 20. Thermal Land Pattern for Direct Thermal Attachment Per JEDEC JESD51-5Thermal Test Board**




908E626 Pin Connections
54-Pin SOICW-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

**Figure 21. Thermal Test Board**

### Device on Thermal Test Board

| | |
|---|---|
| Material: | Single layer printed circuit board<br>FR4, 1.6 mm thickness<br>Cu traces, 0.07 mm thickness |
| Outline: | 80 mm x 100 mm board area, including edge connector for thermal testing |
| Area **A**: | Cu heat-spreading areas on board surface |
| Ambient Conditions: | Natural convection, still air |

**Table 13. Thermal Resistance Performance**

| Thermal Resistance | Area A ($mm^2$) | 1 = Power Chip, 2 = Logic Chip (°C/W) | | |
|---|---|---|---|---|
| | | *m* = 1, *n* = 1 | *m* = 1, *n* = 2<br>*m* = 2, *n* = 1 | *m* = 2, *n* = 2 |
| $R_{\theta JAmn}$ | 0 | 53 | 48 | 53 |
| | 300 | 39 | 34 | 38 |
| | 600 | 35 | 30 | 34 |
| $R_{\theta JSmn}$ | 0 | 21 | 16 | 20 |
| | 300 | 15 | 11 | 15 |
| | 600 | 14 | 9.0 | 13 |

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JSmn}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

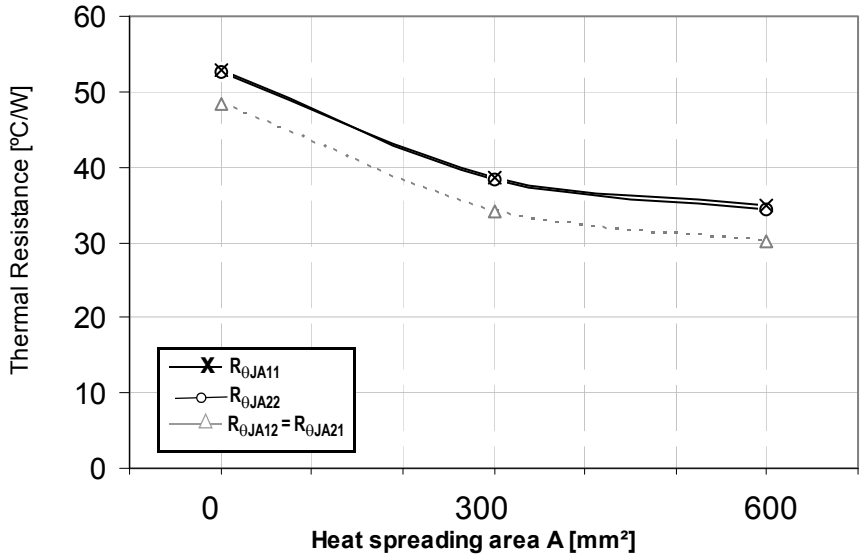



**Figure 22. Device on Thermal Test Board $R_{\theta JA}$**

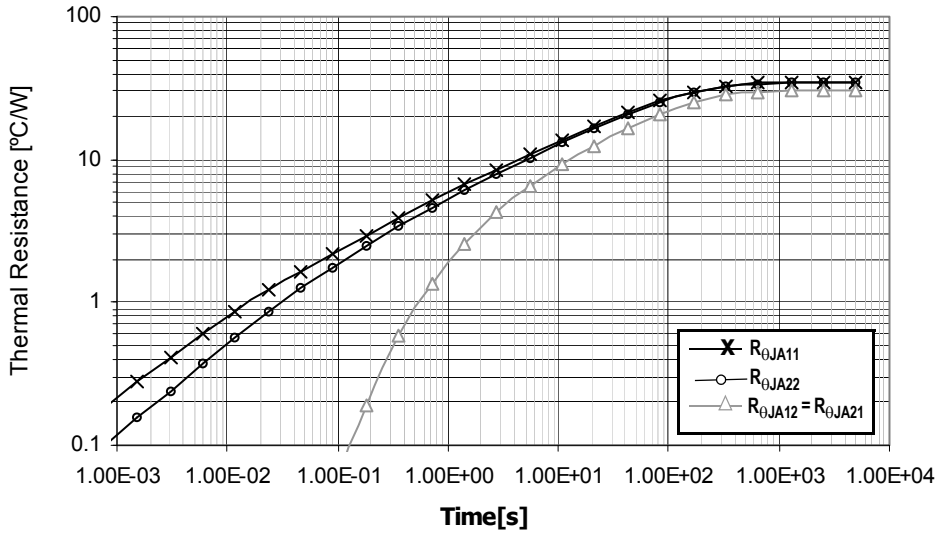



**Figure 23. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)**
**Device on Thermal Test Board Area A = 600 ($mm^2$)**