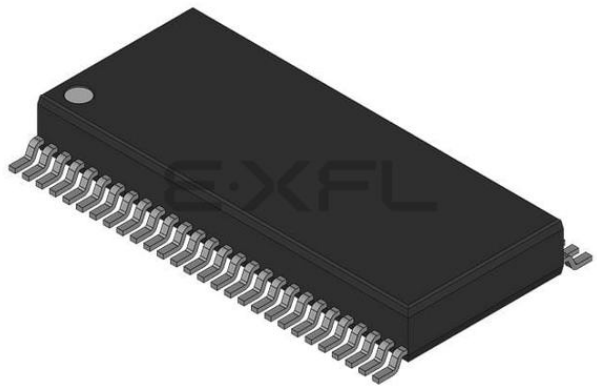

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	13
Voltage - Supply	8V ~ 18V
Operating Temperature	-40°C ~ 115°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mm908e626avek

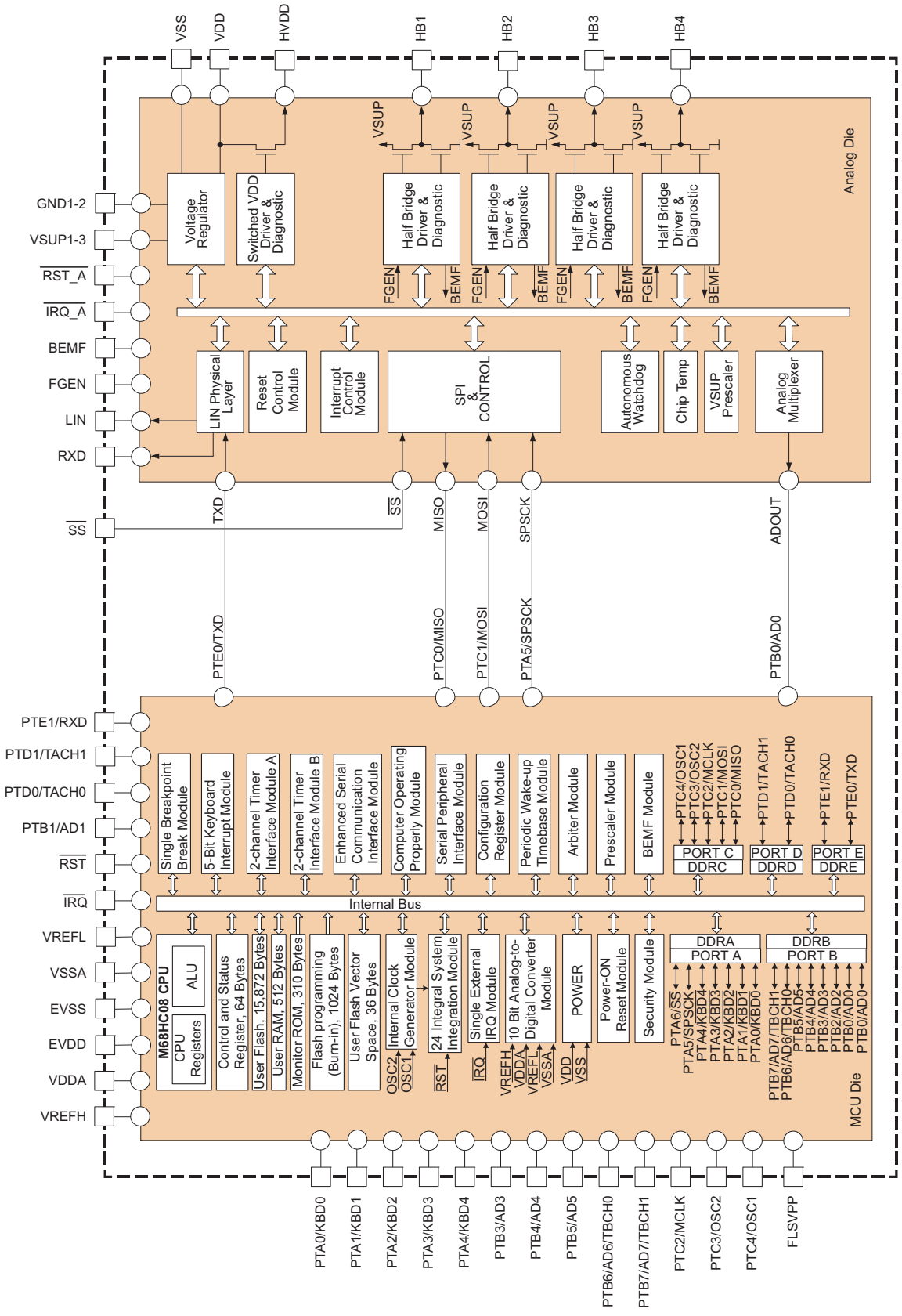


Figure 2. 908E626 Simplified Internal Block Diagram

PIN CONNECTIONS

Transparent Top View of Package

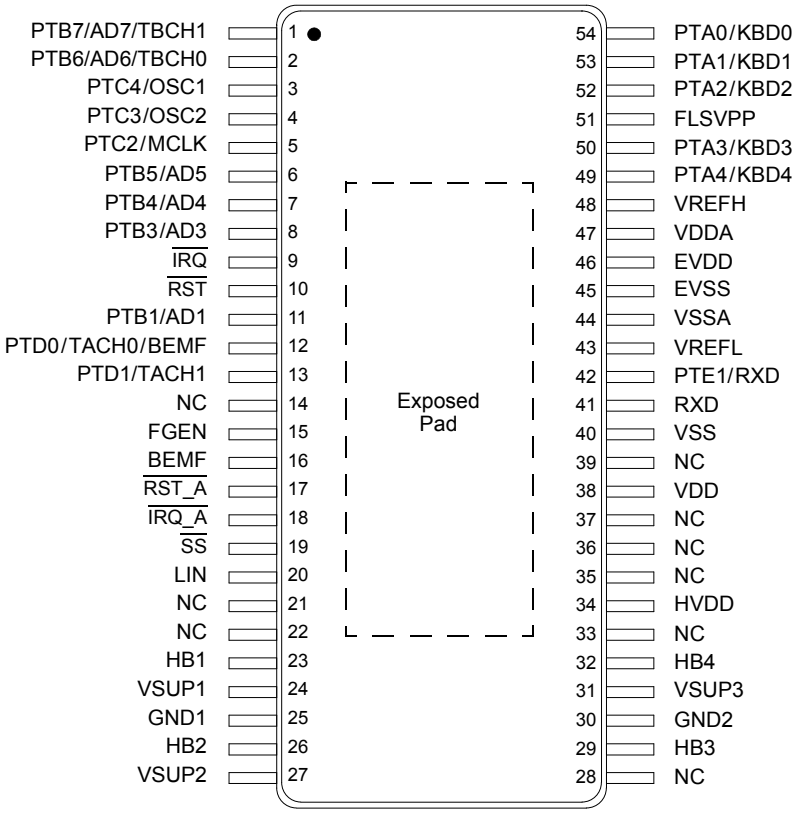


Figure 3. 908E626 Pin Connections

Table 1. 908E626 PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin Description section beginning on page 15.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	9	IRQ	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	10	RST	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0/BEMF PTD1/TACH1	Port D I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage			V
Analog Chip Supply Voltage under Normal Operation (Steady-state)	$V_{SUP(SS)}$	-0.3 to 28	
Analog Chip Supply Voltage under Transient Conditions (1)	$V_{SUP(PK)}$	-0.3 to 40	
Microcontroller Chip Supply Voltage	V_{DD}	-0.3 to 6.0	
Input Pin Voltage			V
Analog Chip	$V_{IN(ANALOG)}$	-0.3 to 5.5	
Microcontroller Chip	$V_{IN(MCU)}$	V_{SS}-0.3 to V_{DD}+0.3	
Maximum Microcontroller Current per Pin			mA
All Pins Except VDD, VSS, PTA0:PTA6, PTC0:PTC1	$I_{PIN(1)}$	±15	
Pins PTA0:PTA6, PTC0:PTC1	$I_{PIN(2)}$	±25	
Maximum Microcontroller V_{SS} Output Current	I_{MVSS}	100	mA
Maximum Microcontroller V_{DD} Input Current	I_{MVDD}	100	mA
LIN Supply Voltage			V
Normal Operation (Steady-state)	$V_{BUS(SS)}$	-18 to 28	
Transient Conditions (1)	$V_{BUS(DYNAMIC)}$	40	
ESD Voltage			V
Human Body Model (2)	V_{ESD1}	±3000	
Machine Model (3)	V_{ESD2}	±150	
Charge Device Model (4)	V_{ESD3}	±500	

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. ESD3 testing is performed in accordance with Charge Device Model, robotic (C_{ZAP} = 4.0 pF).

STATIC ELECTRICAL CHARACTERISTICS

Table 3. STATIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Nominal Operating Voltage	V_{SUP}	8.0	–	18	V
SUPPLY CURRENT					
NORMAL Mode V_{SUP} = 12 V, Power Die ON (PSON=1), MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	–	20	–	mA
STOP Mode (9) V_{SUP} = 12 V, Cyclic Wake-up Disabled	I_{STOP}	–	–	75	µA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Pins $\overline{RST\_A}$, $\overline{IRQ\_A}$					V
Low State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High State Output Voltage (I_{OUT} = 1.0 µA)	V_{OH}	3.85	–	–	
Output Pins BEMF, RXD					V
Low State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High State Output Voltage (I_{OUT} = 1.5 mA)	V_{OH}	3.85	–	–	
Output Pin RXD– Capacitance (10)	C_{IN}	–	4.0	–	pF
Input Pins $\overline{RST\_A}$, FGEN, $\overline{SS}$					V
Input Logic Low Voltage	V_{IL}	–	–	1.5	
Input Logic High Voltage	V_{IH}	3.5	–	–	
Input Pins $\overline{RST\_A}$, FGEN, $\overline{SS}$–Capacitance (10)	C_{IN}	–	4.0	–	pF
Pins $\overline{RST\_A}$, $\overline{IRQ\_A}$–Pull-up Resistor	$R_{PULLUP1}$	–	10	–	kΩ
Pin $\overline{SS}$–Pull-up Resistor	$R_{PULLUP2}$	–	60	–	kΩ
Pins FGEN, MOSI, SPSCK–Pull-down Resistor	$R_{PULLDOWN}$	–	60	–	kΩ
Pin TXD–Pull-up Current Source	I_{PULLUP}	–	35	–	µA

Notes

9. STOP mode current will increase if V_{SUP} exceeds 15 V.
10. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Output Low Level TXD LOW, 500 Ω Pull-up to V_{SUP}	$V_{LIN-LOW}$	–	–	1.4	V
Output High Level TXD HIGH, I_{OUT} = 1.0 µA	$V_{LIN-HIGH}$	V_{SUP}-1.0	–	–	V
Pull-up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Leakage Current to GND Recessive State (-0.5 V < V_{LIN} < V_{SUP})	$I_{BUS\_PAS\_REC}$	0.0	–	20	µA
Leakage Current to GND (V_{SUP} Disconnected) Including Internal Pull-up Resistor, V_{LIN} @ -18 V Including Internal Pull-up Resistor, V_{LIN} @ +18 V	 $I_{BUS\_NO\_GND}$ I_{BUS}	 – –	 -600 25	 – –	µA
LIN Receiver Recessive Dominant Threshold Input Hysteresis	 V_{IH} V_{IL} V_{ITH} V_{IHY}	 0.6V_{LIN} 0 – 0.01V_{SUP}	 – – V_{SUP}/2 –	 V_{SUP} 0.4V_{LIN} – 0.1V_{SUP}	V
LIN Wake-up Threshold	V_{WTH}	–	V_{SUP}/2	–	V
HALF-BRIDGE OUTPUTS (HB1:HB4)					
Switch ON Resistance @ T_J = 25 °C with I_{LOAD} = 1.0 A High Side Low Side	 $R_{DS(ON)HB\_HS}$ $R_{DS(ON)HB\_LS}$	 – –	 425 400	 500 500	mΩ
High Side Overcurrent Shutdown	I_{HBHSOC}	3.0	–	7.5	A
Low Side Overcurrent Shutdown	I_{HBLSOC}	2.5	–	7.5	A
Low Side Current Limitation @ T_J = 25 °C Current Limit 1 (CLS2 = 0, CLS1 = 1, CLS0 = 1) Current Limit 2 (CLS2 = 1, CLS1 = 0, CLS0 = 0) Current Limit 3 (CLS2 = 1, CLS1 = 0, CLS0 = 1) Current Limit 4 (CLS2 = 1, CLS1 = 1, CLS0 = 0) Current Limit 5 (CLS2 = 1, CLS1 = 1, CLS0 = 1)	 I_{CL1} I_{CL2} I_{CL3} I_{CL4} I_{CL5}	 – 210 300 450 600	 55 260 370 550 740	 – 315 440 650 880	mA
Half-bridge Output HIGH Threshold for BEMF Detection	V_{BEMFH}	–	-30	0.0	V
Half-bridge Output LOW Threshold for BEMF Detection	V_{BEMFL}	–	-60	-5.0	mV
Hysteresis for BEMF Detection	V_{BEMFHY}	–	30	–	mV
Low Side Current-to-Voltage Ratio (V_{ADOUT} [V]/I_{HB} [A]) CSA = 1 CSA = 0	 $RATIO_H$ $RATIO_L$	 7.0 1.0	 12.0 2.0	 14.0 3.0	V/A

Table 5. MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
ADC	10 Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud Rate Adjustment
ICG	Internal Clock Generation Module
BEMF Counter	Special Counter for *SMARTMOS* BEMF Output

TIMING DIAGRAMS

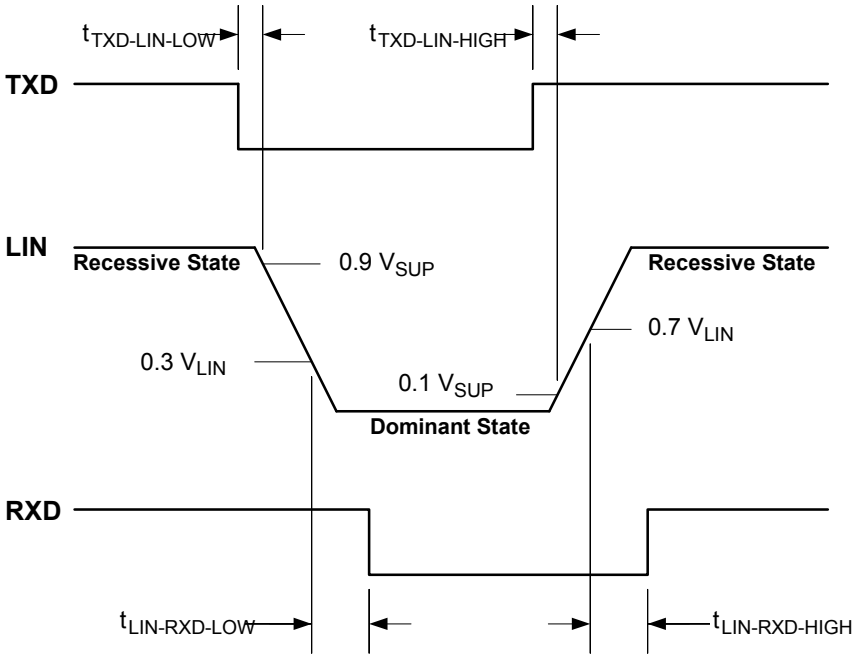


Figure 4. LIN Timing Description

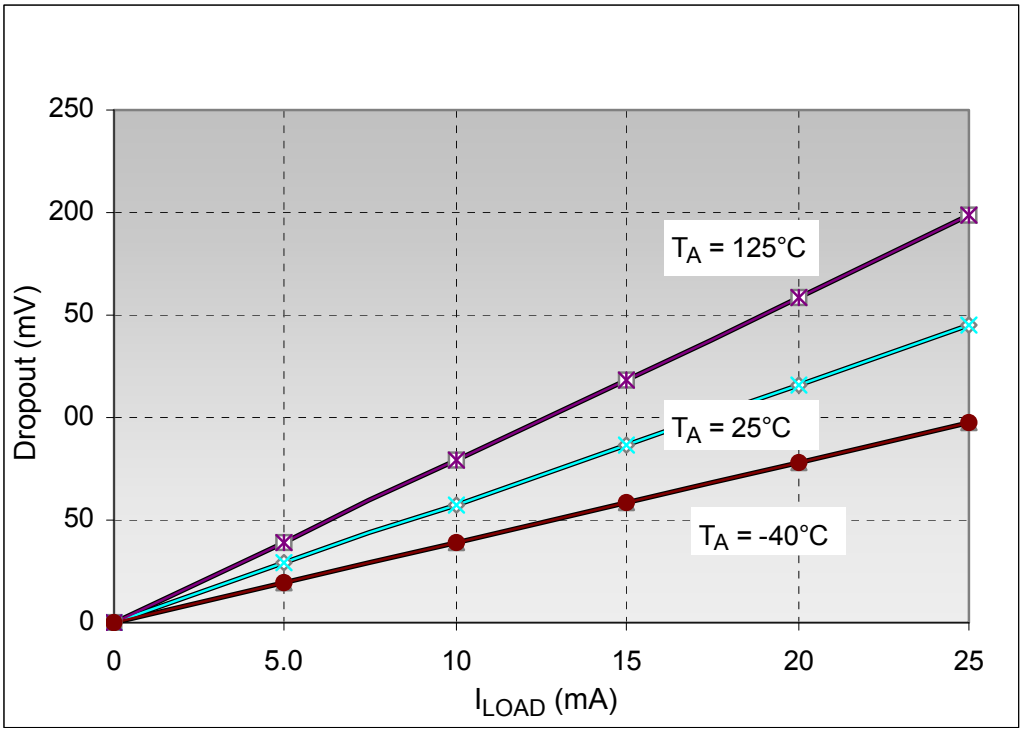


Figure 7. Dropout Voltage on HVDD

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E626 device was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E626 is well suited to perform stepper motor control, e.g. for climate or light-levelling control via a 3-wire LIN bus.

This device combines an standard HC08 MCU core (68HC908EY16) with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as four half-bridge outputs. Other ports are also provided including a selectable HVDD pin. An internal voltage regulator is provided on the *SMARTMOS* IC chip, which provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables the device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and the third for ground.

FUNCTIONAL PIN DESCRIPTION

See Figures 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on Figures 3 for a depiction of the pin locations on the package.

PORT A I/O PINS (PTA0:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins, KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die. The PTA6/$\overline{SS}$ pin is likewise not accessible.

For details refer to the 68HC908EY16 datasheet.

PORT B I/O PINS (PTB1, PTB3:7)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module. The PTB6:PTB7 pins are also shared with the Timer B module.

PTB0/AD0 is internally connected to the ADOUT pin of the analog die, allowing diagnostic measurements to be calculated; e.g., current recopy, V_{SUP}, etc. The PTB2/AD2 pin is not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

PORT C I/O PINS (PTC2:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT D I/O PINS (PTD0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special function, bidirectional I/O port pins that can also be programmed to be timer pins.

In step motor applications, the PTD0 pin should be connected to the BEMF output of the analog die, to evaluate the BEMF signal with a special BEMF module of the MCU.

PTD1 pin is recommended for use as an output pin for generating the FGEN signal (PWM signal), if required by the application.

PORT E I/O PIN (PTE1)

PTE1/RXD and PTE0/TXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die.The connection for the receiver must be done externally.

EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

EXTERNAL RESET PIN ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should be either left open (not connected) or connected to GND.

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

INTERRUPTS

The 908E626 has six different interrupt sources as described in the following paragraphs. The interrupts can be disabled or enabled via the SPI. After reset all interrupts are automatically disabled.

LOW VOLTAGE INTERRUPT

The Low Voltage Interrupt (LVI) is related to the external supply voltage, V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVI flag. If the Low Voltage Interrupt is enabled, an interrupt will be initiated.

With LVI the H-Bridges (high side MOSFET only) are switched off. All other modules are not influenced by this interrupt.

During STOP mode the LVI circuitry is disabled.

HIGH VOLTAGE INTERRUPT

The High Voltage Interrupt (HVI) is related to the external supply voltage, V_{SUP}. If this voltage rises above the HVI threshold, it will set the HVI flag. If the High Voltage Interrupt is enabled, an interrupt will be initiated.

With HVI the H-Bridges (high side MOSFET only) are switched off. All other modules are not influenced by this interrupt.

During STOP mode the HVI circuitry is disabled.

HIGH TEMPERATURE INTERRUPT

The High Temperature Interrupt (HTI) is generated by the on-chip temperature sensors. If the chip temperature is above the HTI threshold, the HTI flag will be set. If the High Temperature Interrupt is enabled, an interrupt will be initiated.

During STOP mode the HTI circuitry is disabled.

AUTONOMOUS WATCHDOG INTERRUPT (AWD)

Refer to Autonomous Watchdog (AWD) on page 30.

LIN INTERRUPT

If the LINIE bit is set, a falling edge on the LIN pin will generate an interrupt. During STOP mode this interrupt will initiate a system wake-up.

OVERCURRENT INTERRUPT

If an overcurrent condition on a half-bridge or the HVDD output is detected and the OCIE bit is set and an interrupt generated.

SYSTEM WAKE-UP

System wake-up can be initiated by any of four events:

- A falling edge on the LIN pin
- A wake-up signal from the AWD
- An LVR condition

If one of these wake-up events occurs and the interrupt mask bit for this event is set, the interrupt will wake-up the microcontroller as well as the main voltage regulator (MREG) Figures 8.

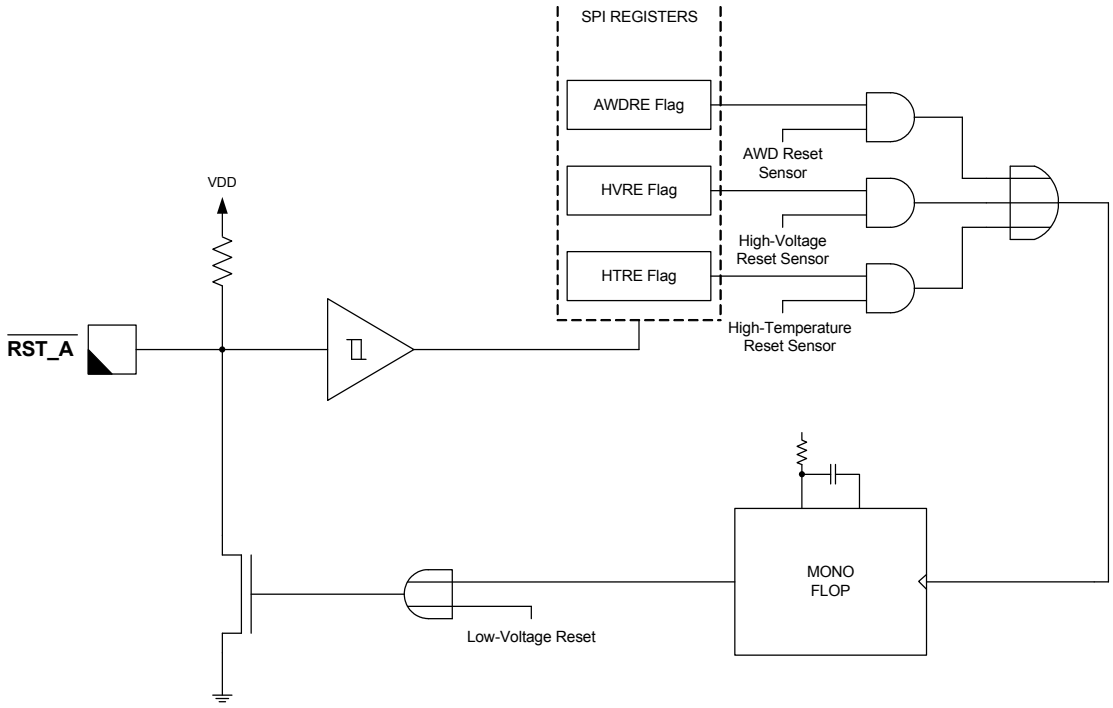


Figure 10. Internal Reset Routing

RESET INTERNAL SOURCES

Autonomous Watchdog

AWD modules generates a reset because of a timeout (watchdog function).

High Temperature Reset

To prevent damage to the device, a reset will be initiated if the temperature rises above a certain value. The reset is maskable with bit HTRE in the Reset Mask Register. After a reset the high temperature reset is disabled.

Low Voltage Reset

The LVR is related to the internal V_{DD}. In case the voltage falls below a certain threshold, it will pull down the $\overline{RST\_A}$ pin.

High Voltage Reset

The HVR is related to the external V_{SUP} voltage. In case the voltage is above a certain threshold, it will pull down the $\overline{RST\_A}$ pin. The reset is maskable with bit HVRE in the Reset Mask Register. After a reset the high voltage reset is disabled.

RESET EXTERNAL SOURCE

External Reset Pin

The microcontroller has the capability of resetting the *SMARTMOS* device by pulling down the $\overline{RST}$ pin.

Reset Mask Register (RMR)

Register Name and Address: RMR - $06

	Bit7	6	5	4	3	2	1	Bit0
Read	TTEST	0	0	0	0	0	HVRE	HTRE
Write								
Reset	0	0	0	0	0	0	0	0

TTEST—High Temperature Reset Test

This read/write bit is for test purposes only. It decreases the overtemperature shutdown limit for final test. Reset clears the HTRE bit.

- 1 = Low temperature threshold enabled.
- 0 = Low temperature threshold disabled.

HVRE—High Voltage Reset Enable Bit

This read/write bit enables resets on high voltage conditions. Reset clears the HVRE bit.

- 1 = High voltage reset enabled.
- 0 = High voltage reset disabled.

HTRE—High Temperature Reset Enable Bit

This read/write bit enables resets on high temperature conditions. Reset clears the HTRE bit.

- 1 = High temperature reset enabled.
- 0 = High temperature reset disabled.

SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) creates the communication link between the microcontroller and the 908E626.

The interface consists of four pins (see Figure 11):

- $\overline{SS}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock (maximum frequency 4.0 MHz)

A complete data transfer via the SPI consists of 2 bytes. The master sends address and data, slave system status, and data of the selected address.

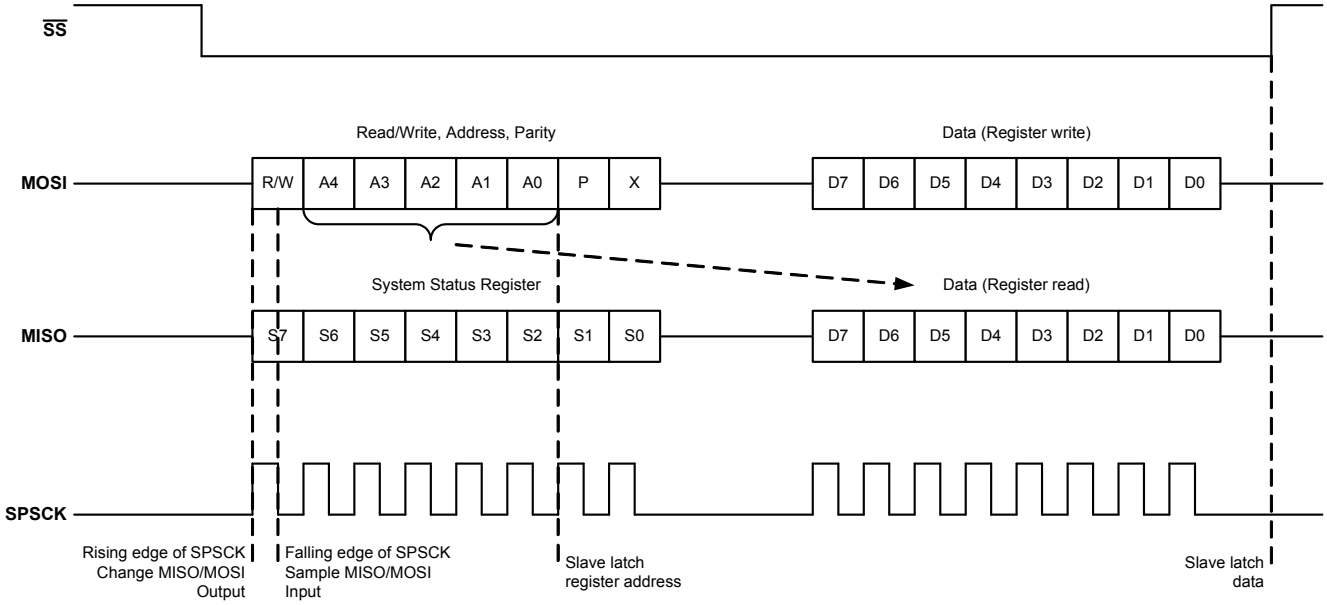


Figure 11. SPI Protocol

During the inactive phase of $\overline{SS}$, the new data transfer is prepared. The falling edge on the $\overline{SS}$ line indicates the start of a new data transfer and puts MISO in the low-impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.

The MISO output changes data on a rising edge of SPSCK. The MOSI input is sampled on a falling edge of SPSCK. The data transfer is only valid if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.

After a write operation, the transmitted data is latched into the register by the rising edge of $\overline{SS}$. Register read data is internally latched into the SPI at the time when the parity bit is transferred. $\overline{SS}$ HIGH forces MISO to high-impedance.

MASTER ADDRESS BYTE

A4:A0

Contains the address of the desired register.

R/$\overline{W}$

Contains information about a read or a write operation.

- If R/$\overline{W}$ = 1, the second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0, the master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SMARTMOS* register on rising edge of $\overline{SS}$.

Parity P

The parity bit is equal to “0” if the number of 1 bits is an even number contained within R/$\overline{W}$, A4:A0. If the number of 1 bits is odd, P equals “1”. For example, if R/$\overline{W}$ = 1, A4:A0 = 00001, then P equals “0.”

The parity bit is only evaluated during a write operation.

Bit X

Not used.

Master Data Byte

Contains data to be written or no valid data during a read operation.

Offset Chopping

If bit OFC_EN in the H-bridge Control Register (HBCTL) is set, HB1 and HB2 will continue to switch on the low side MOSFETs with the rising edge of the FGEN signal and HB3 and HB4 will switch on the low side MOSFETs with the falling edge on the FGEN input. In step motor applications, this feature allows the reduction of EMI due to a reduction of the di/dt (Figure 14).

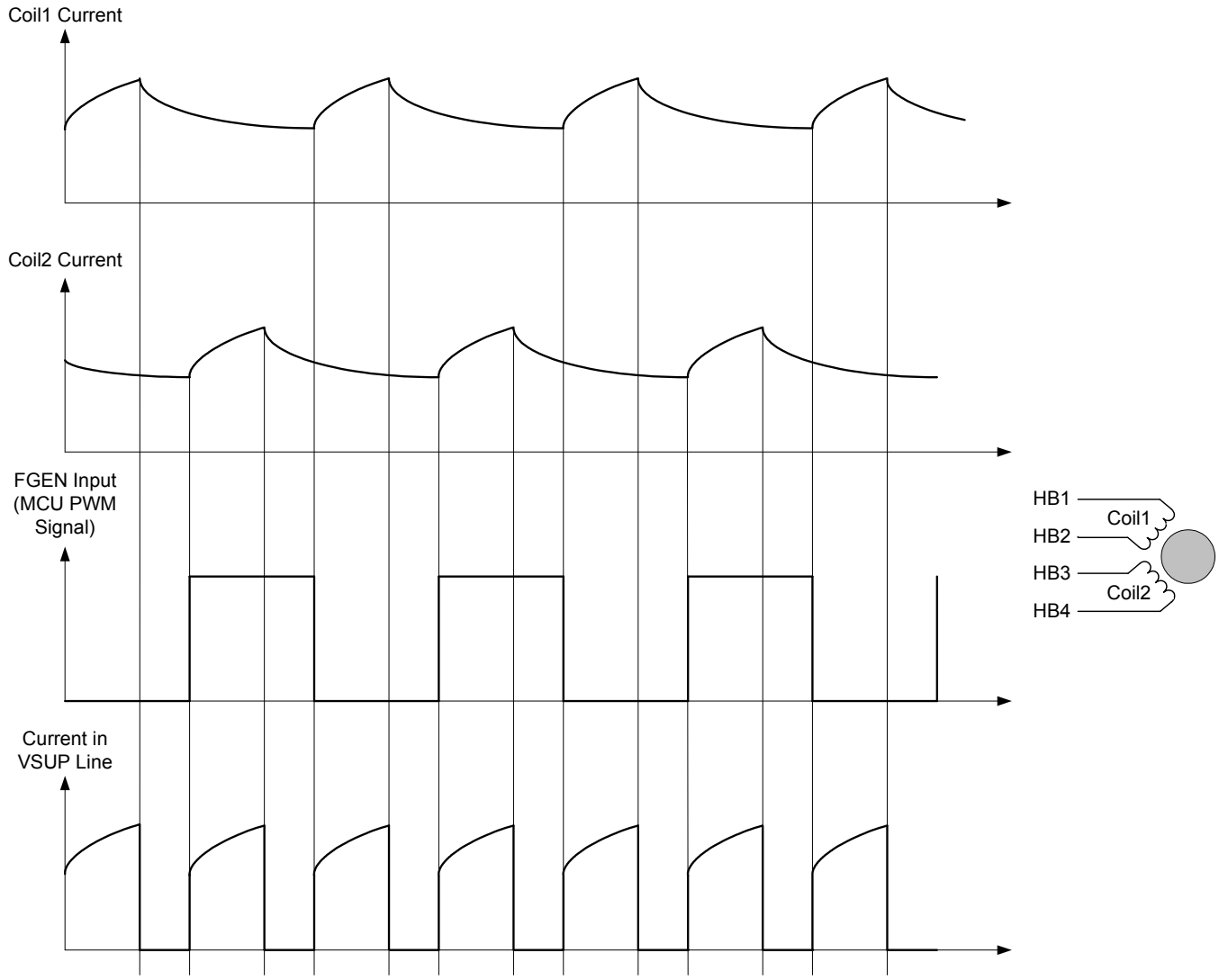


Figure 14. Offset Chopping for Step Motor Control

HALF-BRIDGE CURRENT RECOPY

Each low side MOSFET has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the analog multiplexer.

The factor for the current sense amplification can be selected via bit CSA in the System Control Register.

- CSA = 1: Low resolution selected (500 mA measurement range).
- CSA = 0: High resolution selected (2.5 A measurement range).

HALF-BRIDGE BEMF GENERATION

The BEMF output is set to “1” if a recirculation current is detected in any half-bridge. This recirculation current flows via the two freewheeling diodes of the power MOSFETs. The BEMF circuitry detects that and generates a HIGH on the BEMF output as long as a recirculation current is detected. This signal provides a flexible and reliable detection of stall in step motor applications. For this the BEMF circuitry takes advantage of the instability of the electrical and mechanical behavior of a step motor when blocked. In addition the signal can be used for open load detection (absence of this signal) (see Figure 15).

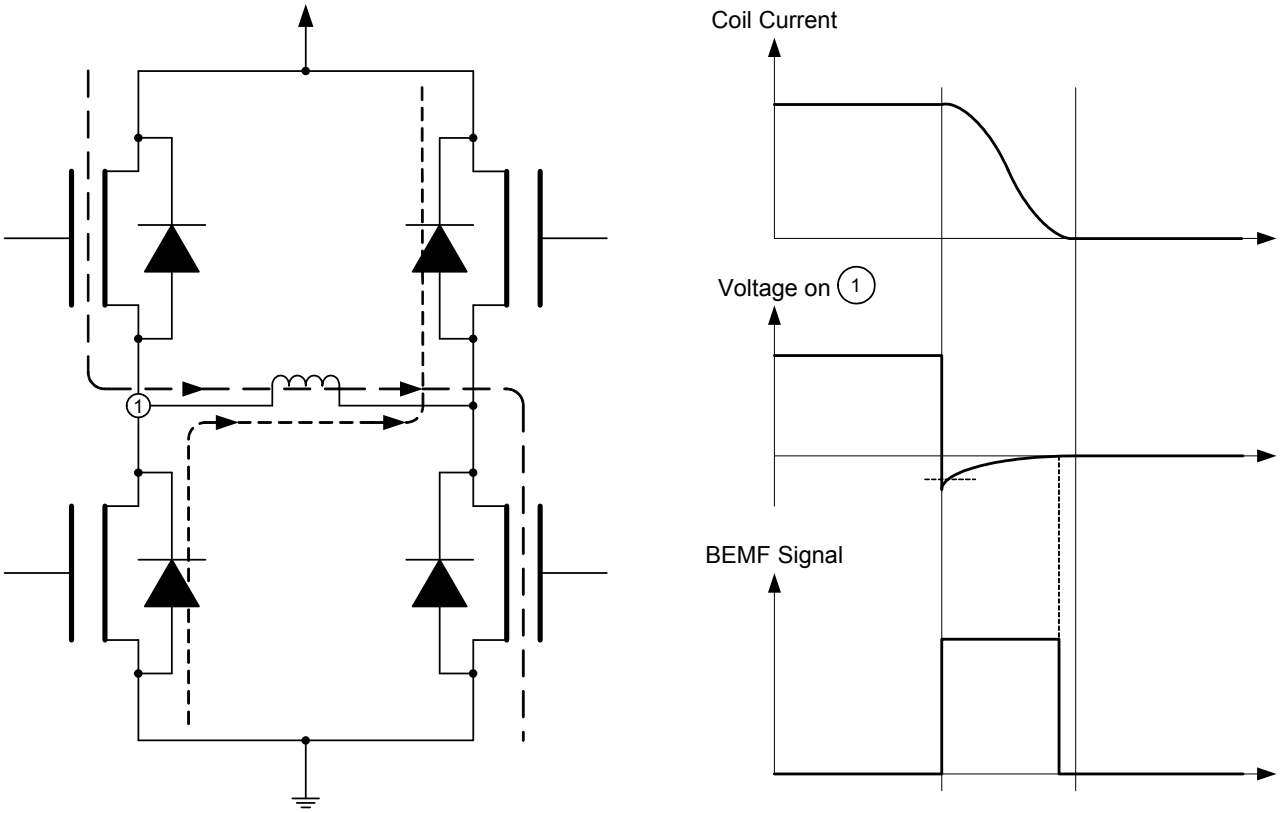


Figure 15. BEMF Signal Generation

HALF-BRIDGE OVERTEMPERATURE PROTECTION

The half-bridge outputs provide an overtemperature prewarning with the HTF in the Interrupt Flag Register (IFR). In order to protect the outputs against overtemperature, the High Temperature Reset must be enabled. If this value is reached, the part generates a reset and disables all power outputs.

HALF-BRIDGE OVERCURRENT PROTECTION

The half-bridges are protected against short to GND, short to VSUP, and load shorts.

In the event an overcurrent on the high side is detected, the high side MOSFETs on all HB high side MOSFETs are switched off automatically. In the event an overcurrent on the low side is detected, all HB low side MOSFETs are switched off automatically. In both cases, the overcurrent status flag HB_OCF in the System Status Register (SYSSTAT) is set.

The overcurrent status flag is cleared (and the outputs re-enabled) by writing a logic [1] to the HB_OCF flag in the System Status Register or by reset.

HALF-BRIDGE OVERVOLTAGE/UNDERVOLTAGE

The half-bridge outputs are protected against undervoltage and overvoltage conditions. This protection is done by the low and high voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the outputs are automatically disabled.

The overvoltage/undervoltage status flags are cleared (and the outputs re-enabled) by writing a logic [1] to the LVF/HVF flags in the Interrupt Flag Register or by reset. Clearing this flag is useless as long as a high or low voltage condition is present.

Half-bridge Control Register (HBCTL)

Register Name and Address: HBCTL - $02

	Bit7	6	5	4	3	2	1	Bit0
Read	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
Write								
Reset	0	0	0	0	0	0	0	0

OFC_EN—H-bridge Offset Chopping Enable Bit

This read/write bit enables offset chopping. Reset clears the OFC_EN bit.

- 1 = Offset chopping enabled.
- 0 = Offset chopping disabled.

CSA—H-bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-bridges. Reset clears the CSA bit.

- 1 = Current sense amplification set for measuring 0.5 A.
- 0 = Current sense amplification set for measuring 2.5 A.

CLS2:CLS0—H-Bridge Current Limitation Selection Bits

These read/write bits select the current limitation value according to Table 8. Reset clears the CLS2:CLS0 bits.

Table 8. H-Bridge Current Limitation Value Selection Bits

CLS2	CLS1	CLS0	Current Limit
0	0	0	No Limit
0	0	1	
0	1	0	
0	1	1	55 mA (typ)
1	0	0	260 mA (typ)
1	0	1	370 mA (typ)
1	1	0	550 mA (typ)
1	1	1	740 mA (typ)

Switchable VDD Outputs

The HVDD pin is a switchable VDD output pin. It can be used for driving external circuitry that requires a V_{DD} voltage. The output is enabled with bit PSON in the System Control Register and can be switched on/off with bit HVDDON in the Power Output Register. Low or high voltage conditions (LVI/HVI) have no influence on this circuitry.

HVDD Overtemperature Protection

Overtemperature protection is enabled if the high temperature reset is enabled.

HVDD Overcurrent Protection

The HVDD output is protected against overcurrent. In the event the overcurrent limit is or was reached, the output automatically switches off and the HVDD overcurrent flag in the System Status Register is set.

System Control Register (SYSCTL)

Register Name and Address: SYSCTL - $03

	Bit7	6	5	4	3	2	1	Bit0
Read	PSON	SRS1	SRS0	0	0	0	0	0
Write								GS
Reset	0	0	0	0	0	0	0	0

PSON—Power Stages On Bit

This read/write bit enables the power stages (half-bridges, LIN transmitter and HVDD output). Reset clears the PSON bit.

- 1 = Power stages enabled.
- 0 = Power stages disabled.

SRS0:SRS1—LIN Slew Rate Selection Bits

These read/write bits enable the user to select the appropriate LIN slew rate for different baud rate configurations as shown in Table 9.

The high speed slew rates are used, for example, for programming via the LIN and are not intended for use in the application.

Table 9. LIN Slew Rate Selection Bits

SRS1	SRS0	LIN Slew Rate
0	0	Initial Slew Rate (20 kBaud)
0	1	Slow Slew Rate (10 kBaud)
1	0	High Speed II (8x)
1	1	High Speed I (4x)

Go to STOP Mode Bit (GS)

This write-only bit instructs the 908E626 to power down and go into STOP mode. Reset or CPU interrupt requests clear the GS bit.

- 1 = Power down and go into STOP mode
- 0 = Not in STOP mode

System Status Register (SYSSTAT)

Register Name and Address: SYSSTAT - $0c

	Bit7	6	5	4	3	2	1	Bit0
Read	0	LINCL	HVDD_OCF	0	LVF	HVF	$\overline{HB\_OCF}$	HTF
Write								
Reset	0	0	0	0	0	0	0	0

LINCL — LIN Current Limitation Bit

This read-only bit is set if the LIN transmitter operates in current limitation region. Due to excessive power dissipation in the transmitter, software is advised to turn the transmitter off immediately.

- 1 = Transmitter operating in current limitation region.
- 0 = Transmitter not operating in current limitation region.

HVDD_OCF—HVDD Output Overcurrent Flag Bit

This read/write flag is set on an overcurrent condition at the HVDD pin. Clear HVDD_OCF and enable the output by writing a logic [1] to the HVDD_OCF Flag. Reset clears the

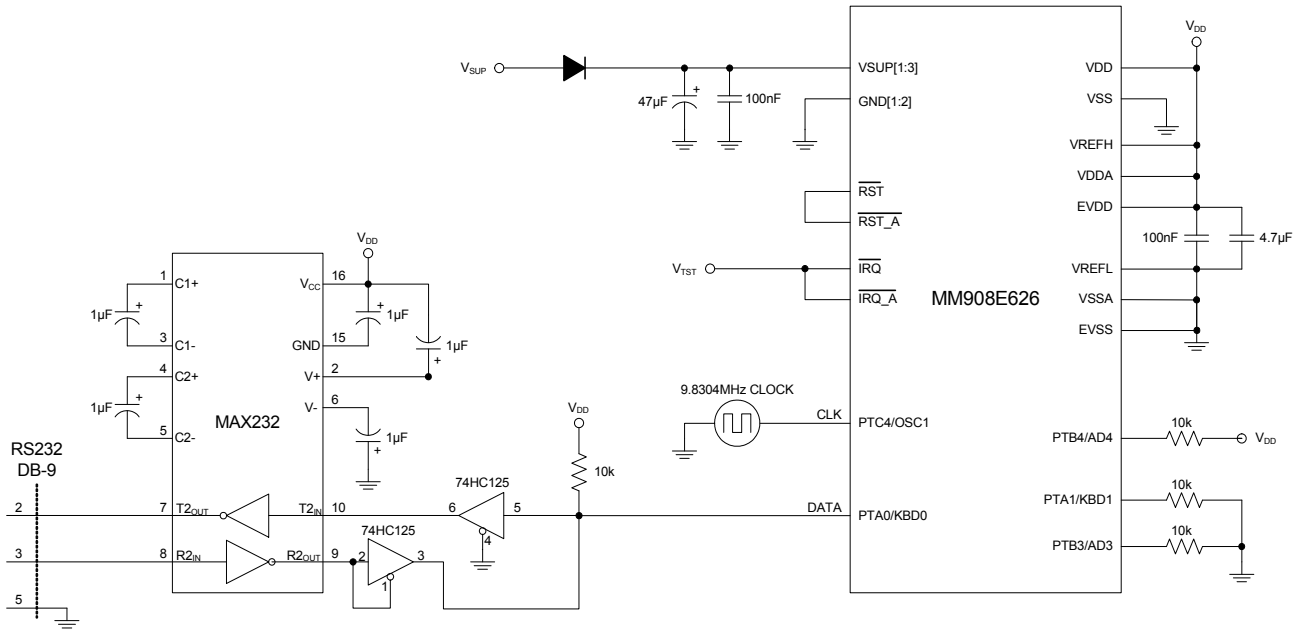


Figure 17. Normal Monitor Mode Circuit

Table 10 summarizes the possible configurations and the necessary setups.

Table 10. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Timeout	Communication Speed		
				PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND							ON	disabled	disabled	—	Nominal 1.6 MHz	Nominal 6300
User	V_{DD}	V_{DD}	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6 MHz	Nominal 6300

Notes

19. PTA0 must have a pull-up resistor to V_{DD} in monitor mode
20. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1
21. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
22. X = don't care
23. V_{TST} is a high voltage $V_{DD} + 3.5\ V \leq V_{TST} \leq V_{DD} + 4.5\ V$

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be found on the Freescale web site, www.freescale.com.

VSUP Pins (VSUP1:VSUP3)

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

LIN Pin

For DPI (Direct Power Injection) and ESD (Electrostatic Discharge) its recommended to place a high quality ceramic decoupling capacitor near the LIN pin. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage Regulator Output Pins (VDD and AGND)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU digital supply pins (EVDD and EVSS)

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

MCU analog supply pins (VREFH, VDDA, VREFL, and VSSA)

To avoid noise on the analog supply pins its important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 18 and Figure 19 show the recommendations on schematics and layout level and Table 11 indicates recommended external components and layout considerations.

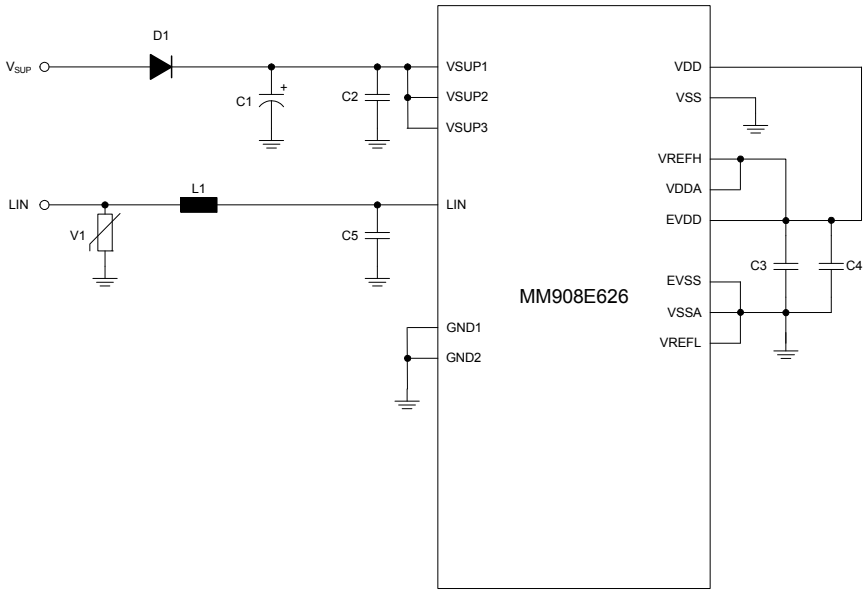
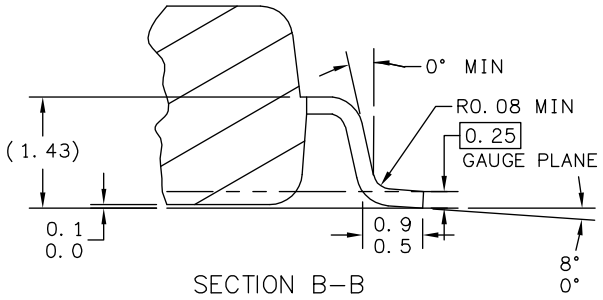
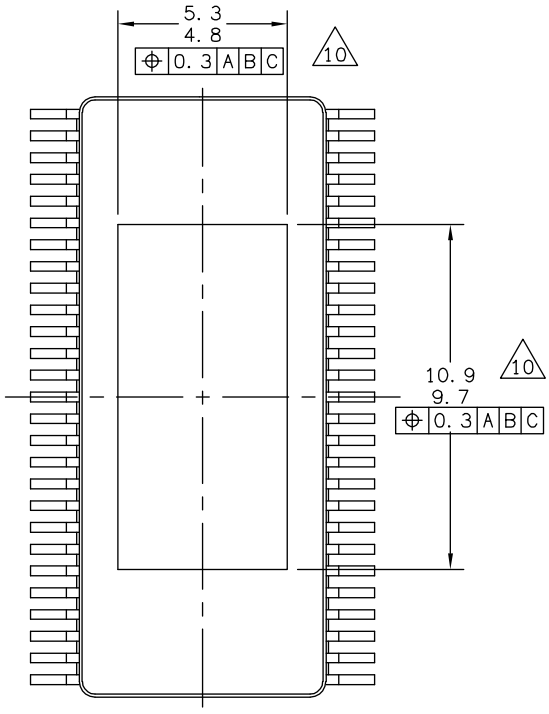


Figure 18. EMC/EMI Recommendations



SECTION B–B

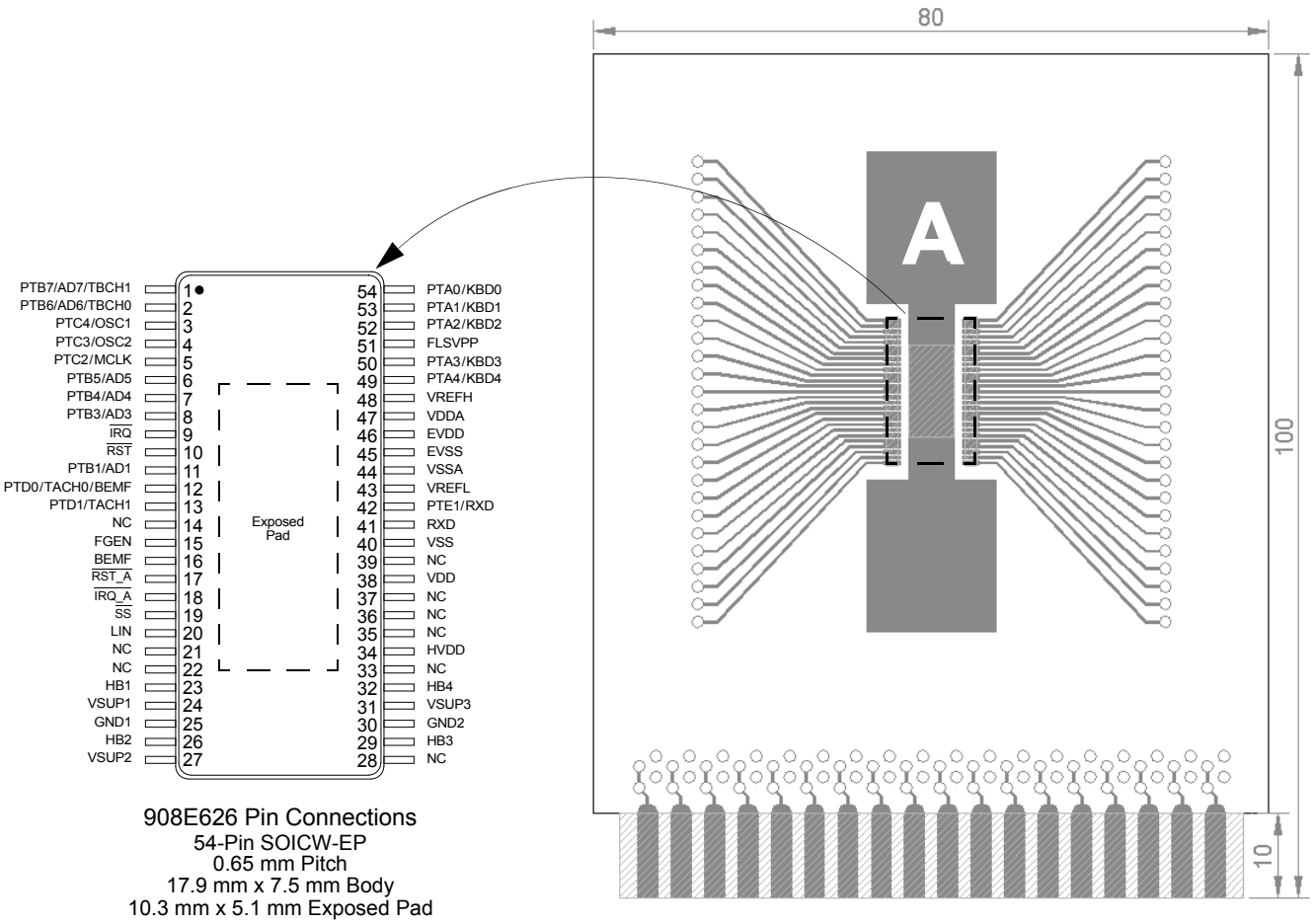


VIEW C–C

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 54LD SOIC W/B, 0.65 PITCH 5.1 X 10.3 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ARL10519D	REV: D
	CASE NUMBER: 1400–03	02 MAY 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D

908E626



908E626 Pin Connections
54-Pin SOICW-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 21. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 13. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m = 1, *n* = 1	*m* = 1, *n* = 2 *m* = 2, *n* = 1	*m* = 2, *n* = 2
$R_{\theta JAmn}$	0	53	48	53
	300	39	34	38
	600	35	30	34
$R_{\theta JSmn}$	0	21	16	20
	300	15	11	15
	600	14	9.0	13

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JSmn}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

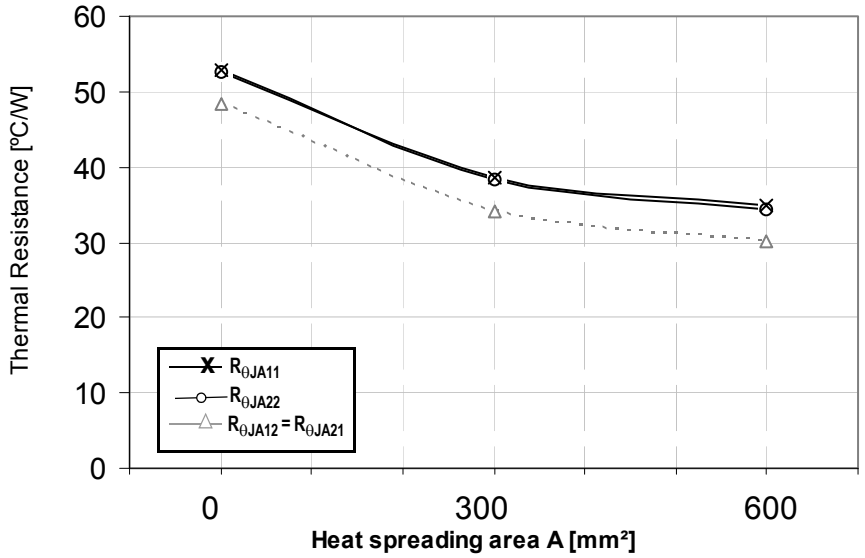


Figure 22. Device on Thermal Test Board $R_{\theta JA}$

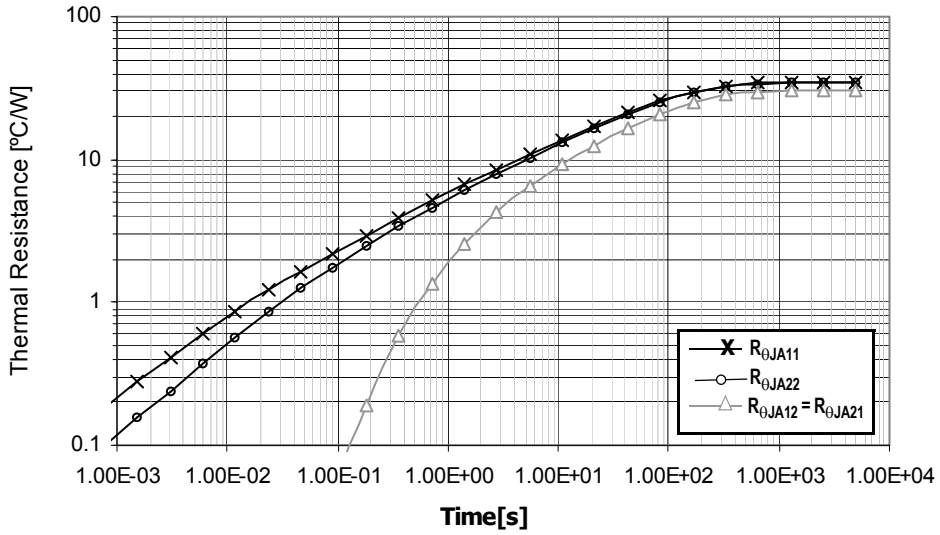


Figure 23. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)