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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	13
Voltage - Supply	8V ~ 18V
Operating Temperature	-40°C ~ 115°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e626avpekr2

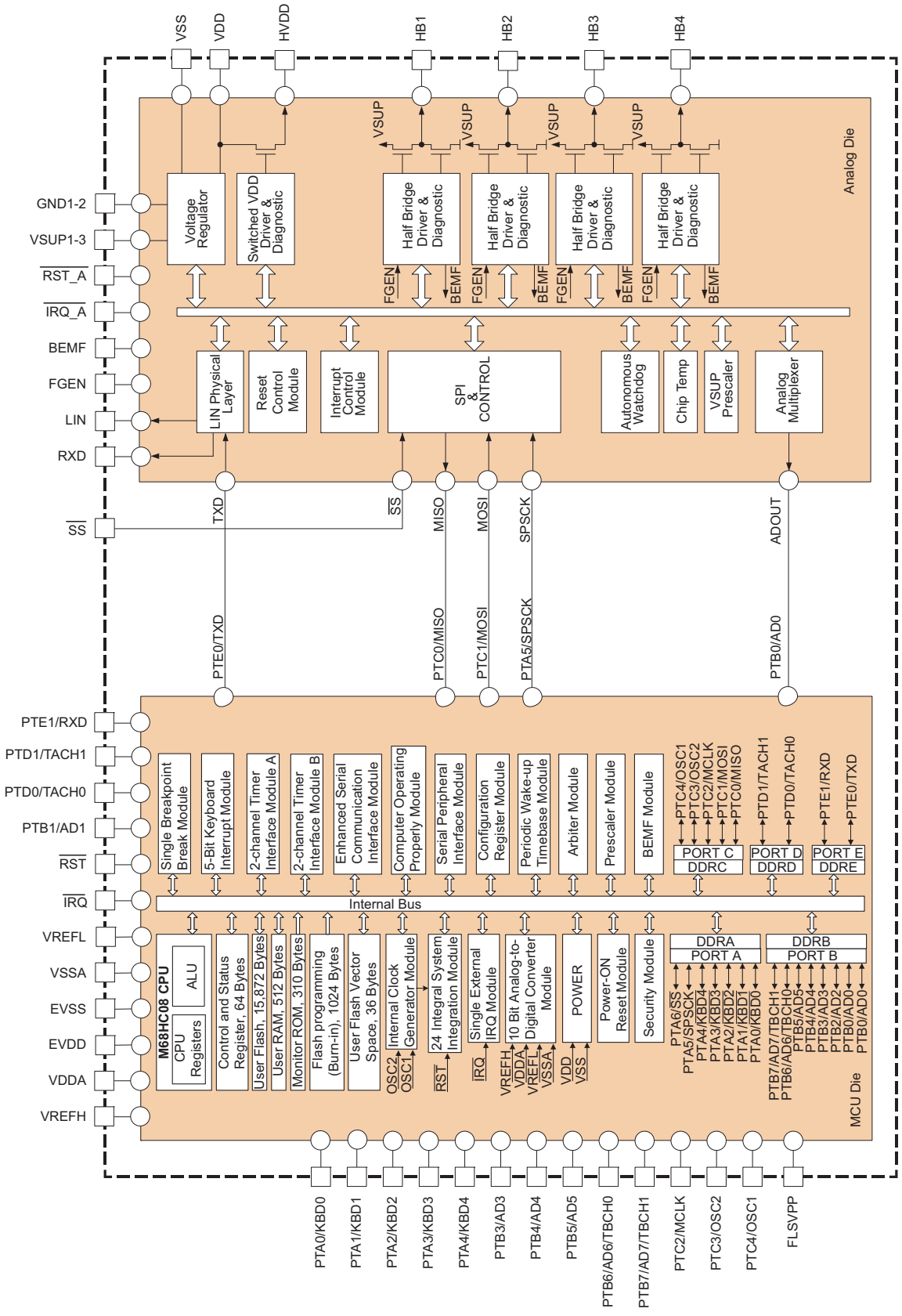


Figure 2. 908E626 Simplified Internal Block Diagram

Table 1. 908E626 PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin Description section beginning on page 15.

Die	Pin	Pin Name	Formal Name	Definition
–	14, 21, 22, 28, 33, 35, 36, 37, 39	NC	No Connect	Not connected.
MCU	42	PTE1/RXD	Port E I/O	This pin is a special function, bidirectional I/O port pin that can is shared with other functional modules in the MCU.
MCU	43 48	VREFL VREFH	ADC References	These pins are the reference voltage pins for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Pins	These pins are the power supply pins for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	15	FGEN	Current Limitation Frequency Input	This is the input pin for the half-bridge current limitation PWM frequency.
Analog	16	BEMF	Back Electromagnetic Force Output	This pin gives the user information about back electromagnetic force (BEMF).
Analog	17	$\overline{\text{RST\_A}}$	Internal Reset	This pin is the bidirectional reset pin of the analog die.
Analog	18	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	19	$\overline{\text{SS}}$	Slave Select	This pin is the SPI slave select pin for the analog chip.
Analog	20	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
Analog	23 26 29 32	HB1 HB2 HB3 HB4	Half-bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for step motor drivers, DC motor drivers, or as high side and low side switches.
Analog	24 27 31	VSUP1 VSUP2 VSUP3	Power Supply Pins	These pins are device power supply pins.
Analog	25 30	GND1 GND2	Power Ground Pins	These pins are device power ground connections.
Analog	34	HVDD	Switchable V_{DD} Output	This pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3 pin Hall-effect sensors.
Analog	38	VDD	Voltage Regulator Output	The 5.0 V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	40	VSS	Voltage Regulator Ground	Ground pin for the connection of all non-power ground connections (microcontroller and sensors).
Analog	41	RXD	LIN Transceiver Output	This pin is the output of LIN transceiver.
–	EP	Exposed Pad	Exposed Pad	The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage			V
Analog Chip Supply Voltage under Normal Operation (Steady-state)	$V_{SUP(SS)}$	-0.3 to 28	
Analog Chip Supply Voltage under Transient Conditions (1)	$V_{SUP(PK)}$	-0.3 to 40	
Microcontroller Chip Supply Voltage	V_{DD}	-0.3 to 6.0	
Input Pin Voltage			V
Analog Chip	$V_{IN(ANALOG)}$	-0.3 to 5.5	
Microcontroller Chip	$V_{IN(MCU)}$	V_{SS}-0.3 to V_{DD}+0.3	
Maximum Microcontroller Current per Pin			mA
All Pins Except VDD, VSS, PTA0:PTA6, PTC0:PTC1	$I_{PIN(1)}$	±15	
Pins PTA0:PTA6, PTC0:PTC1	$I_{PIN(2)}$	±25	
Maximum Microcontroller V_{SS} Output Current	I_{MVSS}	100	mA
Maximum Microcontroller V_{DD} Input Current	I_{MVDD}	100	mA
LIN Supply Voltage			V
Normal Operation (Steady-state)	$V_{BUS(SS)}$	-18 to 28	
Transient Conditions (1)	$V_{BUS(DYNAMIC)}$	40	
ESD Voltage			V
Human Body Model (2)	V_{ESD1}	±3000	
Machine Model (3)	V_{ESD2}	±150	
Charge Device Model (4)	V_{ESD3}	±500	

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. ESD3 testing is performed in accordance with Charge Device Model, robotic (C_{ZAP} = 4.0 pF).

STATIC ELECTRICAL CHARACTERISTICS

Table 3. STATIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Nominal Operating Voltage	V_{SUP}	8.0	–	18	V
SUPPLY CURRENT					
NORMAL Mode V_{SUP} = 12 V, Power Die ON (PSON=1), MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	–	20	–	mA
STOP Mode (9) V_{SUP} = 12 V, Cyclic Wake-up Disabled	I_{STOP}	–	–	75	µA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Pins $\overline{RST\_A}$, $\overline{IRQ\_A}$					V
Low State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High State Output Voltage (I_{OUT} = 1.0 µA)	V_{OH}	3.85	–	–	
Output Pins BEMF, RXD					V
Low State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High State Output Voltage (I_{OUT} = 1.5 mA)	V_{OH}	3.85	–	–	
Output Pin RXD– Capacitance (10)	C_{IN}	–	4.0	–	pF
Input Pins $\overline{RST\_A}$, FGEN, $\overline{SS}$					V
Input Logic Low Voltage	V_{IL}	–	–	1.5	
Input Logic High Voltage	V_{IH}	3.5	–	–	
Input Pins $\overline{RST\_A}$, FGEN, $\overline{SS}$–Capacitance (10)	C_{IN}	–	4.0	–	pF
Pins $\overline{RST\_A}$, $\overline{IRQ\_A}$–Pull-up Resistor	$R_{PULLUP1}$	–	10	–	kΩ
Pin $\overline{SS}$–Pull-up Resistor	$R_{PULLUP2}$	–	60	–	kΩ
Pins FGEN, MOSI, SPSCK–Pull-down Resistor	$R_{PULLDOWN}$	–	60	–	kΩ
Pin TXD–Pull-up Current Source	I_{PULLUP}	–	35	–	µA

Notes

9. STOP mode current will increase if V_{SUP} exceeds 15 V.
10. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Output Low Level TXD LOW, 500 Ω Pull-up to V_{SUP}	$V_{LIN-LOW}$	–	–	1.4	V
Output High Level TXD HIGH, I_{OUT} = 1.0 µA	$V_{LIN-HIGH}$	V_{SUP}-1.0	–	–	V
Pull-up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Leakage Current to GND Recessive State (-0.5 V < V_{LIN} < V_{SUP})	$I_{BUS\_PAS\_REC}$	0.0	–	20	µA
Leakage Current to GND (V_{SUP} Disconnected) Including Internal Pull-up Resistor, V_{LIN} @ -18 V Including Internal Pull-up Resistor, V_{LIN} @ +18 V	 $I_{BUS\_NO\_GND}$ I_{BUS}	 – –	 -600 25	 – –	µA
LIN Receiver Recessive Dominant Threshold Input Hysteresis	 V_{IH} V_{IL} V_{ITH} V_{IHY}	 0.6V_{LIN} 0 – 0.01V_{SUP}	 – – V_{SUP}/2 –	 V_{SUP} 0.4V_{LIN} – 0.1V_{SUP}	V
LIN Wake-up Threshold	V_{WTH}	–	V_{SUP}/2	–	V
HALF-BRIDGE OUTPUTS (HB1:HB4)					
Switch ON Resistance @ T_J = 25 °C with I_{LOAD} = 1.0 A High Side Low Side	 $R_{DS(ON)HB\_HS}$ $R_{DS(ON)HB\_LS}$	 – –	 425 400	 500 500	mΩ
High Side Overcurrent Shutdown	I_{HBHSOC}	3.0	–	7.5	A
Low Side Overcurrent Shutdown	I_{HBLSOC}	2.5	–	7.5	A
Low Side Current Limitation @ T_J = 25 °C Current Limit 1 (CLS2 = 0, CLS1 = 1, CLS0 = 1) Current Limit 2 (CLS2 = 1, CLS1 = 0, CLS0 = 0) Current Limit 3 (CLS2 = 1, CLS1 = 0, CLS0 = 1) Current Limit 4 (CLS2 = 1, CLS1 = 1, CLS0 = 0) Current Limit 5 (CLS2 = 1, CLS1 = 1, CLS0 = 1)	 I_{CL1} I_{CL2} I_{CL3} I_{CL4} I_{CL5}	 – 210 300 450 600	 55 260 370 550 740	 – 315 440 650 880	mA
Half-bridge Output HIGH Threshold for BEMF Detection	V_{BEMFH}	–	-30	0.0	V
Half-bridge Output LOW Threshold for BEMF Detection	V_{BEMFL}	–	-60	-5.0	mV
Hysteresis for BEMF Detection	V_{BEMFHY}	–	30	–	mV
Low Side Current-to-Voltage Ratio (V_{ADOUT} [V]/I_{HB} [A]) CSA = 1 CSA = 0	 $RATIO_H$ $RATIO_L$	 7.0 1.0	 12.0 2.0	 14.0 3.0	V/A

Table 5. MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
ADC	10 Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud Rate Adjustment
ICG	Internal Clock Generation Module
BEMF Counter	Special Counter for *SMARTMOS* BEMF Output

TIMING DIAGRAMS

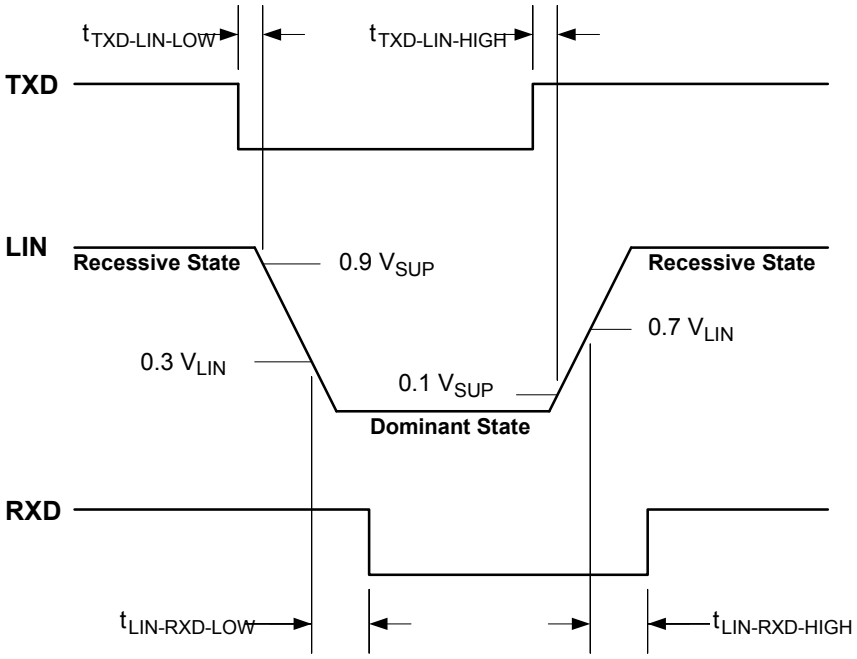
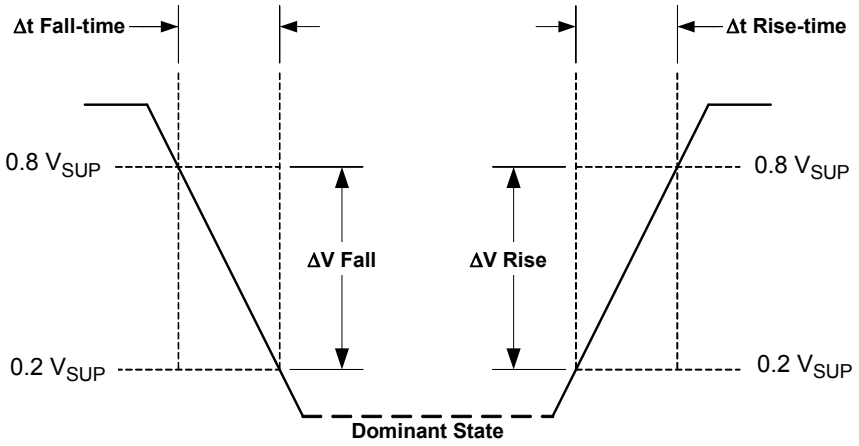


Figure 4. LIN Timing Description



$$SR_F = \frac{\Delta V\ Fall}{\Delta t\ Fall\text{-}time} \qquad SR_R = \frac{\Delta V\ Rise}{\Delta t\ Rise\text{-}time}$$

Figure 5. LIN Slew Rate Description

FUNCTIONAL DIAGRAMS

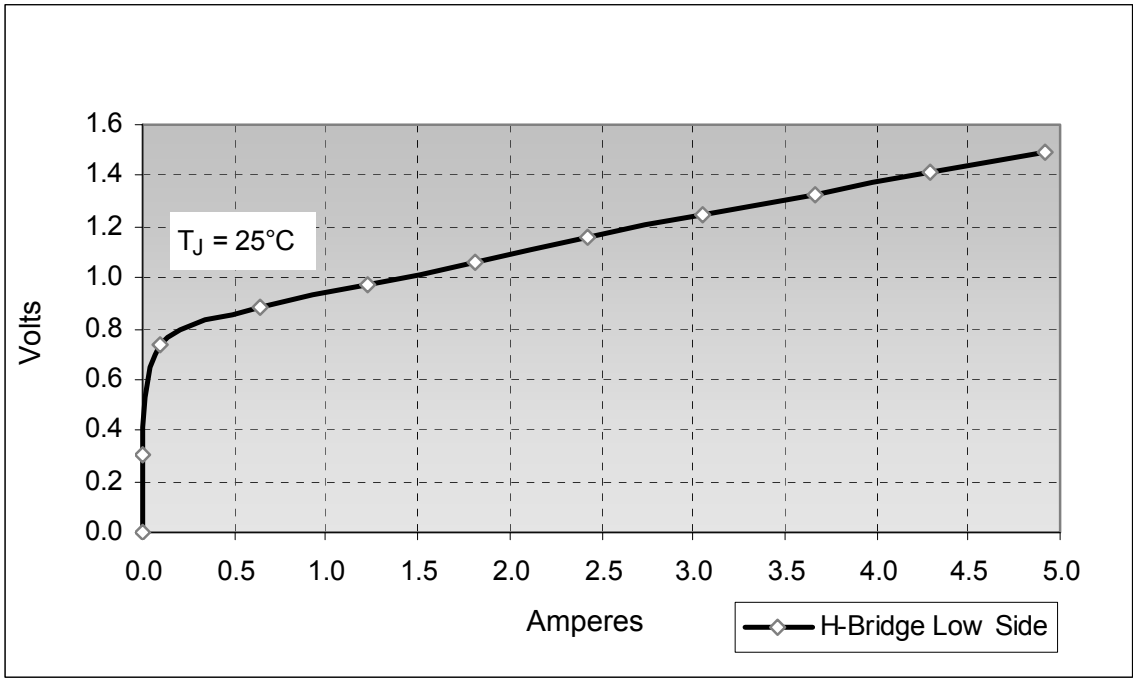


Figure 6. Free Wheel Diode Forward Voltage

CURRENT LIMITATION FREQUENCY INPUT PIN (FGEN)

Input pin for the half-bridge current limitation PWM frequency. This input is not a real PWM input pin; it should just supply the period of the PWM. The duty cycle will be generated automatically.

Important The recommended FGEN frequency should be in the range of 0.1 kHz to 20 kHz.

BACK ELECTROMAGNETIC FORCE OUTPUT PIN (BEMF)

This pin gives the user information about back electromagnetic force (BEMF). This feature allows stall detection and coil failures in step motor applications. In order to evaluate this signal the pin must be directly connected to pin PTD0/TACH0/BEMF.

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset pin of the analog die. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

SLAVE SELECT PIN ($\overline{\text{SS}}$)

This pin is the SPI Slave Select pin for the analog chip. All other SPI connections are done internally. $\overline{\text{SS}}$ must be connected to PTB1 or any other logic I/O of the microcontroller.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E626 device includes power MOSFETs configured as four half-bridge driver outputs. The HB1:HB4 outputs may be configured for step motor drivers, DC motor drivers, or as high side and low side switches.

The HB1:HB4 outputs are short-circuit and overtemperature protected, and they feature current recopy, current limitation, and BEMF generation. Current limitation and recopy are done on the low side MOSFETs.

POWER SUPPLY PINS (VSUP1:VSUP3)

VSUP1:VSUP3 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1 AND GND2)

GND1 and GND2 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

SWITCHABLE V_{DD} OUTPUT PIN (HVDD)

The HVDD pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; The output is short-circuit protected.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD, VDDA, and VREFH pins must be connected together.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors).

Important VSS, EVSS, VSSA, and VREFL pins must be connected together.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces.

VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should be either left open (not connected) or connected to GND.

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

- 0 = High temperature condition has not occurred.

LVF—LOW VOLTAGE FLAG BIT

This read/write flag is set on a low voltage condition. Clear LVF by writing a logic [1] to LVF. If a low voltage condition is still present while writing a logic [1] to LVF, the writing has no effect. Therefore, a low voltage interrupt cannot be lost due to inadvertent clearing of LVF. Reset clears the LVF bit. Writing a logic [0] to LVF has no effect.

- 1 = Low voltage condition has occurred.
- 0 = Low voltage condition has not occurred.

HVF—HIGH VOLTAGE FLAG BIT

This read/write flag is set on a high voltage condition. Clear HVF by writing a logic [1] to HVF. If high voltage condition is still present while writing a logic [1] to HVF, the writing has no effect. Therefore, a high voltage interrupt cannot be lost due to inadvertent clearing of HVF. Reset clears the HVF bit. Writing a logic [0] to HVF has no effect.

- 1 = High voltage condition has occurred.
- 0 = High voltage condition has not occurred.

OCF—OVERCURRENT FLAG BIT

This read-only flag is set on an overcurrent condition. Reset clears the OCF bit. To clear this flag, write a logic [1] to the appropriate overcurrent flag in the SYSSTAT Register. See Figure 9, which shows the two signals triggering the OCF.

- 1 = High current condition has occurred.
- 0 = High current condition has not occurred.

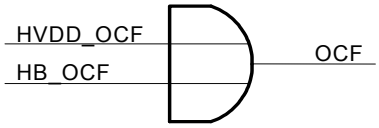


Figure 9. Principal Implementation for OCF

INTERRUPT MASK REGISTER (IMR)

Register Name and Address: IMR - $04

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	LINIE	HTIE	LVIE	HVIE	OCIE	0
Write								
Reset	0	0	0	0	0	0	0	0

LINIE—LIN LINE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the LIN flag, LINF. Reset clears the LINIE bit.

- 1 = Interrupt requests from LINF flag enabled.
- 0 = Interrupt requests from LINF flag disabled.

HTIE—HIGH TEMPERATURE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the high temperature flag, HTF. Reset clears the HTIE bit.

- 1 = Interrupt requests from HTF flag enabled.
- 0 = Interrupt requests from HTF flag disabled.

LVIE—LOW VOLTAGE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the low voltage flag, LVF. Reset clears the LVIE bit.

- 1 = Interrupt requests from LVF flag enabled.
- 0 = Interrupt requests from LVF flag disabled.

HVIE—HIGH VOLTAGE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the high voltage flag, HVF. Reset clears the HVIE bit.

- 1 = Interrupt requests from HVF flag enabled.
- 0 = Interrupt requests from HVF flag disabled.

OCIE—OVERCURRENT INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the overcurrent flag, OCF. Reset clears the OCIE bit.

- 1 = Interrupt requests from OCF flag enabled.
- 0 = Interrupt requests from OCF flag disabled.

RESET

The 908E626 chip has four internal reset sources and one external reset source, as explained in the paragraphs below. Figure 10 depicts the internal reset sources.

SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) creates the communication link between the microcontroller and the 908E626.

The interface consists of four pins (see Figure 11):

- $\overline{SS}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock (maximum frequency 4.0 MHz)

A complete data transfer via the SPI consists of 2 bytes. The master sends address and data, slave system status, and data of the selected address.

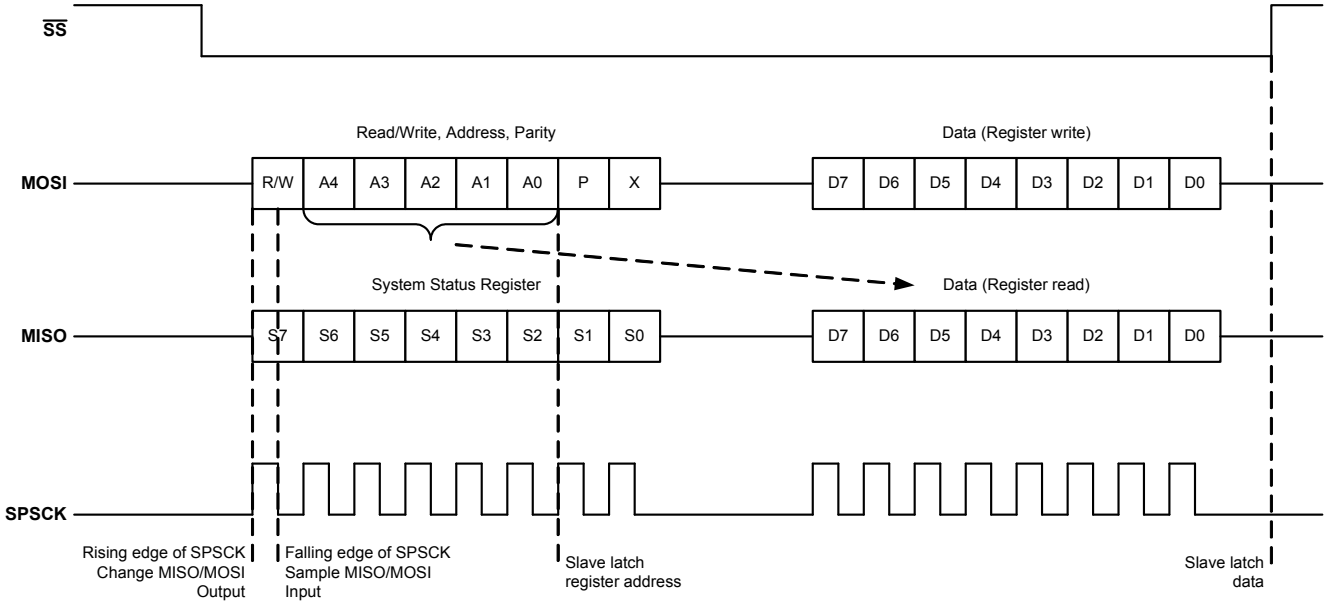


Figure 11. SPI Protocol

During the inactive phase of $\overline{SS}$, the new data transfer is prepared. The falling edge on the $\overline{SS}$ line indicates the start of a new data transfer and puts MISO in the low-impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.

The MISO output changes data on a rising edge of SPSCK. The MOSI input is sampled on a falling edge of SPSCK. The data transfer is only valid if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.

After a write operation, the transmitted data is latched into the register by the rising edge of $\overline{SS}$. Register read data is internally latched into the SPI at the time when the parity bit is transferred. $\overline{SS}$ HIGH forces MISO to high-impedance.

MASTER ADDRESS BYTE

A4:A0

Contains the address of the desired register.

R/$\overline{W}$

Contains information about a read or a write operation.

- If R/$\overline{W}$ = 1, the second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0, the master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SMARTMOS* register on rising edge of $\overline{SS}$.

Parity P

The parity bit is equal to “0” if the number of 1 bits is an even number contained within R/$\overline{W}$, A4:A0. If the number of 1 bits is odd, P equals “1”. For example, if R/$\overline{W}$ = 1, A4:A0 = 00001, then P equals “0.”

The parity bit is only evaluated during a write operation.

Bit X

Not used.

Master Data Byte

Contains data to be written or no valid data during a read operation.

HALF-BRIDGES

Outputs HB1:HB4 provide four low resistive half-bridge output stages. The half-bridges can be used in H-Bridge, high side, or low side configurations.

Reset clears all bits in the H-Bridge Output Register (HBOUT) owing to the fact that all half-bridge outputs are switched off.

HB1:HB4 output features:

- Short-circuit (overcurrent) protection on high side and low side MOSFETs.
- Current recopy feature (low side MOSFET).
- Overtemperature protection.
- Overvoltage and undervoltage protection.
- Current limitation feature (low side MOSFET).

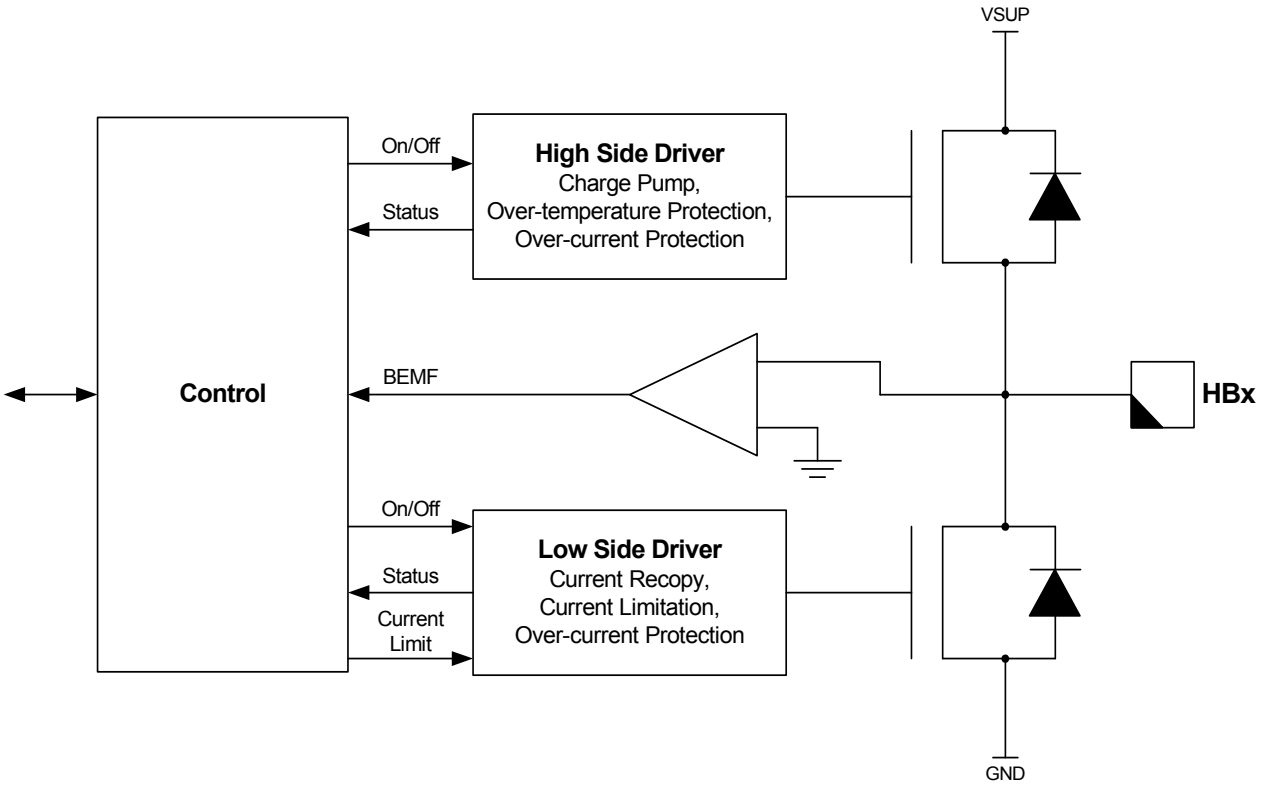


Figure 12. Half-bridge Push-Pull Output Driver

Half-bridge Control

Each output MOSFET can be controlled individually. The general enable of the circuitry is done by setting PSON in the System Control Register (SYSCTL). HBx_L and HBx_H form one half-bridge. It is not possible to switch on both MOSFETs in one half-bridge at the same time. If both bits are set, the high side MOSFET has a higher priority.

To avoid both MOSFETs (high side and low side) of one half-bridge being on at the same time, a break-before-make circuit exists.Switching the high side MOSFET on is inhibited as long as the potential between gate and V_{SS} is not below a certain threshold. Switching the low side MOSFET on is blocked as long as the potential between gate and source of the high side MOSFET did not fall below a certain threshold.

Half-bridge Output Register (HBOUT)

Register Name and Address: HBOUT - $01

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
Reset	0	0	0	0	0	0	0	0

HBx_L—Low Side On/Off Bits

These read/write bits turn on the low side MOSFETs. Reset clears the HBx_L bits.

- 1 = Low side MOSFET turned on for half-bridge output x.
- 0 = Low side MOSFET turned off for half-bridge output x.

HBx_H—High Side On/Off Bits

These read/write bits turn on the high side MOSFETs. Reset clears the HBx_H bits.

- 1 = High side MOSFET turned on for half-bridge output x.
- 0 = High side MOSFET turned on for half-bridge output x.

HALF-BRIDGE CURRENT LIMITATION

Each low side MOSFET offers a current limit or constant current feature. This features is realized by a pulse width modulation on the low side MOSFET. The pulse width modulation on the outputs is controlled by the FGEN input and the load characteristics. The FGEN input provides the PWM frequency, whereas the duty cycle is controlled by the load characteristics.

The recommended frequency range for the FGEN and the PWM is 0.1 kHz to 20 kHz.

Functionality

Each low side MOSFET switches off if a current above the selected current limit was detected. The 908E626 offers five different current limits (refer to Table 8, for current limit values). The low side MOSFET switches on again if a rising edge on the FGEN input was detected (Figure 13).

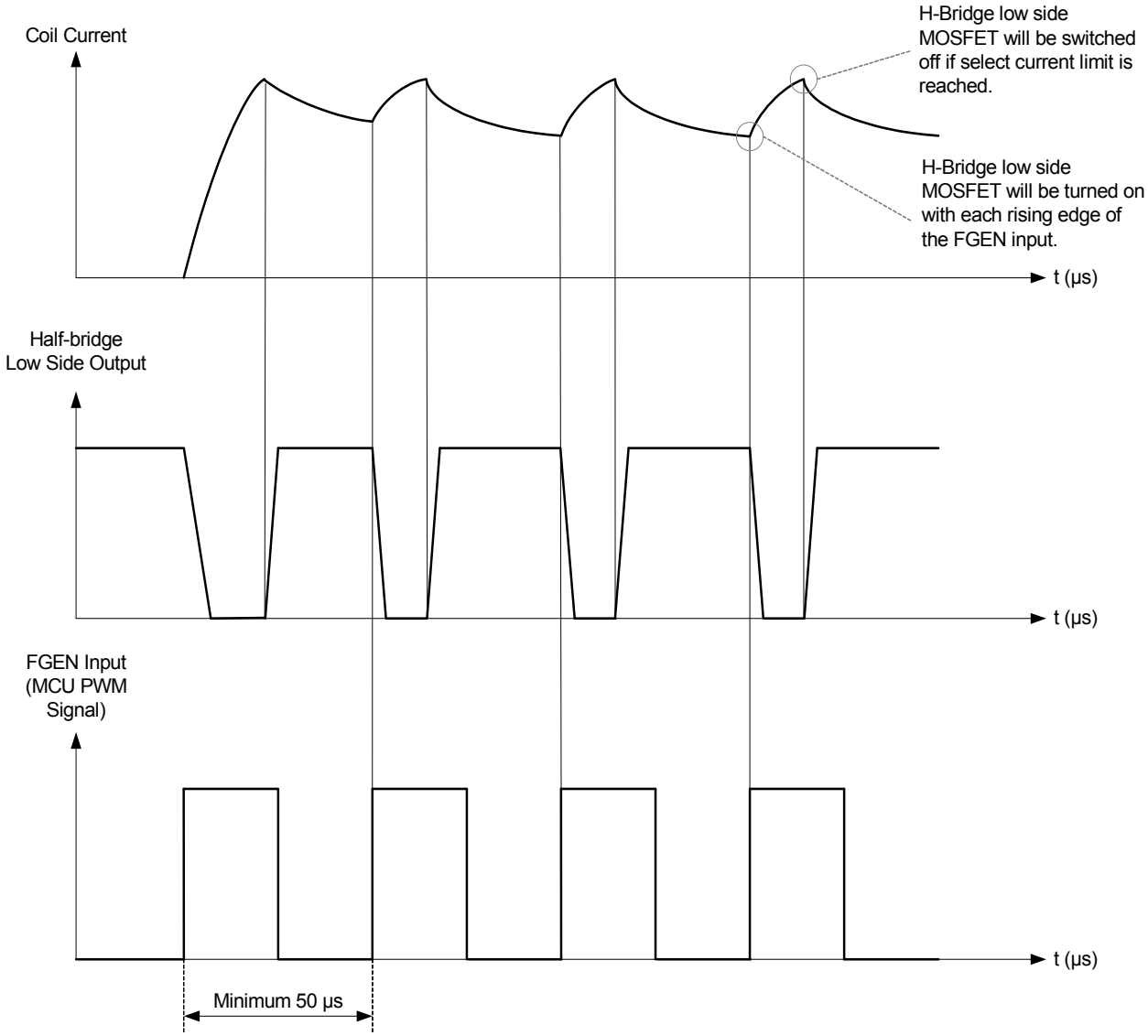


Figure 13. Half-bridge Current Limitation

- 1 = Current sense amplification set for measuring 0.5 A.
- 0 = Current sense amplification set for measuring 2.5 A.

CLS2:CLS0—H-Bridge Current Limitation Selection Bits

These read/write bits select the current limitation value according to Table 8. Reset clears the CLS2:CLS0 bits.

Table 8. H-Bridge Current Limitation Value Selection Bits

CLS2	CLS1	CLS0	Current Limit
0	0	0	No Limit
0	0	1	
0	1	0	
0	1	1	55 mA (typ)
1	0	0	260 mA (typ)
1	0	1	370 mA (typ)
1	1	0	550 mA (typ)
1	1	1	740 mA (typ)

Switchable VDD Outputs

The HVDD pin is a switchable VDD output pin. It can be used for driving external circuitry that requires a V_{DD} voltage. The output is enabled with bit PSON in the System Control Register and can be switched on/off with bit HVDDON in the Power Output Register. Low or high voltage conditions (LVI/HVI) have no influence on this circuitry.

HVDD Overtemperature Protection

Overtemperature protection is enabled if the high temperature reset is enabled.

HVDD Overcurrent Protection

The HVDD output is protected against overcurrent. In the event the overcurrent limit is or was reached, the output automatically switches off and the HVDD overcurrent flag in the System Status Register is set.

System Control Register (SYSCTL)

Register Name and Address: SYSCTL - $03

	Bit7	6	5	4	3	2	1	Bit0
Read	PSON	SRS1	SRS0	0	0	0	0	0
Write								GS
Reset	0	0	0	0	0	0	0	0

PSON—Power Stages On Bit

This read/write bit enables the power stages (half-bridges, LIN transmitter and HVDD output). Reset clears the PSON bit.

- 1 = Power stages enabled.
- 0 = Power stages disabled.

SRS0:SRS1—LIN Slew Rate Selection Bits

These read/write bits enable the user to select the appropriate LIN slew rate for different baud rate configurations as shown in Table 9.

The high speed slew rates are used, for example, for programming via the LIN and are not intended for use in the application.

Table 9. LIN Slew Rate Selection Bits

SRS1	SRS0	LIN Slew Rate
0	0	Initial Slew Rate (20 kBaud)
0	1	Slow Slew Rate (10 kBaud)
1	0	High Speed II (8x)
1	1	High Speed I (4x)

Go to STOP Mode Bit (GS)

This write-only bit instructs the 908E626 to power down and go into STOP mode. Reset or CPU interrupt requests clear the GS bit.

- 1 = Power down and go into STOP mode
- 0 = Not in STOP mode

System Status Register (SYSSTAT)

Register Name and Address: SYSSTAT - $0c

	Bit7	6	5	4	3	2	1	Bit0
Read	0	LINCL	HVDD_OCF	0	LVF	HVF	$\overline{HB\_OCF}$	HTF
Write								
Reset	0	0	0	0	0	0	0	0

LINCL — LIN Current Limitation Bit

This read-only bit is set if the LIN transmitter operates in current limitation region. Due to excessive power dissipation in the transmitter, software is advised to turn the transmitter off immediately.

- 1 = Transmitter operating in current limitation region.
- 0 = Transmitter not operating in current limitation region.

HVDD_OCF—HVDD Output Overcurrent Flag Bit

This read/write flag is set on an overcurrent condition at the HVDD pin. Clear HVDD_OCF and enable the output by writing a logic [1] to the HVDD_OCF Flag. Reset clears the

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E626 has the MC68HC908EY16 MCU embedded, typically all the development tools available for the MCU also apply for this device. However, due to the fact of the additional analog die circuitry and the nominal +12 V supply voltage some additional items have to be considered:

- nominal 12 V rather than 5.0 V or 3.0 V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ pin, but also the $\overline{IRQ\_A}$ pin

For a detailed information on the MCU related development support, see the MC68HC908EY16 datasheet - section, development support.

The programming is principally possible at two stages in the manufacturing process - first on chip level, before the IC is soldered onto a pcb board, and second, after the IC is soldered onto the pc board.

Chip level programming

At the Chip level, the easiest way is to only power the MCU with +5.0 V (see Figure 16), and not provide the analog chip with VSUP. In this setup, all the analog pins should be left open (e.g. VSUP[1:3]), and interconnections between the MCU and the analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 datasheet - section, development support.

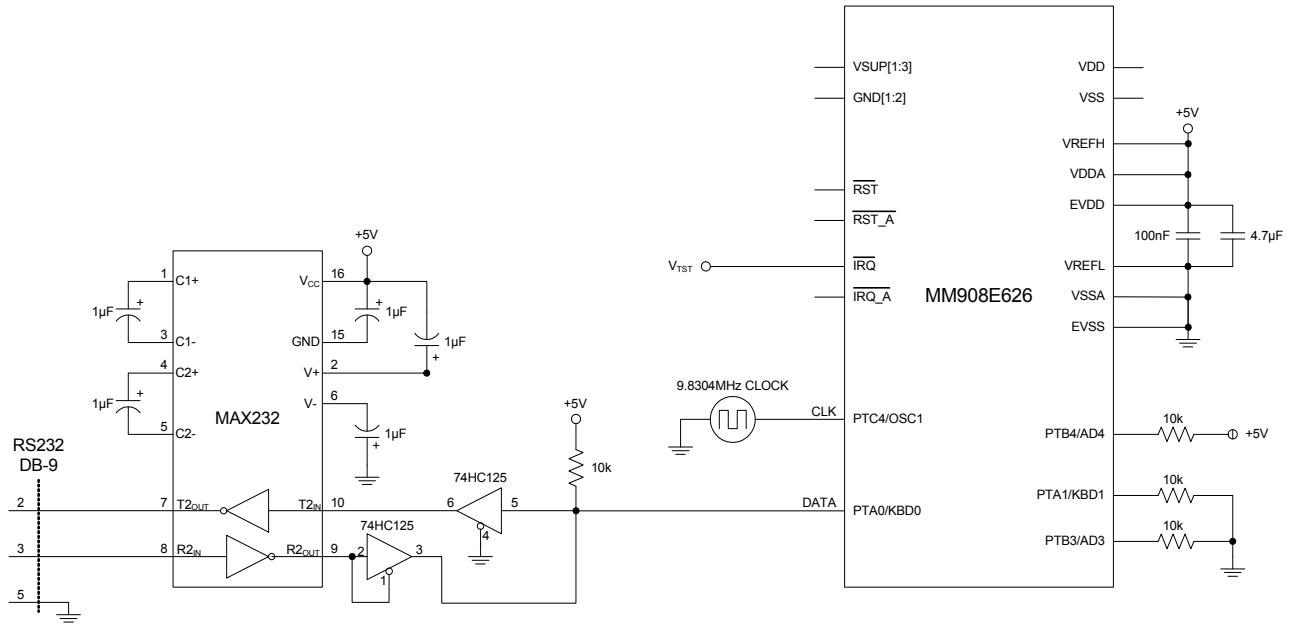


Figure 16. Normal Monitor Mode Circuit (MCU only)

It is also possible to supply the whole system with V_{SUP} (12 V) instead as described in Figure 17.

PCB level programming

If the IC is soldered onto the pc board, it is typically not possible to separately power the MCU with +5.0 V. The whole system has to be powered up providing V_{SUP} (see Figure 17).

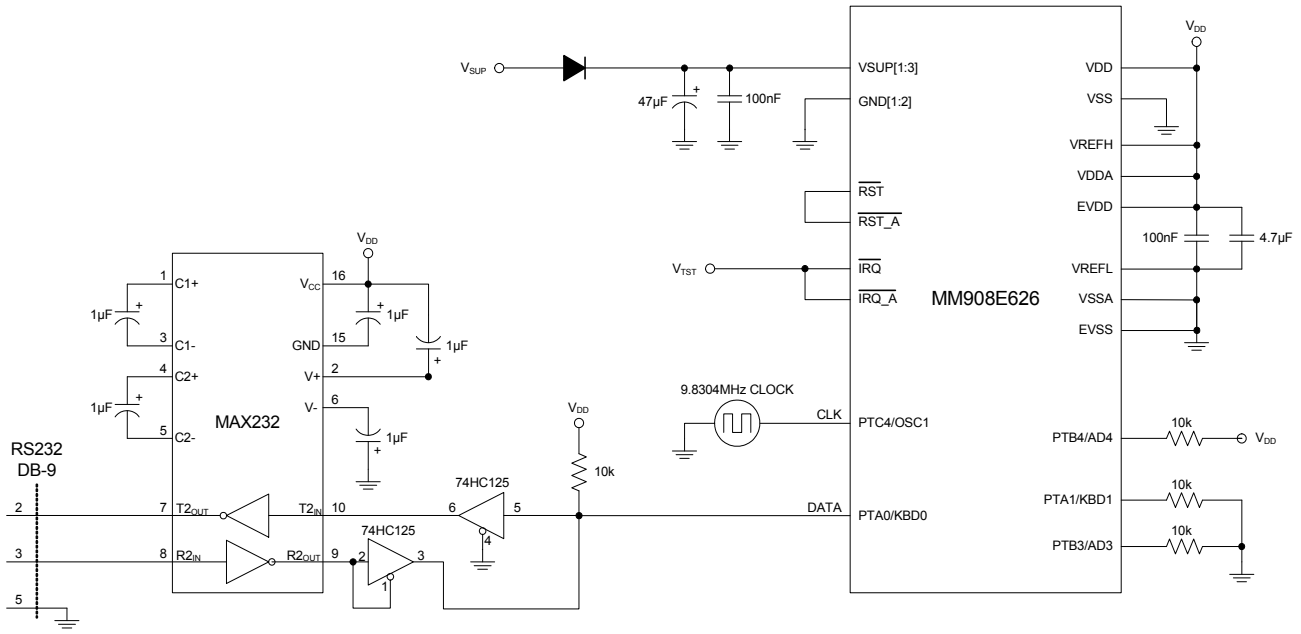


Figure 17. Normal Monitor Mode Circuit

Table 10 summarizes the possible configurations and the necessary setups.

Table 10. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Timeout	Communication Speed		
				PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND							ON	disabled	disabled	—	Nominal 1.6 MHz	Nominal 6300
User	V_{DD}	V_{DD}	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6 MHz	Nominal 6300

Notes

19. PTA0 must have a pull-up resistor to V_{DD} in monitor mode
20. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1
21. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
22. X = don't care
23. V_{TST} is a high voltage $V_{DD} + 3.5\ V \leq V_{TST} \leq V_{DD} + 4.5\ V$

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.4mm FROM MAXIMUM EXPOSED PAD SIZE

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TITLE: 54LD SOIC W/B, 0.65 PITCH 5.1 X 10.3 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ARL10519D	REV: D
	CASE NUMBER: 1400–03	02 MAY 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D

908E626

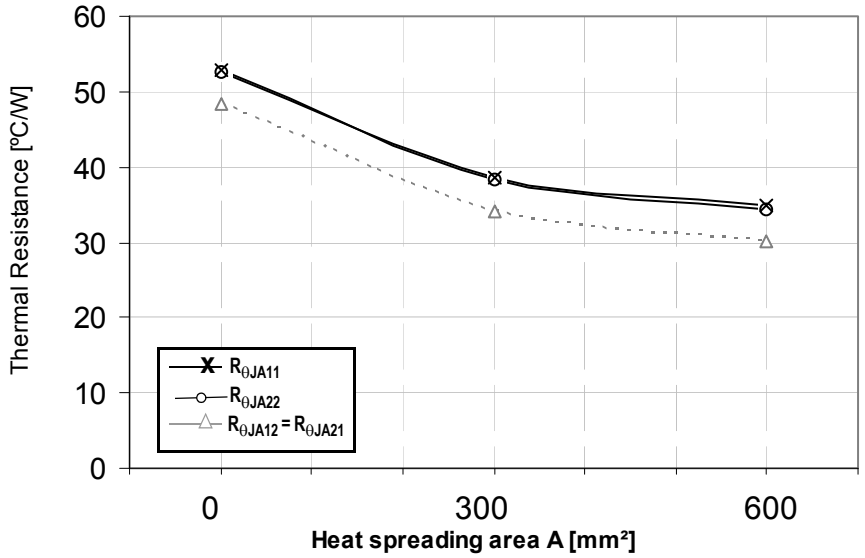

Figure 22. Device on Thermal Test Board $R_{\theta JA}$

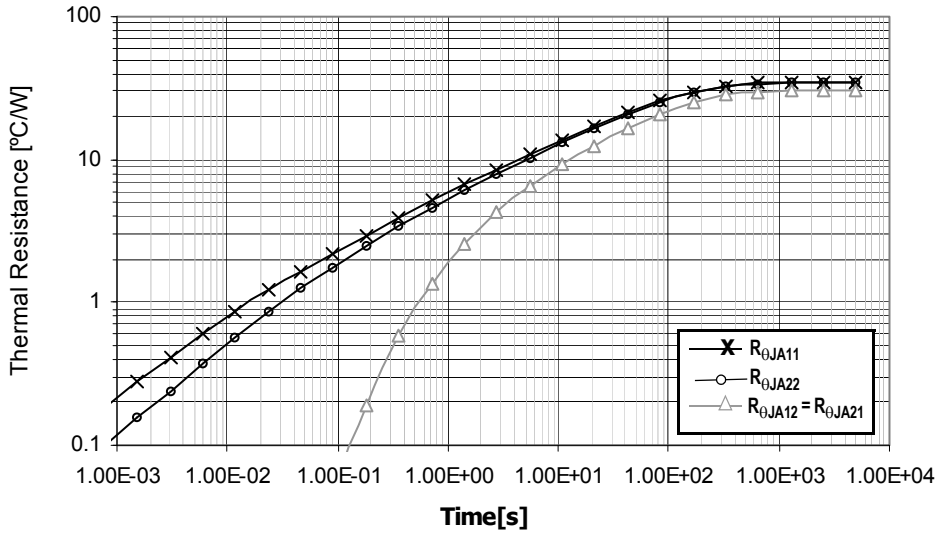

Figure 23. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	9/2008	• Implemented Revision History page • Minor corrections throughout the document • Updated to current Freescale format and style • Added MM908E626AVEK to the ordering information • Corrected package drawing designation • Added STOP mode
5.0	7/2009	• Corrected several non-technical cross-references.
6.0	9/2011	• Corrected text for Autonomous Watchdog Interrupt. Page 17. • Corrected part number in Go to STOP Mode Bit. Page 30. • Removed footnotes in register table for SYSCTL and AWDCTL. • Corrected Figure 4 LIN Timing description. • Updated Freescale form and style • Added MM908E626AVPEK to the ordering information. • Removed the DWB package type. • Added RoHS image to page 1 and RoHS statement to back page. • Changed Peak Package Reflow Temperature During Reflow description • Added note (8)
7.0	4/2012	• Added MM908E626AVPEK to the ordering information • Removed 908E626AVEK/R2 from the ordering information • Updated Freescale form and style
8.0	4/2012	• Corrected Figure 4, LIN Timing Description, replacing V_{LIN} with V_{SUP}
9.0	6/2012	• Added MM908E626AVEK/R2 to the ordering information
10.0	8/2012	• Corrected broken links within the document.
11.0	2/2013	• Removed MM908E626AVEK from the ordering information • Update format.

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