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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	94
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 41x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk51dn512clq10

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3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

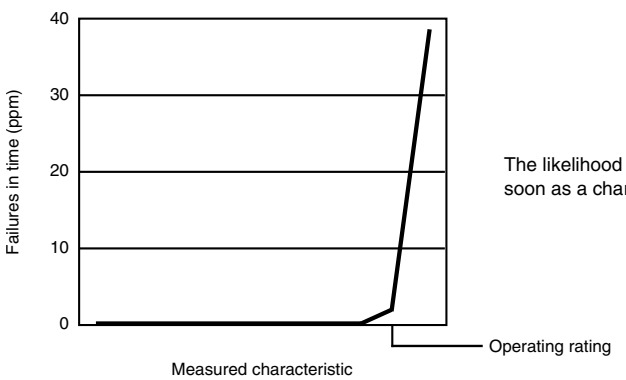
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	85	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	48	°C/W	1

Table continues on the next page...

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	29	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	36	38	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	30	25	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	16	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	9	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns

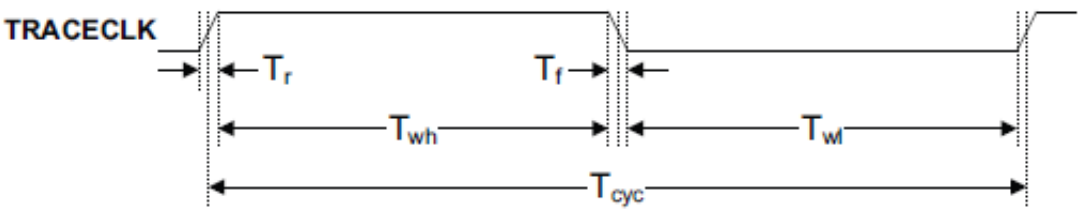


Figure 3. TRACE_CLKOUT specifications

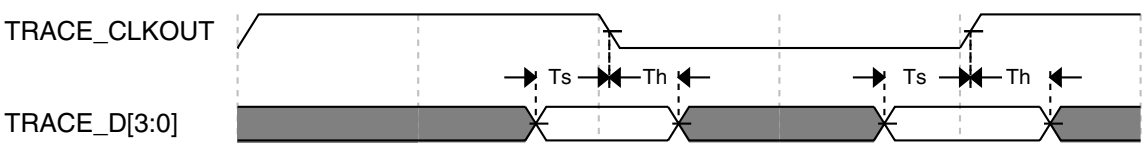


Figure 4. Trace data specifications

6.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz	— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
PLL						
f_{vco}	VCO operating frequency	48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)	—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)	—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz	 — —	 120 50	 — —	 ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz	 — —	 1350 600	 — —	 ps ps	8
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 16. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	µs	
$t_{swapx02}$	• control code 0x02	—	70	150	µs	
$t_{swapx04}$	• control code 0x04	—	70	150	µs	
$t_{swapx08}$	• control code 0x08	—	—	30	µs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.

6.4.2 EzPort switching specifications

Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz

Table continues on the next page...

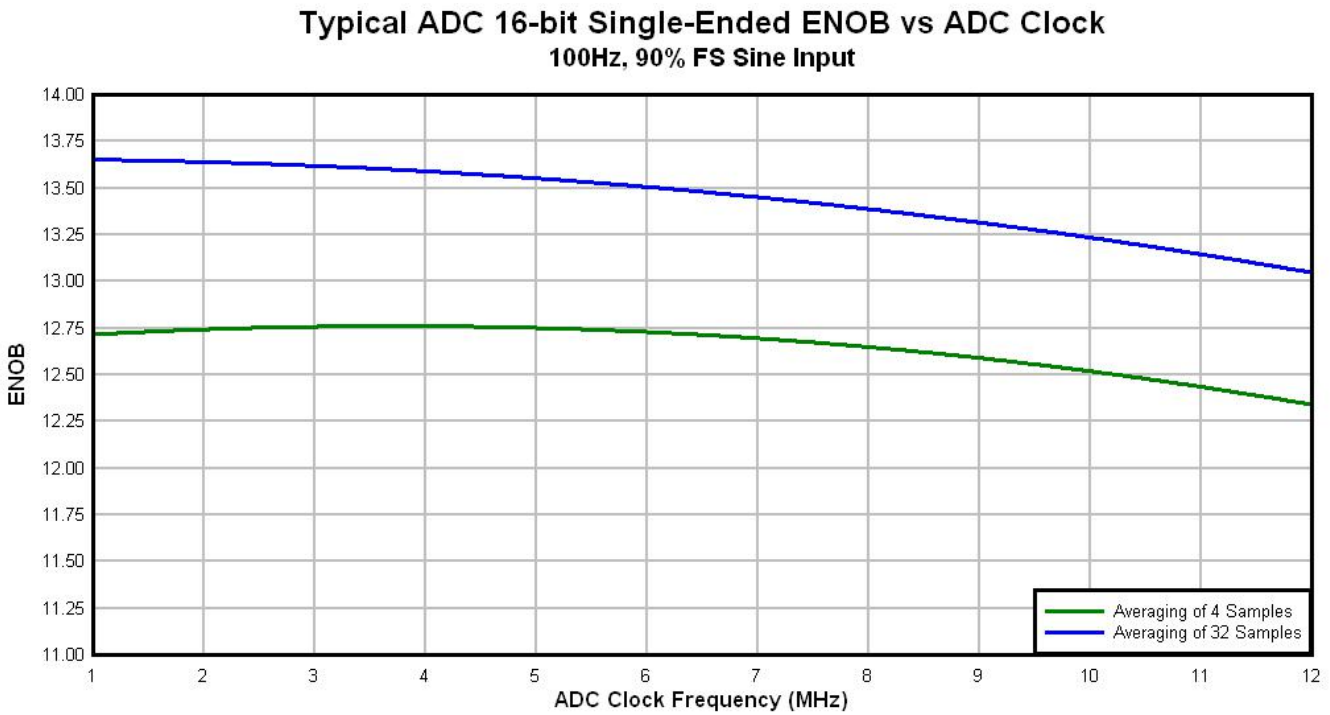


Figure 14. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.1.3 16-bit ADC with PGA operating conditions

Table 29. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V_{REFPGA}	PGA ref voltage		VREF_OUT	VREF_OUT	VREF_OUT	V	2, 3
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	
V_{CM}	Input Common Mode range		V_{SSA}	—	V_{DDA}	V	
R_{PGAD}	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	— — —	128 64 32	— — —	kΩ	IN+ to IN-[4]
R_{AS}	Analog source resistance		—	100	—	Ω	5
T_S	ADC sampling time		1.25	—	—	μs	6

Table continues on the next page...

Table 31. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

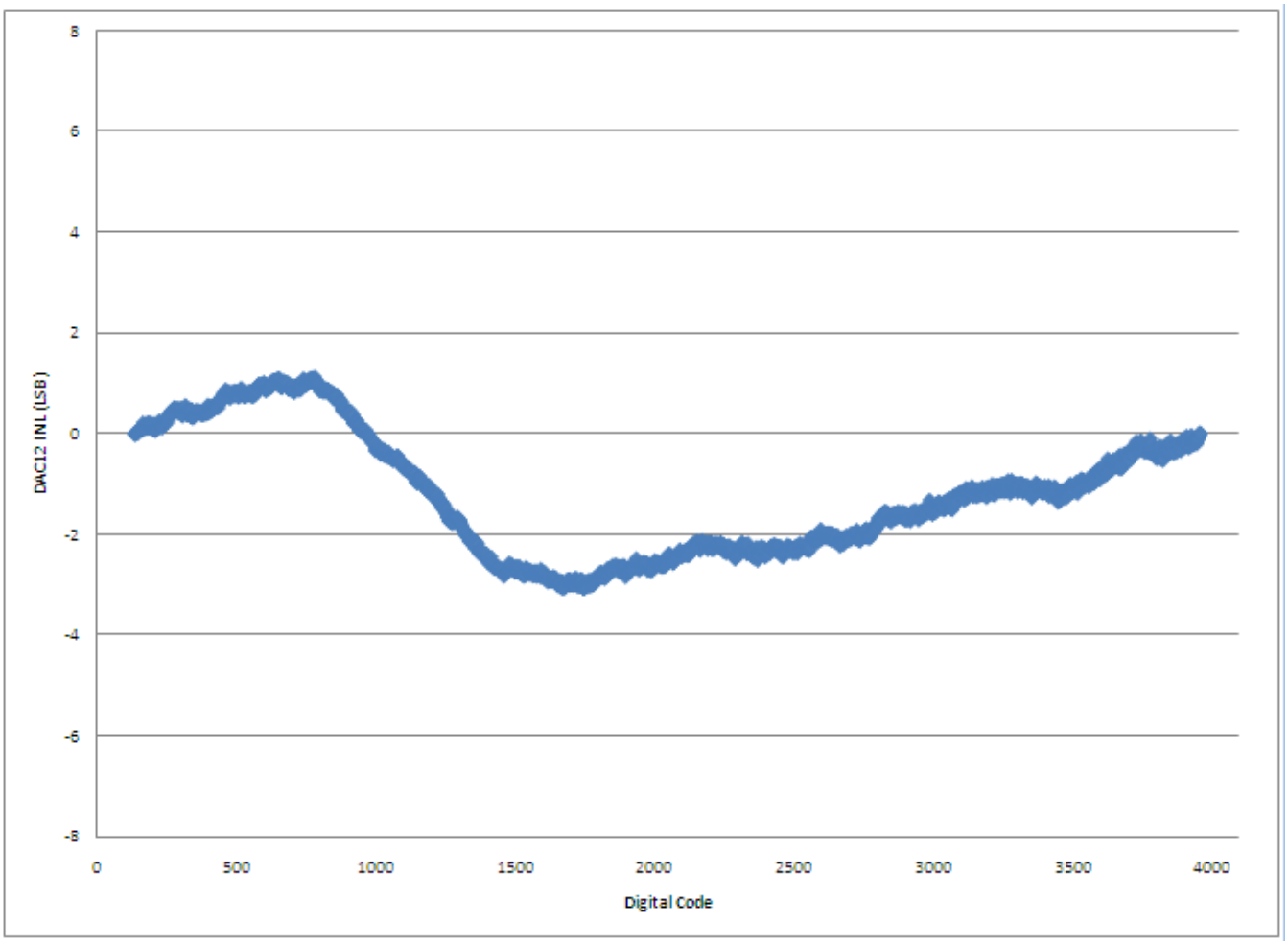


Figure 17. Typical INL error vs. digital code

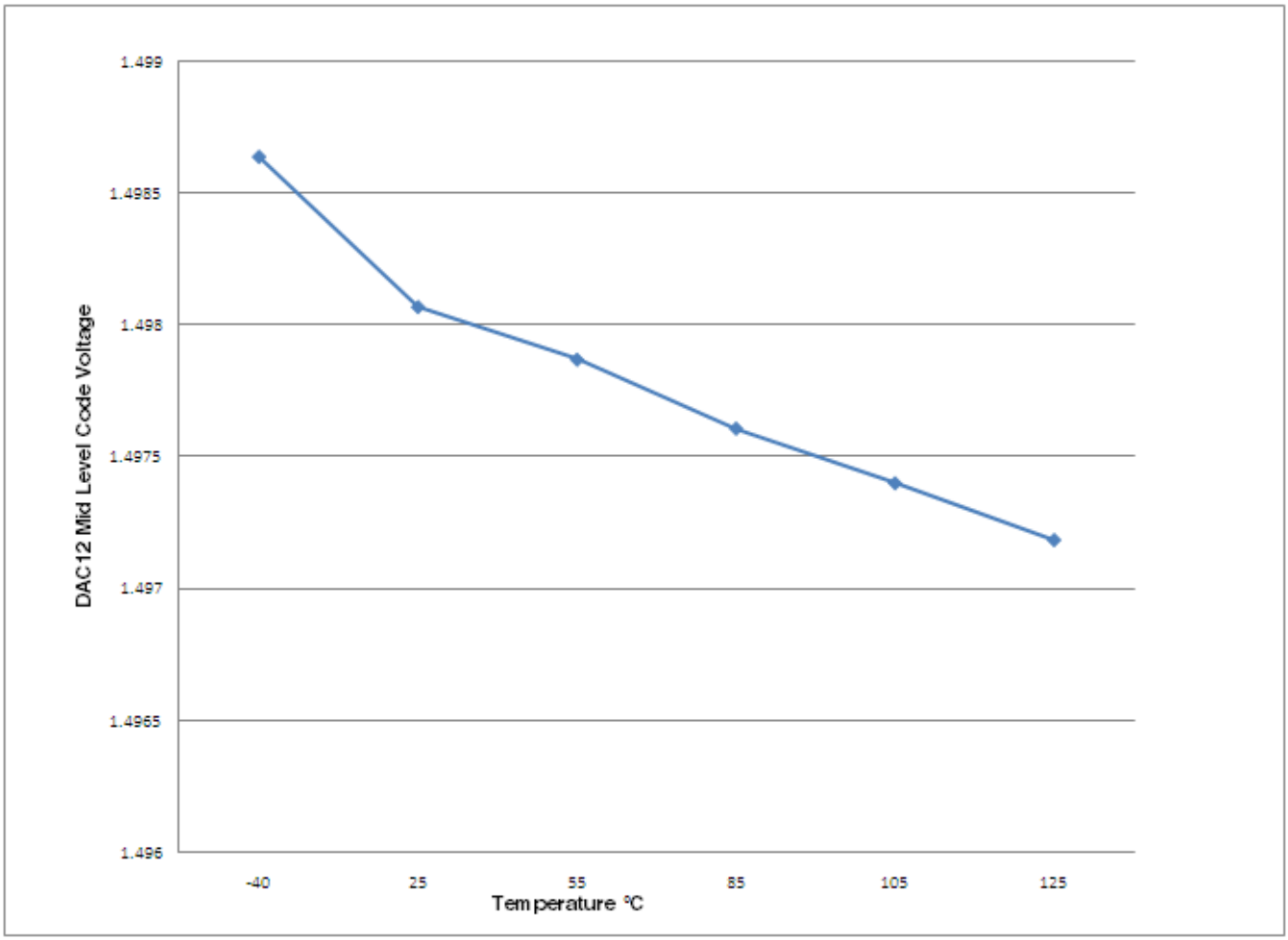


Figure 18. Offset at half scale vs. temperature

6.6.4 Op-amp electrical specifications

Table 34. Op-amp electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	1.71	—	3.6	V
I_{SUPPLY}	Supply current (I_{OUT}=0mA, CL=0), low-power mode	—	92	195	µA
I_{SUPPLY}	Supply current (I_{OUT}=0mA, CL=0), high-speed mode	—	465	865	µA
V_{OS}	Input offset voltage	—	±3	±10	mV
α_{VOS}	Input offset voltage temperature coefficient	—	10	—	µV/C
I_{OS}	Typical input offset current across the following temp range (0–50°C)	—	±500	—	pA
I_{OS}	Typical input offset current across the following temp range (-40–105°C)	—	4	—	nA

Table continues on the next page...

Table 38. TRIAMP limited range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OS}	Input offset voltage	—	±3	±5	mV	
α_{VOS}	Input offset voltage temperature coefficient	—	4.8	—	µV/C	
I_{OS}	Input offset current	—	±300	±600	pA	
I_{BIAS}	Input bias current	—	±300	±600	pA	
R_{OUT}	Output AC impedance	—	—	1500	Ω	@ 100kHz, High speed mode
$\|X_{IN}\|$	AC input impedance (f_{IN}=100kHz)	—	159	—	kΩ	
CMRR	Input common mode rejection ratio	—	70	—	dB	
PSRR	Power supply rejection ratio	—	70	—	dB	
SR	Slew rate (ΔV_{IN}=500mV) — Low-power mode	0.1	—	—	V/µs	
SR	Slew rate (ΔV_{IN}=500mV) — High speed mode	1.5	3.5	—	V/µs	
GBW	Unity gain bandwidth — Low-power mode 50pF	0.15	—	—	MHz	
GBW	Unity gain bandwidth — High speed mode 50pF	1	—	—	MHz	
A_V	DC open-loop voltage gain	80	—	—	dB	
GM	Gain margin	—	20	—	dB	
PM	Phase margin	60	69	—	deg	

6.6.7 Voltage reference electrical specifications

Table 39. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 40. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	

Table continues on the next page...

Table 40. VREF full-range operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only current	—	—	80	µA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 41. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 42. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General switching specifications.

6.8 Communication interfaces

6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

6.8.2 USB DCD electrical specifications

Table 43. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}	USB_DM sink current	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 USB VREG electrical specifications

Table 44. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

Table 46. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

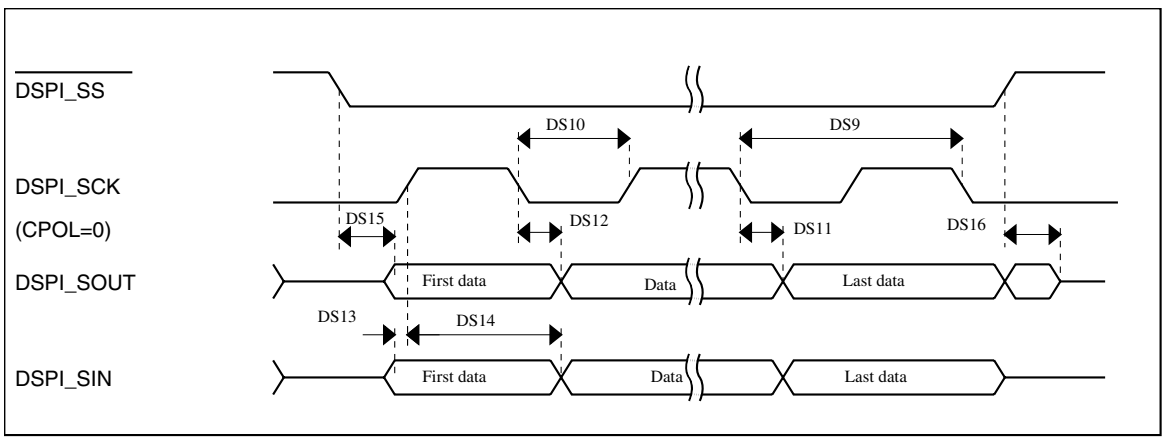


Figure 20. DSPI classic SPI timing — slave mode

6.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 47. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2

Table continues on the next page...

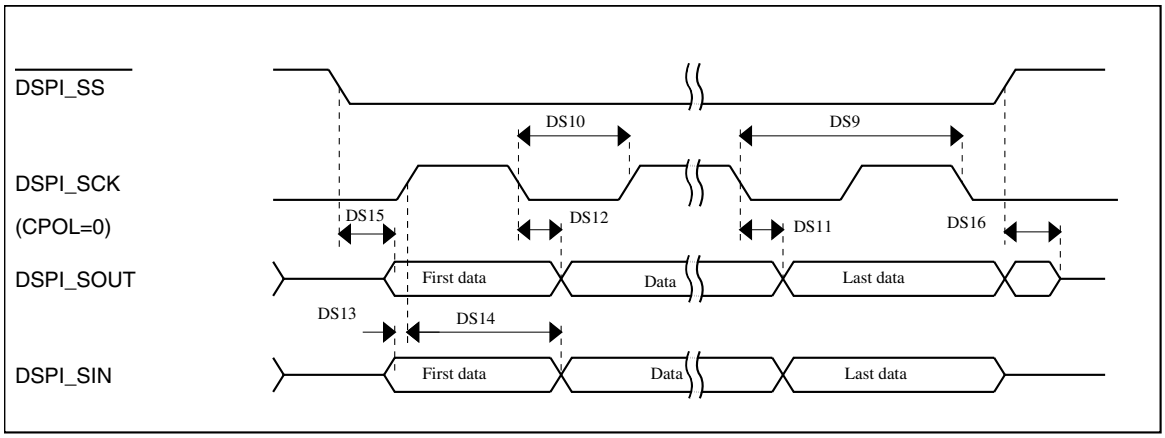


Figure 22. DSPI classic SPI timing — slave mode

6.8.6 Inter-Integrated Circuit Interface (I^2C) timing

Table 49. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
62	M9	PTA10	DISABLED		PTA10		FTM2_CH0		FB_AD15	FTM2_QD_PHA	TRACE_D0	
63	L9	PTA11	DISABLED		PTA11		FTM2_CH1		FB_OE_b	FTM2_QD_PHB		
64	K9	PTA12	CMP2_IN0	CMP2_IN0	PTA12		FTM1_CH0		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b	I2S0_TXD0	FTM1_QD_PHA	
65	J9	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4		FTM1_CH1		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	I2S0_TX_FS	FTM1_QD_PHB	
66	L10	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX		FB_AD31	I2S0_RX_BCLK	I2S0_TXD1	
67	L11	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX		FB_AD30	I2S0_RXD0		
68	K10	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b/ UART0_COL_b		FB_AD29	I2S0_RX_FS	I2S0_RXD1	
69	K11	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b		FB_AD28	I2S0_MCLK		
70	E8	VDD	VDD	VDD								
71	G8	VSS	VSS	VSS								
72	M12	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
73	M11	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
74	L12	RESET_b	RESET_b	RESET_b								
75	K12	PTA24	DISABLED		PTA24				FB_AD14			
76	J12	PTA25	DISABLED		PTA25				FB_AD13			
77	J11	PTA26	DISABLED		PTA26				FB_AD12			
78	J10	PTA27	DISABLED		PTA27				FB_AD11			
79	H12	PTA28	DISABLED		PTA28				FB_AD10			
80	H11	PTA29	DISABLED		PTA29				FB_AD19			
81	H10	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA	LCD_P0	
82	H9	PTB1	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB	LCD_P1	
83	G12	PTB2	LCD_P2/ ADC0_SE12/ TSI0_CH7	LCD_P2/ ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3	LCD_P2	
84	G11	PTB3	LCD_P3/ ADC0_SE13/ TSI0_CH8	LCD_P3/ ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_b			FTM0_FLT0	LCD_P3	

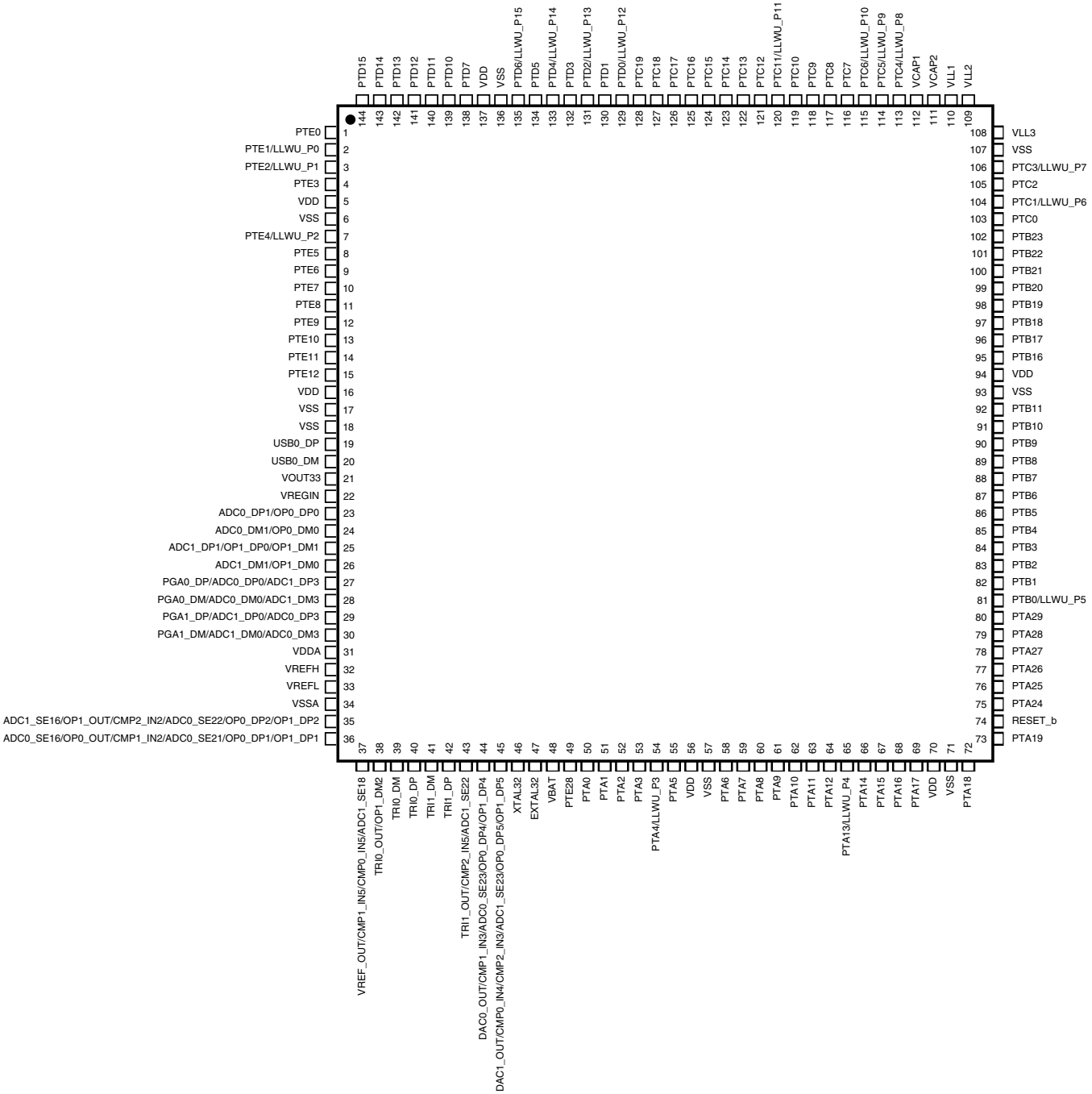


Figure 31. K51 144 LQFP Pinout Diagram